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LL9000 Series HCMOS Logic Arrays

Description

The LL9000 series of silicon-gate HCMOS logic arrays from LSI Logic Corporation exhibits bipolar speeds, while at the same time, offers low power consumption, high noise margins and ease of design. The LL9000 series is implemented in silicon-gate 1.5-micron drawn gate length, 2-layer metal interconnection technology. A range of array sizes from 880 to 10,013 gates is offered. Each gate is equivalent to a 2-input NAND or NOR. Maximum pin counts range up to 224.

The speed and range of gate counts available in the LL9000 series make it ideal for LSI and VLSI implementation of a variety of high-performance functions. The high-density members can be used for VLSI implementation of complete high-performance subsystem architectures such as intelligent special-purpose processors or multifunction controllers. The low gate count members can be used for the replacement of high-speed logic such as Schottky TTL or even 10K ECL. The intermediate members can be used for high-performance dedicated peripheral controllers, intelligent support functions, etc.

Features

- Silicon-gate 1.5-micron (1.1-micron effective) HCMOS technology
- Speeds higher than 74S TTL — 1.0 ns through 2-input NAND gate and interconnection, TA = 25°C, fanout = 2, VDD = 5 V
- Directly compatible with LL7000 series macrocell and macrofunction libraries
- Optimal structure of two n-channel and two p-channel transistors
- Complexities ranging from 880 to 10,013 gates
- Pin counts ranging up to 224
- Fully supported by LDS® (LSI Design System)
- All non-power pads configurable as inputs, outputs or bidirectional I/O
- TTL/CMOS I/O compatibility
- Configurable output drive up to 12 mA under worst-case commercial conditions
- Input protection circuitry
- LL93200 evaluation device available
- Full military capability
- Ceramic and plastic packages

Product Outline

Device Number	Gate Complexity	Maximum Pads[3]		Maximum I/O Pads[3]		Maximum Package Pins[4]		Gate Speed (ns)[1]	
		Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic	Typ	Max[2]
LL9080	880	52	68	44	60	50	66	1.0	1.74
LL9140	1443	66	86	58	78	64	84	1.0	1.74
LL9220	2224	78	106	70	98	76	104	1.0	1.74
LL9320	3192	96	128	80	112	92	124	1.0	1.74
LL9420	4242	114	150	98	134	110	146	1.0	1.74
LL9600	6072	138	186	122	170	134	182	1.0	1.74
LL9840	8370	166	222	150	206	162	218	1.0	1.74
LL91000	10,013	174	232	158	216	170	224	1.0	1.74

Notes:

1. 2-input NAND gate, fanout = 2; and statistically necessary interconnection.
2. TA = 0°C to 70°C, VDD = 5 V ± 5%.
3. The difference between the maximum number of pads and I/Os is the number of dedicated VDD or VSS pads. It may be necessary to configure additional I/O pads for VDD/VSS, depending on the number and drive of the output buffers.
4. Wherever possible, the lower pad count plastic or ceramic pad pitch should be used.

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Product Description

The LL9000 series of arrays is manufactured using an advanced 1.5-micron, oxide-isolated silicon-gate HCMOS fabrication process. The use of short channel lengths, thin gate oxides and two levels of metal interconnection provides bipolar speeds. The small device structures and low power consumption also allow high gate counts due to the smaller chip size and the minimal heat dissipation. The LL9000 series eliminates the need for bipolar technology and its attendant limitations such as low-to-medium complexities, special packaging, cooling, lower noise immunity, etc.

Macrocells

The arrays consist of columns of gates in the core region, I/O buffers around the periphery, and wiring channels in-between. Each gate consists of two n-channel and two p-channel transistors. These gates can be configured into a variety of logic elements such as exclusive-OR gates or flip-flops using unique metal interconnections. These elements are called macrocells and are the basic building blocks available to the user. The LL9000 series contains over 150 macrocells. Macrocells needed to support scan testing are available.

Macrofunctions

Logic functions with higher complexity are also available. These more complex elements, called macrofunctions, are composed of macrocells. Simple macrofunctions are, in turn, used to hierarchically build higher-level macrofunctions until the logic is completely specified.

For user convenience, a selection of macrofunctions composed of macrocells is also available in the LL9000 library. These macrofunctions implement generic functions such as counters, decoders, shift registers, etc., and are optimized for gate usage and for performance characteristics. In some cases, such as upgrading existing products that use 7400/4000 series MSI/SSI functions, or because of previous familiarity, designers may prefer to use 7400/4000 series functions as building blocks. A large selection of these elements is also provided in the LL9000 series macrofunction library.

Table 1 lists some representative macrofunctions. Detailed information on available macrocells and macrofunctions is provided in other LSI Logic publications. The "AC Characteristics" section lists some of the commonly used macrofunctions, their propagation delays and their complexity.

Macrocells for Level-Sensitive Scan Design

The LL9000 series macrocell library also contains macrocells needed to support scan testing. Scan testing is the capability to serially shift the contents of all internal flip-flops off-chip in a test mode.

Table 1. Representative Macrofunctions Available in the LL9000 Series

Adders Up to 16 bits	**Decoders** 2-to-4 decoders 3-to-8 decoders 4-to-10 decoders
Comparators Magnitude Equality 4 and 8 bits	**ALUs** 16-bit 181 type
Parity Generators 8-bit odd parity detector	**2900 Family** 2901 2909 2910
Registers 8-bit data latch 8-bit data register, clear and direct 4-bit shift register, sync parallel load and clear 4-bit shift register, async parallel load	**FIFO** 16×4
Counters Binary, BCD, Gray and Johnson counters in a variety of configurations Large modulo counters	**Multipliers** 8×8 12×12 16×16
Clock Generators 2-phase clock generator, buffered	

I/O Buffers

Each I/O buffer around the perimeter of the array consists of an input protection circuit and large n- and p-channel transistors for driving off-chip loads. All non-power peripheral cell locations can be used as input, output or bidirectional 3-state cells. If necessary, they can even be used to buffer heavily loaded internal signals such as clock nets. Further flexibility is provided by pullup/pulldown resistors and choice of input levels and current drive:

- All I/O pads have pullup and pulldown resistors (typically 80K Ω)
- Output drive can be tailored to 1.0 mA, 2.0 mA or 4.0 mA. Additional drive capability can be obtained by paralleling two (8.0 mA) or three (12.0 mA) drivers
- Three input voltage options are available on any input/output pin. CMOS input buffers provide standard 1.5 V and 3.5 V input levels. TTL input buffers provide standard 0.8 V and 2.0 V (2.25 V on industrial and military devices) input levels. Schmitt trigger inputs provide 1.5 V hysteresis. See the "DC Characteristics" section for more details.
- All I/Os are protected against latch-up and electrostatic discharge

Propagation Delays

Propagation delays of the LL9000 series macrocells are a function of several factors:

- Fanout
- Interconnection routing
- Junction temperature
- Supply voltage
- Processing tolerance
- Input transition time
- Input signal polarity

The LDS design verifier program generates the propagation delays for all networks automatically once the network has been entered into the development system or workstation. Prior to layout, these values are based on the estimated interconnections. After layout, the program is re-run and final delay values based on actual interconnections are obtained.

Prior to availability of the network in computer format, approximate delays may be calculated as follows:

Propagation delays for some popular macrocells are shown in the "AC Characteristics" section for nominal processing, 5 V operation, 25°C temperature and for various fanouts, with statistically estimated wirelengths.

The effect of temperature may be estimated from Figure 1. The maximum junction temperature corresponds to a temperature multiplier (KT). In CMOS technology, the junction temperature is usually equal or very close to the ambient temperature. Similarly, Figure 2 shows the effect of supply voltage (KV). LSI Logic assumes a 40% variability resulting from all other factors including processing, that is, a factor of 1.4 for the worst-case processing multiplier (KO).

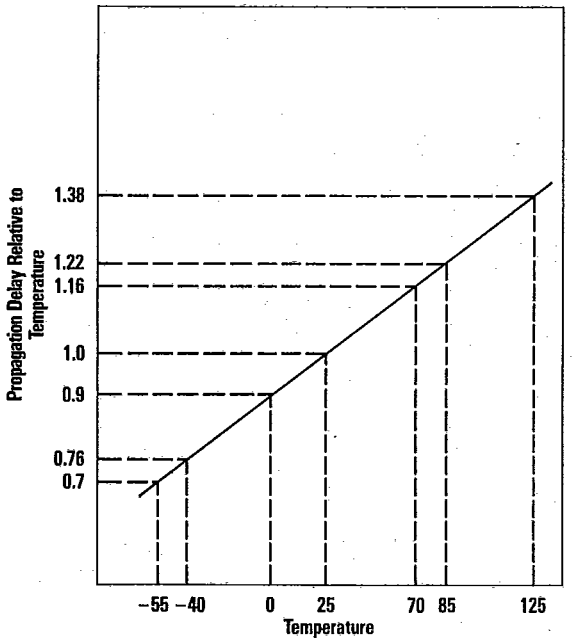

Figure 1: CMOS Propagation Delays as a Function of Temperature

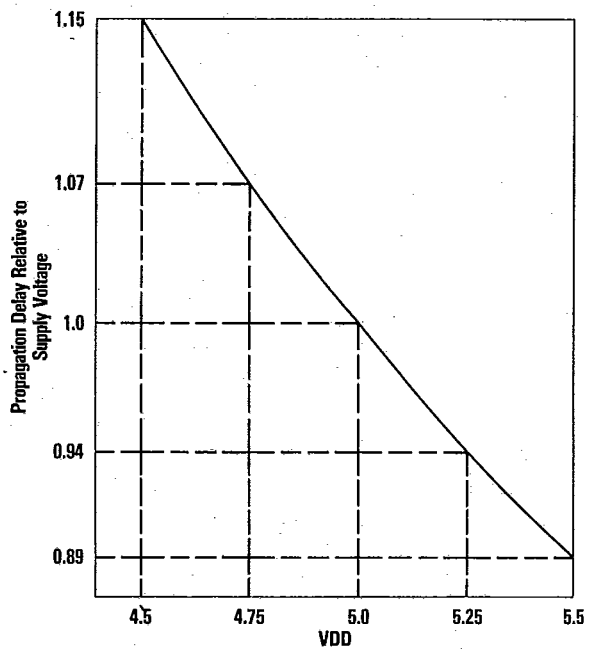

Figure 2. CMOS Propagation Delays as a Function of Supply Voltage

Propagation Delays (Continued)

The maximum propagation delay is

$$TMAX = KO \bullet KT \bullet KV \bullet TTYP$$

A simple example will illustrate the technique.

The circuit of Figure 3 must operate over 0°C to 70°C, and 4.75 V to 5.25 V power supply voltage. Using Figures 1 and 2 and the KO multiplier, we determine the worst-case maximum delay to be $1.4 \times 1.16 \times 1.07 = 1.74$ times the typical delay.

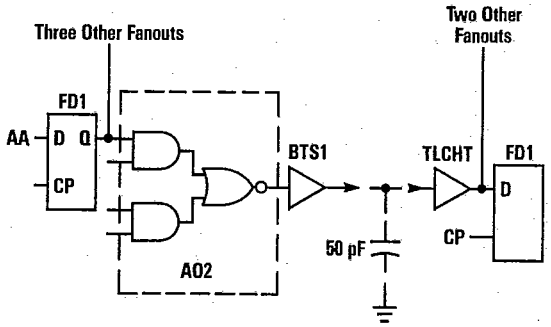

Figure 3. Example of Worst-Case Propagation Delay through Critical Path

The FD1 flip-flop, clocked by the signal CLK, feeds an AO2 AND-NOR gate combination and three other loads. The AO2 drives a BTS1 3-state buffer directly. The BTS1 drives off-chip, through a PC board, and on to another array using a TLCHT input level shifter. The total capacitance at the output, interconnect, and input is 50 pF. The TLCHT drives the D input of an FD1 D flip-flop and two other loads. The delay characteristics of all the macrocells are tabulated in Table 2. The total clock-to-clock delay is 11.58 ns typical, $11.58 \times 1.74 = 20.15$ ns worst-case. LDS programs are used to obtain accurate delays after the logic has been entered into the system.

Table 2. Propagation Delay Calculation

Input Signal AA	FD1 Load (4)	AO2 Load (3.5)	3-state Output BTS1 CL=50 pF	TLCHT Load (5)	FD1 Set-up	Typical Path Delay	W. C. Path Delay
Goes HIGH	2.94	2.70	3.01	2.35	1.1	11.58	20.15
Goes LOW	2.42	0.99	2.06	4.11	1.1	11.2	19.49

Note that the signal is inverted at the output of AO2.

Product Options Available

The LL9000 series is offered in a variety of operating temperature ranges and production processing flows. The following standard operating temperature ranges are offered:

- Military (−55°C to +125°C)
- Industrial (−40°C to +85°C)
- Commercial (0°C to +70°C)

Other special temperature ranges are also available.

Production flow options other than LSI Logic's standard commercial flow are available. Various military flows including MIL-STD-883 Level B are supported. Full MIL 38510 qualification is available when required.

Packaging

The LL9000 series can be packaged in a variety of plastic and ceramic dual in-line packages, leadless and leaded chip carriers, and pin-grid arrays. Plastic packages are not available for the full military temperature range. The compatibility chart of Table 3 shows the packages and pin counts available for the various members of the LL9000 series.

Table 3. Package Selector Guide for the LL9000 Series

Device	Dual In-Line Packages		Chip Carriers		Pin-Grid Arrays	
	Plastic	Ceramic	Plastic	Ceramic	Plastic	Ceramic
LL9080	22+	22+	N/A	20+	68+	64+
LL9140	22+	22+	44+	28+	68+	64+
LL9220	22+	22+	44+	28+	68+	64+
LL9320	24+	24+	44+	44+	68+	64+
LL9420	28+	44+	44+	52+	68+	64+
LL9600	28+	40+	44+	68+	68+	64+
LL9840	N/A	64+	68+	84+	68+	68+
LL91000	N/A	64+	68+	84+	68+	68+

Package families include:
Ceramic DIPs—24, 28, 40, 42, 48 and 64 leads
Plastic DIPs—24, 28, 40, 48 and 64 (0.070" pitch) leads
Ceramic chip carriers—28, 44, 52, 68, 84 and 100 leads
Plastic chip carriers—68, 84 and 124 leads
Ceramic pin-grid arrays—64, 68, 84, 100, 120, 144, 180 and 224 leads
Plastic pin-grid arrays—68, 84, 100, 120, 144 and 180 leads

LL9320Q Evaluation Device

A user of the LL9000 series can, prior to design commencement, measure its performance under his unique system and environmental conditions. The LL9320Q contains a variety of logic functions such as 2-, 3-, or 4-input NAND gates, 2- or 4-input NOR gates, output buffers with different drive capability, a variety of different flip-flops, inverters, TTL-to-CMOS level-shifters, etc. In addition, complex circuits such as ALUs and up-down counters are included. These functions are implemented in several different test circuits. Technology parameters such as propagation delays, power consumption, input/output characteristics, etc., can be measured under different conditions of loading, supply voltage, ambient temperature, etc.

Getting Started on the Design

To get started on a logic array design, the following sequence of preliminary steps is suggested.

1. The complete system is partitioned into LSI building blocks. An effort should be made to minimize the I/O count when partitioning between circuits. Each functional block to be implemented in a logic array is then converted to a logic schematic. The user can describe his logic using LSI Logic's megafunction, macrofunction or macrocell libraries or 7400/4000 series functions. The user of hierarchical design techniques on the LDS design system allows design expression at these various levels. Ultimately, when the logic is compiled on LDS, it is "flattened" into macrocells. It is advisable to structure the complete schematic as a set of functional subsystems such as a 16-bit ALU, a data receiver, a programmable timer or a register file, to allow comprehensible and easy hierarchical simulation.

2. The base clock frequency and the critical path timing are necessary to make the correct choice of technology. The LL9000 series can typically support designs operating beyond 50 MHz. The critical path timing is determined based on macrocell propagation delays (see the "Propagation Delays" and "AC Characteristics" sections). To verify the capability of a technology under the unique environmental and system conditions of a user application, an evaluation device such as the LL9320Q may be used.

3. The next step is an estimation of the gate count and I/O requirements of the logic to establish the complexity of the array required. The gate utilization actually achieved in a given array for a specific design depends on the gate count, pin requirements, as well as factors that affect routability. For example, block-oriented logic with minimum inter-block interaction provides high utilization, whereas wide, extensive bussing lowers it.

4. Finally, a choice of array size, package, temperature range and performance is made.

During all these steps, the customer usually consults LSI Logic to ensure compatibility and completeness of the design specifications.

A set of specifications is then submitted to LSI Logic. After their acceptance, the logic designer takes the one-week LDS training class and starts his design. The design process and the user interface to LDS are oriented toward the skills of a system designer rather than a semiconductor device or VLSI designer. Alternatively, the customer can contract LSI Logic for a turnkey design.

Design Support and Interface

The LDS system may be used for logic specification, basic network verification (gate usage, I/O pad usage, average fanout per net, estimated automatic wireability), logic simulation and performance analysis, automatic placement and routing, resimulation with actual wirelengths to verify the AC performance, mask PG tape generation and test tape generation. The basic design flow is outlined in Figure 7.

VDD and VSS Requirements

HCMOS is fast technology rivaling Schottky TTL speeds. High-speed operation places stringent requirements on the ground bussing and the number of power and ground pads required to avoid current spikes when the output buffers charge and discharge their output capacitance.

To increase noise immunity, two ground busses (VSS and VSS2) are used on the array. All inputs and interior logic are on the VSS2 bus, all output buffers on the VSS bus. These two busses are connected to independent package ground pin.

VDD and VSS Requirements (Continued)

More than two power (VDD) and ground (VSS) pins may be required to support several high-drive outputs switching simultaneously at high speed. For example, the type B1 buffer has a low impedance for high drive capability and may provide a peak transient current of 60 mA. If 16 B1 buffers switch simultaneously, a peak current of nearly one amp is generated through the VSS bus, bonding wire, package and out to the PC board. There are therefore guidelines on the number of required VSS and VDD pins based on three factors:

- The driver capability of the buffer
- The number of buffers switching simultaneously
- The location of power and ground pads relative to the outputs

Each VSS pad can support a maximum of 16 B1 equivalent buffers (8 on each side of the VSS pad). Each VDD pad can support up to 32 B1 equivalent B1 buffers (16 on each side). The number of VSS2 pads required depends on the array size and on the number of output buffers used. Figure 4 shows the minimum number of VSS2 pads required by each array size.

Array	Minimum Number of VSS2 Pads Required
LL9080	2
LL9140	2
LL9220	2
LL9320	4
LL9420	4
LL9600	4
LL9840	4
LL91000	4

Figure 4. Minimum Allowable VSS2 Pads Required by Each Array Size

Output types can be mixed: high drive when needed, low drive when acceptable to reduce noise and power dissipation. Note that inputs may be ignored when calculating power pins since CMOS inputs sink and source minimal current. Figure 5 shows the current drive capabilities of some of the more common output buffer types compared to the B1 buffer.

Buffer Type	B1 Equivalent Drive Capability
B14	0.25
B18	0.5
B1	1
B2	2
B3	3

Figure 5. Current Drive Capabilities of Output Buffer Types

Figure 6 shows the footprint for the LL9600P array. Dedicated VSS, VSS2, and VDD power pads are separated into primary and secondary pads. The primary pads are grouped together in sets of two or four at the midpoint of each of the four sides. The secondary pads are located individually near the four corners of the chip. All primary pads must be used first. Primary pads cannot be used as signal pads. If additional power pads are required, then the secondary pads will be used. All secondary pads not used for power may be used as a signal pad. Similar footprints for other array sizes are available from LSI Logic.

If pin count is high, request a "tight pitch" footprint — each LL9000 series device is available with shorter pad-to-pad spacing, or a "tighter pad pitch," allowing approximately 25% more pads. This pad pitch is designed for use with ceramic packages.

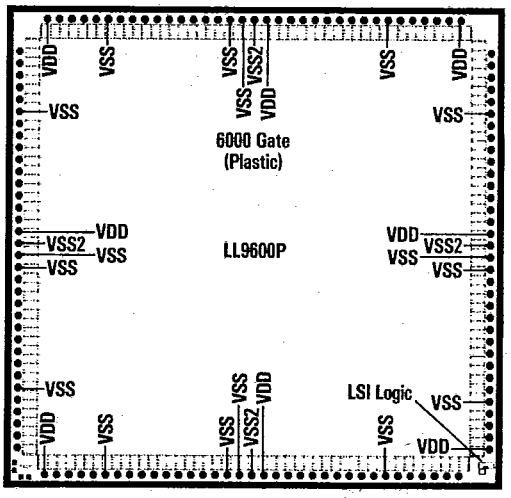

Figure 6. LL9600 Footprint (Plastic Pad Pitch)

Power Dissipation

Power dissipation in CMOS circuits is made up of four basic elements.

The first is due to leakage. It constitutes the quiescent power dissipation and is essentially negligible (few microwatts) for CMOS technology.

The second is DC current through ON transistors. This can be from a variety of sources:

- a low on an input with a pullup resistor (all TTL inputs have nominal 80K Ω pullup resistors)
- outputs which sink or source current
- any unconnected inputs without a pullup or pulldown
- any internal gates whose inputs are floating (e.g., a data bus with all the lines disabled)
- inputs at worst-case levels, particularly TTL inputs at 2 V

Care should be exercised during logic design to make sure that there is a test condition in which all this DC current may be turned off, so that DC leakage may be easily measured.

The third source of power dissipation is due to overlap currents when the p- and n-transistors are switching from the high-to-low state or vice-versa. This contributes less than 10% of the power dissipated and occurs for the transition period when $VTH(N) < VIN < VDD - VTH(P)$.

The fourth and most important factor is the charging and discharging of circuit capacitance. The charging of a capacitor C to a voltage V through a p-channel device builds up a charge CV and stores energy CV^2. This energy is later discharged through an n-channel transistor in the CMOS p-n pair. When such switching takes place at a frequency 'f', the resulting power dissipated in the CMOS circuit is equivalent to $P = CV^2f$. This AC power dissipation usually contributes in excess of 90% of the total power dissipated. Thus, the power dissipation in a CMOS circuit is essentially a function of the frequency and logic configuration. Each internal gate in the LL9000 series typically consumes 18 μW/gate/MHz. Each output buffer, with its higher output capacitance and larger capacitive loads, consumes 25 μW/output/MHz/pF. The total power consumption is the sum of the power dissipated by all the gates and output buffers switching each cycle. Table 4 illustrates typical power calculations.

Table 4. Power Dissipation Calculation Example

Parameter	Array Type	
	LL9220	LL9600
Number of available gates	2224	6072
Percentage of gates utilized (%)	85	75
Number of gates utilized	1890	4554
Number of gates switching each cycle (15%)	284	683
Dissipation/gate/MHz (μW)	18	18
Total core dissipation/MHz (mW)	5.1	12.3
Number of available I/O buffers	98	170
Percentage of I/O buffers utilized (%) as outputs	50	50
Number of I/O buffers utilized as outputs	49	85
Number of I/O outputs switching each cycle (20%)	10	17
Dissipation/output buffer/MHz/pF (μW)	25	25
Output capacitive load (pF)	50	50
Dissipation/output buffer/MHz (mW)	1.60	1.60
Total output buffer dissipation/MHz (mW)	16.0	27.2
Total dissipation/MHz (mW)	21.1	39.5
Total dissipation at 10 MHz clock speed (mW)	211	395
Total dissipation at 25 MHz clock speed (mW)	528	988

Reliability and Quality Assurance

The Reliability Department provides LSI Logic with a number of programs to define product reliability levels. Among these programs are: (1) qualification, (2) monitor, (3) failure analysis, and (4) data collection and presentation. The reliability monitor program is designed to assure that all products manufactured and shipped to customers comply with Corporate reliability policy.

The reliability plan is implemented during the development phase when actual test structures and working devices are implemented in silicon. High stress tests are performed to identify and quantify potential failure mechanisms. High stress reliability testing is continued during limited production on units manufactured using defined processes.

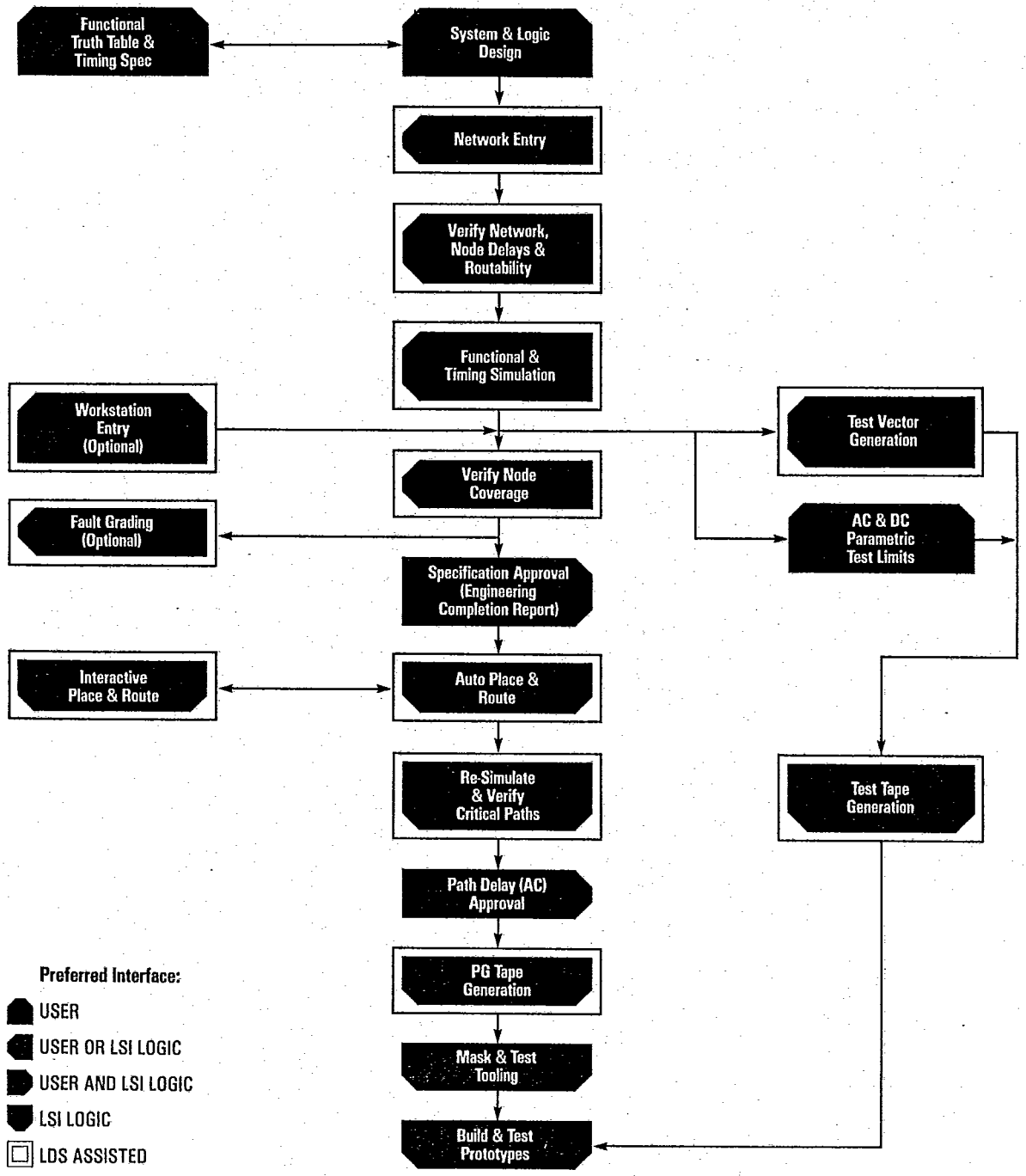

Figure 7. LDS Design Flow

Reporting and Publication of Data

Qualification test reports are prepared and distributed by Reliability for all products or processes which are approved by formal qualification testing for use in the manufacture of LSI Logic products. These reports contain a statement of qualification that certifies the process or product for use by LSI Logic.

New packages are approved and released for production by Reliability after prescribed environmental tests have been completed successfully. All testing is done according to the applicable methods of MIL-STD-883, Level B. Testing methods used include, but are not limited to, the following:

Operating Life	Method 1005
Temperature Cycling	Method 1010
Constant Acceleration	Method 2001
Salt Atmosphere	Method 1009
Lead Integrity	Method 2004
Solderability	Method 2003

In addition, the following are performed on plastic devices:

Biased Humidity	85°C/85% Relative Humidity
Pressure Cooker	TA = 121°C, 15 psig 100% Relative Humidity

See Reliability Data Summary for more details.

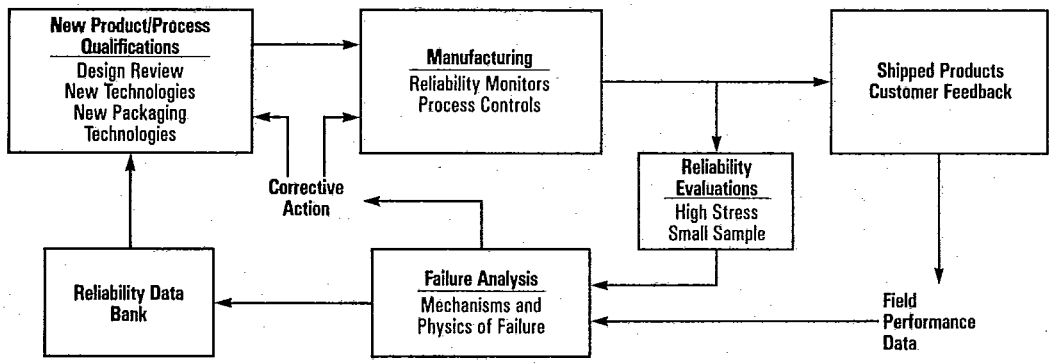

Figure 8

Operating Characteristics

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	−0.3 to +7	V
Input Voltage	VIN	−0.3 to VDD +0.3	V
DC Input Current	IIN	±10	μA
Storage Temperature Range (Ceramic)	TSTG	−65 to +150	°C
Storage Temperature Range (Plastic)	TSTG	−40 to +125	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+3 to +6	V
Operating Ambient Temperature Range · Military	TA	−55 to +125	°C
Industrial Range	TA	−40 to +85	°C
Commercial Range	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V ±5% ambient temperature over the specified temperature range[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIL	Voltage Input LOW					
	TTL Inputs				0.8	V
	CMOS Levels				0.3 VDD	V
VIH	Voltage Input HIGH					
	TTL Inputs, Commercial Temperature Range		2.0			V
	TTL Inputs, Military and Industrial Temperature Range		2.25			V
	CMOS Levels		0.7 VDD			V
VT+	Schmitt-Trigger, Positive-going Threshold			3.0	4.0	V
VT−	Schmitt-Trigger, Negative-going Threshold		1.0	1.5		V
⎍	Hysteresis, Schmitt Trigger	VIL to VIH VIH to VIL	1.0	1.5		V
IIN	Input Current, CMOS, TTL Inputs without Pullup, Pulldown Resistors	VIN = VDD or VSS	−10	±1	10	μA
	Inputs with Pulldown Resistors	VIN = VDD	20	70	230	μA
	Inputs with Pullup Resistors	VIN = VSS	−350	−110	−35	μA
VOH (TTL)	Voltage Output HIGH	Comm / Mil				
	Type B14	IOH = −1 mA / −0.8 mA	2.4	4.5		V
	Type B18	IOH = −2 mA / −1.6 mA				
	Type B1	IOH = −4 mA / −3.2 mA				
	Type B2[2]	IOH = −8 mA / −6.4 mA				
	Type B3[3]	IOH = −12 mA / −9.6 mA				
VOL (TTL)	Voltage Output LOW	Comm / Mil				
	Type B14	IOL = 1 mA / 0.8 mA		0.2	0.4	V
	Type B18	IOL = 2 mA / 1.6 mA				
	Type B1	IOL = 4 mA / 3.2 mA				
	Type B2[2]	IOL = 8 mA / 6.4 mA				
	Type B3[3]	IOL = 12 mA / 9.6 mA				
IOZ	3-State Output Leakage Current	VOH = VSS or VDD	−10	±1	10	μA
IOS	Output Short Circuit Current[4]	VDD = Max, VO = VDD VDD = Max, VO = 0 V	20 −10	60 −35	140 −100	mA mA
IDD	Quiescent Supply Current	VIN = VDD or VSS	User-Design Dependent			
CIN	Input Capacitance	Any Input[5]	2			pF
COUT	Output Capacitance	Any Output[6]	4			pF

Notes:

1. Military temperature range is −55°C to +125°C, ±10% power supply (ceramic packages only); industrial temperature range is −40°C to +85°C, ±5% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Requires two output pads.
3. Requires three output pads.
4. Type B1 output. Output short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.
5. Not applicable to assigned bidirectional buffer (excluding package).
6. Output using single buffer structure (excluding package).

AC Characteristics: VDD = 5 V, TA = 25°C (All values in nanoseconds, unless otherwise stated.)

Macrocell	Input Transition	Propagation Delays: Output Load Capacitance 15 pF	50 pF	85 pF	100 pF	Equivalent Gate Count
UNIDIRECTIONAL BUFFERS						
3-state Output Buffer with 1 mA Drive (BTS14)	tPHL tPLH	5.54 3.56	13.0 6.36	20.56 9.15	23.76 10.34	5
3-state Output Buffer with 12 mA Drive (BTS3)	tPHL tPLH	3.44 3.55	4.32 3.83	5.20 4.11	5.58 4.23	11
3-STATE BIDIRECTIONAL BUFFERS						
3-state I/O Buffers with 4 mA Drive (BTS7)	tPHL tPLH	3.18 3.03	5.08 3.79	6.93 4.55	7.79 4.88	7
3-state I/O Buffers with Pullup (BTS7U)/ Pulldown (BTS7D)	tPHL tPLH	3.18 3.03	5.08 3.79	6.98 4.55	7.79 4.88	7

AC Characteristics (Continued): VDD = 5 V, TA = 25°C (All values in nanoseconds, unless otherwise stated.)

Macrocell	Input Transition	Propagation Delays: Output Load Capacitance 15 pF	50 pF	85 pF	100 pF	Equivalent Gate Count
OUTPUT BUFFERS						
Output Buffer with 1 mA Drive (B14)	tPHL tPLH	5.10 2.90	12.52 5.70	20.12 8.50	23.32 9.68	1
Output Buffer with 12 mA Drive (B3)	tPHL tPLH	4.10 3.98	4.98 4.26	5.87 4.54	6.24 4.66	2

		Fanout 1	2	3	4	8	Equivalent Gate Count
INPUT RECEIVERS							
Input Buffer with CMOS Inputs (IBUF)	tPHL tPLH	2.67 2.61	2.69 2.65	2.72 2.69	2.74 2.73	2.84 2.83	0
Input Buffer with Schmitt Trigger (SCHMDT1)	tPHL tPLH	3.52 2.37	3.57 2.47	3.63 2.58	2.68 2.69	3.90 3.12	3
Input Buffer with TTL Inputs (TLCHT)	tPHL tPLH	3.92 2.15	3.97 2.20	4.01 2.25	4.06 2.30	4.23 2.50	0
INTERNAL BUFFERS							
Single Inverter (IV)	tPHL tPLH	0.57 1.02	0.66 1.23	0.76 1.44	0.85 1.65	1.22 2.50	1
Power Inverter (IVP)	tPHL tPLH	0.42 0.84	0.46 0.95	0.51 1.05	0.56 1.15	0.76 1.58	2
LOGIC GATES							
2-input Exclusive OR (EO)	tPHL tPLH	1.90 1.52	1.96 1.63	2.02 1.74	2.08 1.85	2.32 2.28	3
2-input NAND (ND2)	tPHL tPLH	0.53 1.13	0.66 1.34	0.79 1.55	0.92 1.76	1.44 2.61	1
3-input NAND (ND3)	tPHL tPLH	0.73 1.36	0.90 1.57	1.07 1.78	1.25 1.99	1.95 2.84	2
4-input NAND (ND4)	tPHL tPLH	0.96 1.10	1.17 1.31	1.38 1.52	1.59 1.73	2.44 2.57	2
8-input NAND (ND8)	tPHL tPLH	2.51 2.27	2.56 2.38	2.61 2.49	2.67 2.59	2.88 3.02	6
2-input NOR (NR2)	tPHL tPLH	0.56 1.32	0.65 1.68	0.75 2.03	0.85 2.38	1.24 3.79	1
3-input NOR (NR3)	tPHL tPLH	0.58 2.01	0.68 2.53	0.78 3.05	0.88 3.56	1.28 5.63	2
4-input NOR (NR4)	tPHL tPLH	0.61 2.79	0.71 3.48	0.81 4.16	0.91 4.85	1.31 7.59	2
8-input NOR (NR8)	tPHL tPLH	1.62 3.54	1.67 3.64	1.71 3.75	1.76 3.86	1.95 4.29	6
FLIP-FLOPS							
D Flip-flop (FD1)	tPHL tPLH tS tH	2.01 2.29 1.10 0.80	2.14 2.51 1.10 0.80	2.28 2.72 1.10 0.80	2.42 2.94 1.10 0.80	2.97 3.81 1.10 0.80	5
D Flip-flop with Scan Test Inputs (FD1S)	tPHL tPLH tS tH	2.54 2.50 3.20 1.30	2.67 2.71 3.20 1.30	2.80 2.93 3.20 1.30	2.93 3.15 3.20 1.30	3.45 4.02 3.20 1.30	8
D Flip-flop with Set Direct, Clear Direct (FD3)	tPHL tPLH tS tH	2.01 2.29 1.10 0.80	2.14 2.51 1.10 0.80	2.28 2.72 1.10 0.80	2.42 2.94 1.10 0.80	2.97 3.81 1.10 0.80	7
D Flip-flop with Set Direct, Clear Direct, and Scan Test Inputs (FD3S)	tPHL tPLH tS tH	2.54 2.50 3.20 1.30	2.67 2.71 3.20 1.30	2.80 2.93 3.20 1.30	2.93 3.15 3.20 1.30	3.45 4.02 3.20 1.30	10

AC Characteristics (Continued): VDD = 5 V, TA = 25°C (All values in nanoseconds, unless otherwise stated.)

Macrocell	Input Transition	Fanout 1	2	3	4	8	Equivalent Gate Count
J-K Flip-flop (FJK1)	tPHL	1.97	2.10	2.24	2.37	2.91	8
	tPLH	2.60	2.82	3.03	3.25	4.11	
	tS	2.80	2.80	2.80	2.80	2.80	
	tH	0.90	0.90	0.90	0.90	0.90	
J-K Flip-flop with Scan Test Inputs (FJK1S)	tPHL	2.90	3.03	3.16	3.30	3.82	10
	tPLH	2.89	3.11	3.32	3.53	4.38	
	tS	4.30	4.30	4.30	4.30	4.30	
	tH	2.40	2.40	2.40	2.40	2.40	
LATCHES							
Gated D Latch (LD1)	tPHL	1.91	2.0	2.10	2.19	2.56	3
	tPLH	1.95	2.16	2.37	2.59	3.44	
	tS	1.10	1.10	1.10	1.10	1.10	
	tH	0.80	0.80	0.80	0.80	0.80	
S-R Latch with Separate Input Gates, Set Direct and Reset Direct (LSR1)	tPHL	1.01	1.19	1.36	1.54	2.24	4
	tPLH	1.81	2.17	2.53	2.88	4.31	
D Latch with Scan Test Inputs (LS1)	tPHL	1.81	1.97	2.07	2.18	2.59	6
	tPLH	2.49	2.71	2.92	3.14	4.00	
	tS	3.20	3.20	3.20	3.20	3.20	
	tH	0.80	0.80	0.80	0.80	0.80	
MISCELLANEOUS							
2-to-1 Multiplexer (MUX21LA)	tPHL	1.15	1.20	1.25	1.30	1.50	2
	tPLH	0.85	0.95	1.06	1.16	1.59	

Note: Delays through interconnect are included. Interconnect wirelengths are assumed from statistical distributions for given fanouts.

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