VTC Inc.
Value the Customer™

VM7230/VM7230N

2, 4, 6 OR 8-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

July, 1993

FEATURES

- High Performance
  - Read Gain = 250 V/V Typical
  - Input Noise = 0.75nV/√Hz max
  - Head Inductance Range = 0.2 - 10 µH
  - Write Current Range 10 - 40 mA
  - Input Capacitance = 23 pF max
- Very Low Power Dissipation = 7.5 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Write Unsafe Detection
- VM7230 - Schottky Isolated 400 Ω Damping Resistor
- VM7230N - No Internal Damping Resistor
- Socket Compatible with 2030 Preamp
- Available in 2, 4, 6 or 8-Channel Options

DESCRIPTION

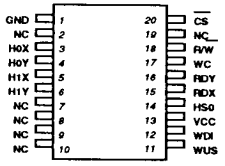
The VM7230 is a high-performance, very low-power read/write preamplifier designed for use with external thin-film recording heads. This circuit will operate on a single 5-volt power supply and is ideally suited for use in battery powered disk drives.

The VM7230 is plug compatible with parts using a 1:1 write current gain, while at the same time preserving the head voltage swing/switching speed advantage of VTC's VM7200.

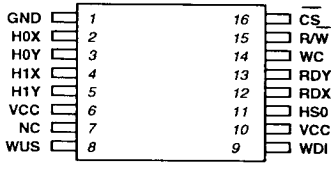
The VM7230 provides write current and data protection circuitry, and low noise read functions for up to eight read/write heads. When deactivated, the device enters a ***sleep mode*** which reduces power dissipation to 7.5 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

The VM7230/VM7230N is available in several different packages. Please consult VTC for package availability.

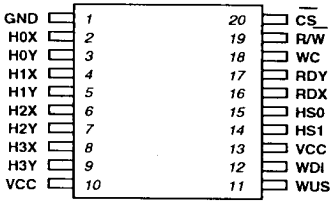
CONNECTION DIAGRAMS



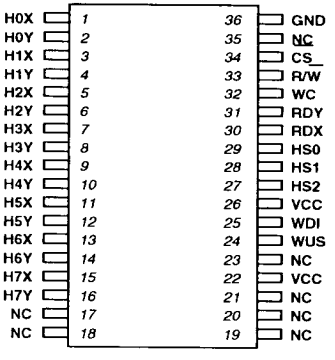
2-Channel
20-lead SSOP



2-Channel
16-lead SOIC

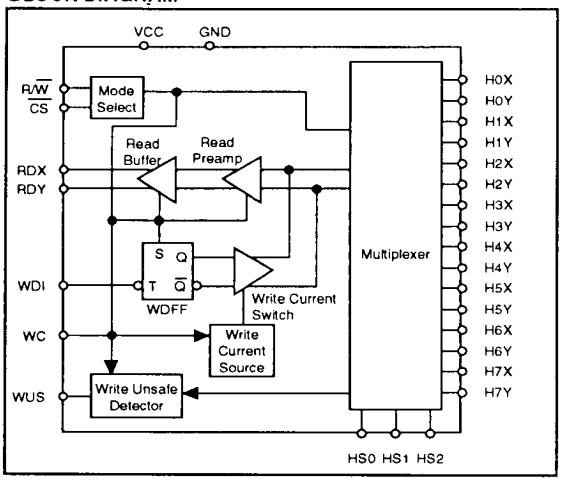


4-Channel
20-lead SOIC, SSOP



8-Channel
36-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 16-lead SOIC ..... 100°C/W
- 20-lead SOIC ..... 80°C/W
- 20-lead SSOP .....TBD
- 28-lead SOIC ..... 75°C/W
- 36-lead SOIC ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

Write current (I_W) ..... 10 to 40mA

Head Inductance (L_H) ..... 0.2 to 10µH

Junction Temperature (T_J) ..... 25°C to 125°C

CIRCUIT OPERATION

The VM7230 addresses up to eight 2-terminal, thin-film recording heads, providing switched write current in the write mode, or data amplification in the read mode. Head selection and mode control is determined by the head select lines, HS1, HS2 and mode control lines, $\overline{CS}$, R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups, provided on the $\overline{CS}$ and R/$\overline{W}$ lines, will force the device into a non-write condition if either control line opens up. The part's operation over a wide range of inductive loads makes it suitable for non-thin-film two-terminal heads also.

Write Mode

In write mode, the VM7230 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the Write Data Flip-Flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (R_{WC}) connected between the WC pin and Ground. An internally generated reference voltage is present at the WC pin. The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} = 1.25/R_{WC}$$

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally, the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- No write current
- WDI frequency too low
- Read or sleep mode
- Open head detect

Read Mode

In read mode, the VM7230 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the Pulse Detector circuit connected to these outputs.

Sleep Mode

When $\overline{CS}$ is high, initially all circuitry is shut down so that power dissipation is reduced to 7.5 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low "wakes up" the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Diode Connected Damping Resistor (patent pending)

The VM7230 has damping resistors isolated by Schottky diodes. The diodes effectively remove the resistor from the circuit during the read mode, however during the write mode with the higher level input signal, the resistor provides damping for the write current waveform. The VM7230N version has the damping network removed.

Input Structure:

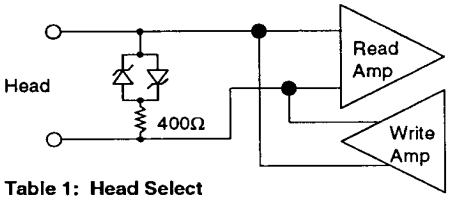


Table 1: Head Select

HS2	HS1	HS0	Head
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write/Awake
0	1	Read/Awake
1	X	Sleep

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0-HS2	I*	Head Select: selects one of up to 8 heads
H0X-H7X H0Y-H7Y	I/O	X, Y Head terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write select: High level selects read mode, low-level selects write mode
WUS	O*	Write unsafe: Open collector output: high level indicates writes unsafe condition
WC		Write current adjust: A resistor adjusts level of write current
RDX-RDY	O*	Read data output: differential output data
VCC		+5 volt supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Recommended operating conditions apply unless otherwise specified.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Supply Current	I_{CC}	Read Mode		33 + I_W/4	42 + I_W/4	mA
		Write Mode		42 + 1.25 I_W	50 + 1.25 I_W	
		Idle Mode		1.5	3	
Power Dissipation	PD	Read Mode		210	255	mW
		Write Mode, I_W = 20mA		370	415	
		Idle Mode		7.5	17	
Input High Voltage	V_{IH}		2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V			80	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V	-160			µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.35	0.5	V
WUS Output High Current	I_{OH}	V_{OH} = 5.0V		13	100	µA
VCC Value for Write Current Turn Off		I_{IH} < 0.2mA	3.7	4.0	4.3	V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	210	255	290	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p	25	40		MHz
		-3db |Zs| < 5Ω, V_{IN} = 1mVp-p	35	60		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.56	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		19	23	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	380	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	3	6		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @5MHz	50	73		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{CC}	45	70		dB
Channel Separation	CS	Unselected channels driven with 20mVp-p @5MHz Selected Channels V_{IN} = 0mVp-p	45	60		dB
Output Offset Voltage	V_{OS}		-300	25	+300	mV
RDX,RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC}-2.3		V
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-250	120	250	mV
Single-Ended Output Resistance	R_{SEO}			36	50	Ω
Output Current	I_O	AC Coupled Load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

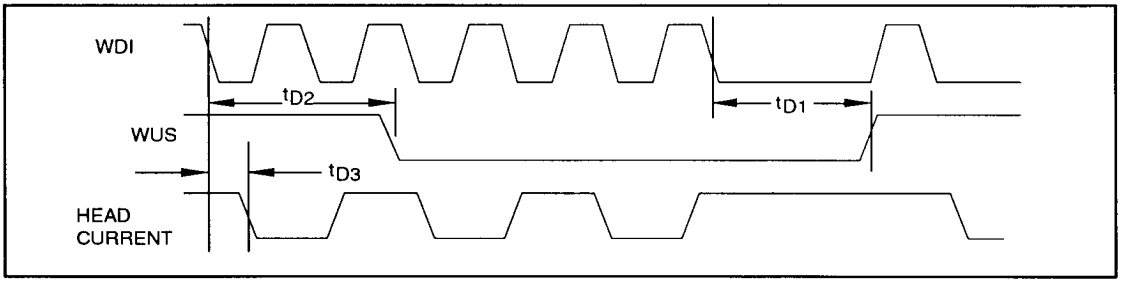


Figure 1: Write Mode Timing Diagram

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Write Current Constant	K_W		1.15	1.25	1.35	V
Write Current Range	I_W	31.2 < R_{WC} < 125Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8	0.5	+8	%
Differential Head Voltage Swing	V_{DH}	Open Head	4	5.2		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_O				25	pF
Differential Output Resistance	R_O		3200			Ω
Unselected Head Transient Current	I_{UH}	I_W = 20mA		0.15	1	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC}-2.3		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	SYM	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W			0.1	1.0	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10MHz read signal envelope			0.6	1.0	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope			0.27	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W			0.08	0.6	µs
HS0, 1 Any Head Delay	t_{HS}	HS0, 1 to 90% of 100mV, 10MHz read signal envelope			0.19	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}			0.6	2.2	3.6	µs
WUS Unsafe to Safe Delay	t_{D2}				0.1	1.0	µs
Head Current Propagation Delay (TD3)	t_{D3}	L_H = 0, R_H = 0, from 50% points			19	30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0			0.2	1	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points	L_H = 0, R_H = 0		5	8	ns
			L_H = 1µH, R_H = 30Ω		16	24	

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.