



STiH246

Advanced STB decoder with integrated dual silicon tuner and dual DVB-S2 demodulator

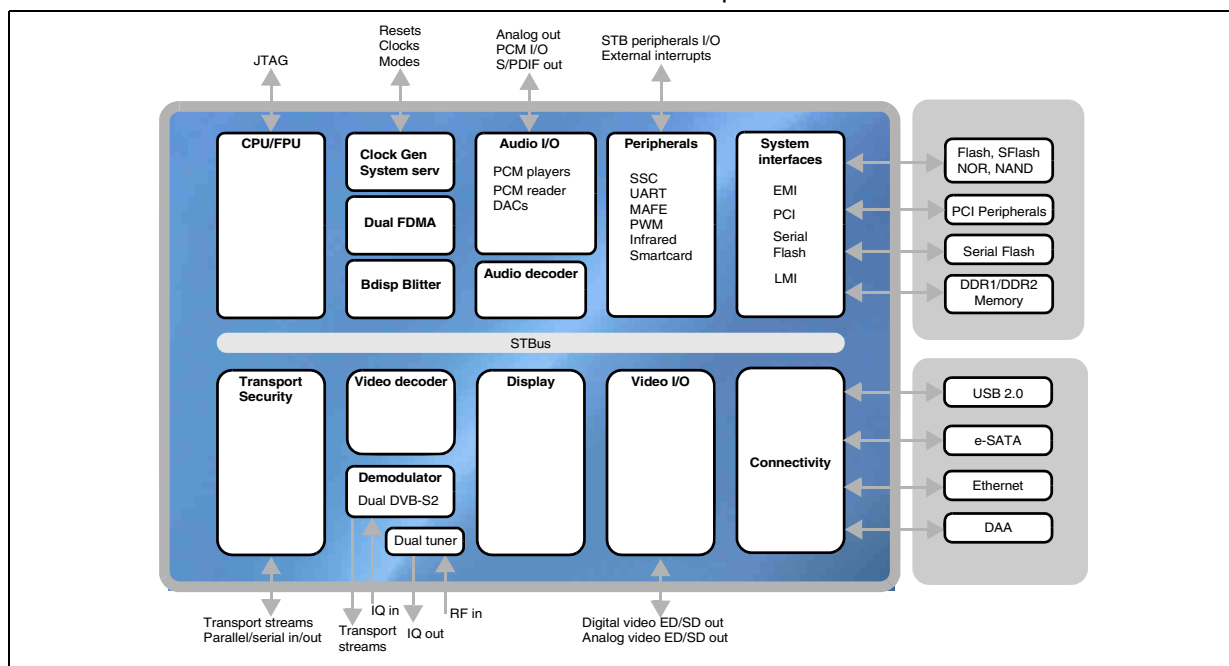
Data brief

Features

- Dual-channel silicon tuner, with 4 x 2 RF switch matrix
- Integrated dual DVB-S2 demodulator
- Dual multi-standard demodulation (DVB-S, DirecTV™ legacy and DVB-S2)
- Advanced high-definition video decoding (H264/VC-1/MPEG2)
- Advanced standard-definition video decoding (H264/VC-1/MPEG2/AVS)
- Advanced multi-channel audio decoding (MPEG 1, 2, MP 3, DD/DD+, AAC/AAC+, and WMA9/WMA9pro)
- Linux, Windows CE® and OS21 compatible ST40 applications CPU
- 16/32-bit DDR1/DDR2 compatible LMI
- Multi-stream, DVR capable transport stream processing
- Extensive connectivity (dual USB 2.0 hosts, e-SATA, Ethernet MAC/MII/RMII, and PCI)
- Advanced security and DRM support including SVP, VGS, MS-DRM, MSTV and DTCP-IP
- 2 DiSEqC™ 2 x 22 KHz interfaces
- Bit error rate monitoring and reporting
- 2 spare TS inputs (one can be output) for other demodulators or DVB-CI transport interface

Description

The STiH246 is a new, advanced decoding SoC targeted at next generation HD STBs. STiH246 is ideally suited to satellite, and hybrid (satellite + IP, terrestrial) networks. The STiH246 integrates in a single IC, dual tuner, dual DVB-S2 demodulator, multi-stream transport demux, an ST40 applications CPU, A/V decoding, video processing, graphics and display composition, advanced security, STB peripherals, A/V DACs, HDMI, digital A/V outputs, dual USB ports, e-SATA port and Ethernet MAC controller.



1 Introduction

The STiH246 uses state-of-the-art process technology to provide fully featured HD AVC decoder IC. It is a highly integrated system-on-chip suitable for STB markets across all networks (satellite/IP/terrestrial/x-DSL) worldwide.

The STiH246 is targeted at the latest Operator and CE manufacturer requirements for STBs which utilize advanced HD decoding (H264/VC-1/MPEG2), and which conform to DVB, ISMA, ATIS-IIF, SCTE, DirecTV, ATSC, ARIB, CEA, ITU, OpenCable and MSTV specifications.

The STiH246 provides a solution for operators to specify a range of low-cost, high-performance HD STBs including low-cost Zappers, IP clients, Interactive STBs, DVR standalone and DVR server/home network capable STBs, and with content delivery possible using broadcast or broadband networks, or both (hybrid STBs). The STiH246 keeps pace with the latest conditional access, DRM and trusted platform requirements of major operators worldwide by incorporating the latest generation of advanced security features. The STiH246 offers current users of STs growing family of advanced decoding ICs enhancements in performance and features whilst reducing cost and time-to-market for the next generation deployments.

Features	Benefits
Combines a dual tuner and dual DVB-S2 demodulator with STB decoding and display functions	This highly integrated SoC helps to reduce board area and manufacturing cost, allowing low-cost and small-size STBs to be designed for DVB-S2 networks
Serial Flash-based secure boot and code storage; 35 mm x 35 mm x 2.30 mm PBGA package	Enables further BOM optimization and cost reduction of advanced decoding SD STBs
ST40 applications CPU; 32 K I cache, 32 K D cache	Superscalar performance from a single CPU core, using standard tools and operating systems (Linux, Windows CE, OS21)
Supports 3D side-by-side and 3D effect user interface	Decoding of advanced standard definition MPEG2, H264 and VC-1/WMV9 streams, with the performance and flexibility for web-based content decoding such as Flash, DivX, MJPEG, XviD and Real
Advanced 2D graphics and display subsystem, and 1080p display output	Allows visually appealing user interfaces and video-rich navigation to be offered to consumers, while high-quality progressive output can be watched on the latest displays
Dual USB 2.0 hosts, Ethernet MAC with MII/RMII and TMII, SD-MMC/SDIO	Extensive high-speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, home network controllers (for example MoCA, Wi-Fi), memory cards
Low power process, design and architecture	Best in class, low-power standby mode, to meet emerging energy standards for STBs. Dynamic configuration of power to individual subsystems enables power-efficient active standby modes

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
28-Jul-2011	1	Initial release.

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