20 V, 4 A, Synchronous, Step-Down DC-to-DC Regulator

Data Sheet

ADP2384

FEATURES

- Input voltage: 4.5 V to 20 V
- Integrated MOSFET: 44 mΩ/11.6 mΩ
- Reference voltage: 0.6 V ± 1%
- Continuous output current: 4 A
- Programmable switching frequency: 200 kHz to 1.4 MHz
- Synchronizes to external clock: 200 kHz to 1.4 MHz
- 180° out-of-phase clock synchronization
- Precision enable and power good
- External compensation
- Internal soft start with external adjustable option
- Startup into a precharged output
- Supported by ADIsimPower design tool

APPLICATIONS

- Communications infrastructure
- Networking and servers
- Industrial and instrumentation
- Healthcare and medical
- Intermediate power rail conversion
- DC-to-dc point-of-load applications

TYPICAL APPLICATIONS CIRCUIT

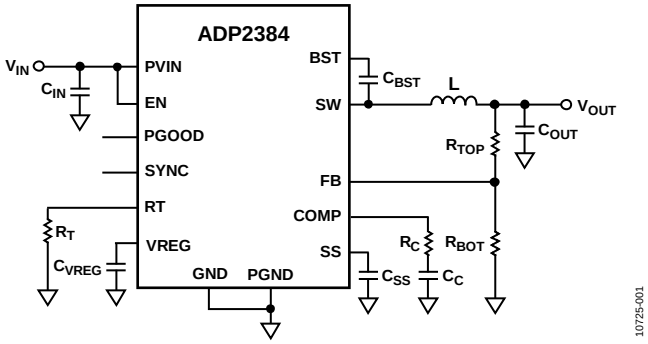

Figure 1.

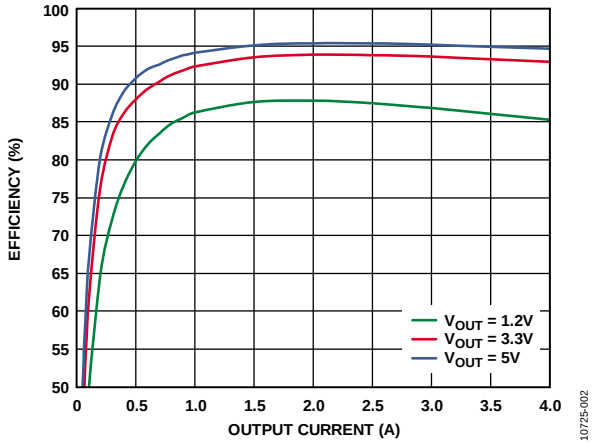

Figure 2. Efficiency vs. Output Current, V_{IN} = 12 V, f_{SW} = 300 kHz

GENERAL DESCRIPTION

The ADP2384 is a synchronous, step-down dc-to-dc regulator with an integrated 44 mΩ, high-side power MOSFET and an 11.6 mΩ, synchronous rectifier MOSFET to provide a high efficiency solution in a compact 4 mm × 4 mm LFCSP package. This device uses a peak current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response. The switching frequency of the ADP2384 can be programmed from 200 kHz to 1.4 MHz. To minimize system noise, the synchronization function allows the switching frequency to be synchronized to an external clock.

The ADP2384 requires minimal external components and operates from an input voltage of 4.5 V to 20 V. The output voltage can be adjusted from 0.6 V to 90% of the input voltage and delivers up to 4 A of continuous current. Each IC draws less than 120 µA current from the input source when it is disabled.

This regulator targets high performance applications that require high efficiency and design flexibility. External compensation and an adjustable soft start function provide design flexibility. The power-good output and precision enable input provide simple and reliable power sequencing.

Other key features include undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP), short-circuit protection (SCP), and thermal shutdown (TSD).

The ADP2384 operates over the −40°C to +125°C junction temperature range and is available in a 24-lead, 4 mm × 4 mm LFCSP package.

Rev. 0

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REVISION HISTORY

8/12—Revision 0: Initial Version

SPECIFICATIONS

V_{PVIN} = 12 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PVIN						
PVIN Voltage Range	V_{PVIN}		4.5		20	V
Quiescent Current	I_Q	No switching	2.1	2.9	3.6	mA
Shutdown Current	I_{SHDN}	EN = GND	45	80	120	µA
PVIN Undervoltage Lockout Threshold	UVLO	PVIN rising		4.3	4.5	V
		PVIN falling	3.5	3.8		V
FB						
FB Regulation Voltage	V_{FB}	0°C < T_J < 85°C	0.594	0.6	0.606	V
		−40°C < T_J < 125°C	0.591	0.6	0.609	V
FB Bias Current	I_{FB}			0.01	0.1	µA
ERROR AMPLIFIER (EA)						
Transconductance	g_m		340	470	600	µS
EA Source Current	I_{SOURCE}		40	60	80	µA
EA Sink Current	I_{SINK}		40	60	80	µA
INTERNAL REGULATOR (VREG)						
VREG Voltage	V_{VREG}	V_{PVIN} = 12 V, I_{VREG} = 50 mA	7.6	8	8.4	V
Dropout Voltage		V_{PVIN} = 12 V, I_{VREG} = 50 mA		340		mV
Regulator Current Limit			65	100	135	mA
SW						
High-Side On Resistance[1]		$V_{BST} - V_{SW}$ = 5 V		44	70	mΩ
Low-Side On Resistance[1]		V_{VREG} = 8 V		11.6	20	mΩ
High-Side Peak Current Limit			4.8	6.1	7.4	A
Low-Side Negative Current-Limit Threshold Voltage[2]				20		mV
SW Minimum On Time	t_{MIN_ON}			125	168	ns
SW Minimum Off Time	t_{MIN_OFF}			200	260	ns
BST						
Bootstrap Voltage	V_{BOOT}		4.5	5	5.5	V
OSCILLATOR (RT PIN)						
Switching Frequency	f_{SW}	R_T = 100 kΩ	530	600	670	kHz
Switching Frequency Range	f_{SW}		200		1400	kHz
SYNC						
Synchronization Range			200		1400	kHz
SYNC Minimum Pulse Width			100			ns
SYNC Minimum Off Time			100			ns
SYNC Input High Voltage			1.3			V
SYNC Input Low Voltage					0.4	V
SS						
Internal Soft Start				1600		Clock cycles
SS Pin Pull-Up Current	I_{SS_UP}		2.5	3.2	3.9	µA
PGOOD						
Power-Good Range						
FB Rising Threshold		PGOOD from low to high		95		%
FB Rising Hysteresis		PGOOD from high to low		5		%
FB Falling Threshold		PGOOD from low to high		105		%
FB Falling Hysteresis		PGOOD from high to low		11.7		%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Power-Good Deglitch Time		PGOOD from low to high		1024		Clock cycle
		PGOOD from high to low		16		Clock cycle
Power-Good Leakage Current		V_{PGOOD} = 5 V		0.01	0.1	µA
Power-Good Output Low Voltage		I_{PGOOD} = 1 mA		125	200	mV
EN						
EN Rising Threshold				1.17	1.28	V
EN Falling Threshold			0.97	1.07		V
EN Source Current		EN voltage below falling threshold		5		µA
		EN voltage above rising threshold		1		µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				25		°C

[1] Pin-to-pin measurement.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN, EN, PGOOD	−0.3 V to +22 V
SW	−1 V to +22 V
BST	V_{SW} + 6 V
FB, SS, COMP, SYNC, RT	−0.3 V to +6 V
VREG	−0.3 V to +12 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a 4-layer, JEDEC standard circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
24-Lead LFCSP_WQ	42.6	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

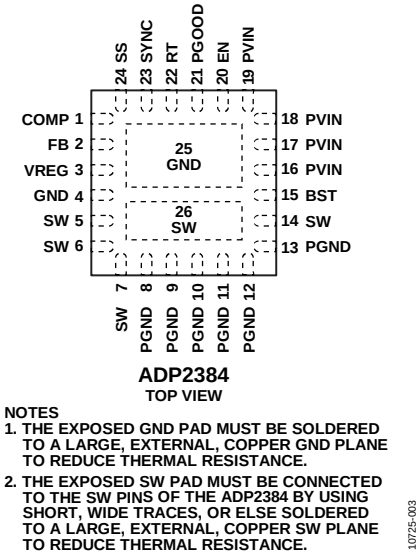

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	Error Amplifier Output. Connect an RC network from COMP to GND.
2	FB	Feedback Voltage Sense Input. Connect to a resistor divider from the output voltage, V_{OUT}.
3	VREG	Output of the Internal 8 V Regulator. The control circuits are powered from this voltage. Place a 1 µF, X7R or X5R ceramic capacitor between this pin and GND.
4	GND	Analog Ground. Return of internal control circuit.
5, 6, 7, 14	SW	Switch Node Output. Connect to the output inductor.
8, 9, 10, 11, 12, 13	PGND	Power Ground. Return of low-side power MOSFET.
15	BST	Supply Rail for the High-Side Gate Drive. Place a 0.1 µF, X7R or X5R capacitor between SW and BST.
16,17,18,19	PVIN	Power Input. Connect to the input power source and connect a bypass capacitor between this pin and PGND.
20	EN	Precision Enable Pin. An external resistor divider can be used to set the turn-on threshold. To enable the part automatically, connect the EN pin to the PVIN pin.
21	PGOOD	Power-Good Output (Open Drain). A pull-up resistor of 10 kΩ to 100 kΩ is recommended.
22	RT	Frequency Setting. Connect a resistor between RT and GND to program the switching frequency from 200 kHz to 1.4 MHz.
23	SYNC	Synchronization Input. Connect this pin to an external clock to synchronize the switching frequency from 200 kHz and 1.4 MHz. See the Oscillator section and Synchronization section for more information.
24	SS	Soft Start Control. Connect a capacitor from SS to GND to program the soft start time. If this pin is open, the regulator uses the internal soft start time.
25	EP, GND	The exposed GND pad must be soldered to a large, external, copper GND plane to reduce thermal resistance.
26	EP, SW	The exposed SW pad must be connected to the SW pins of the ADP2384, using short, wide traces, or else soldered to a large, external, copper SW plane to reduce thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 3.3 µH, C_{OUT} = 47 µF × 2, f_{SW} = 600 kHz, unless otherwise noted.

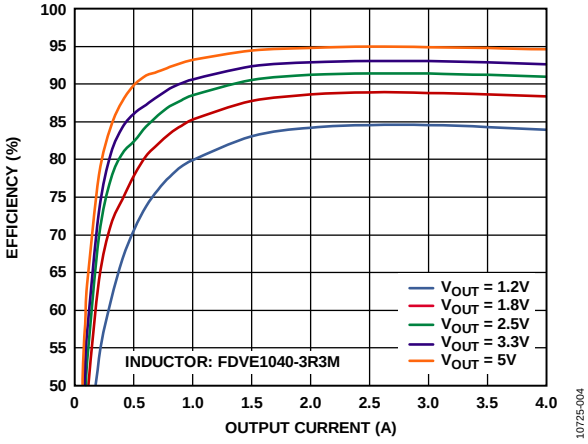

Figure 4. Efficiency at V_{IN} = 12 V, f_{SW} = 600 kHz

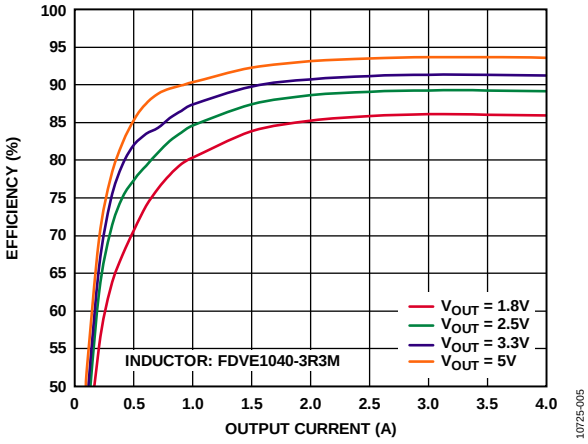

Figure 5. Efficiency at V_{IN} = 18 V, f_{SW} = 600 kHz

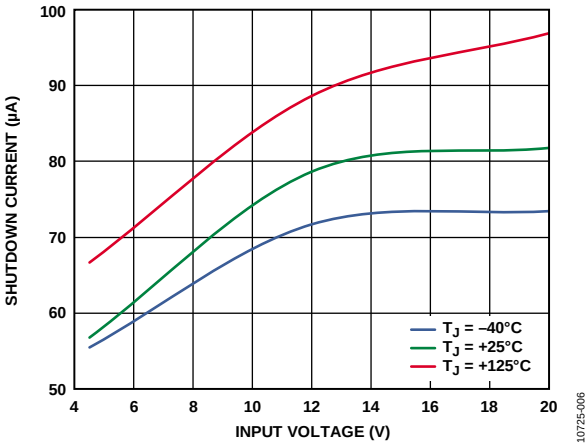

Figure 6. Shutdown Current vs. V_{IN}

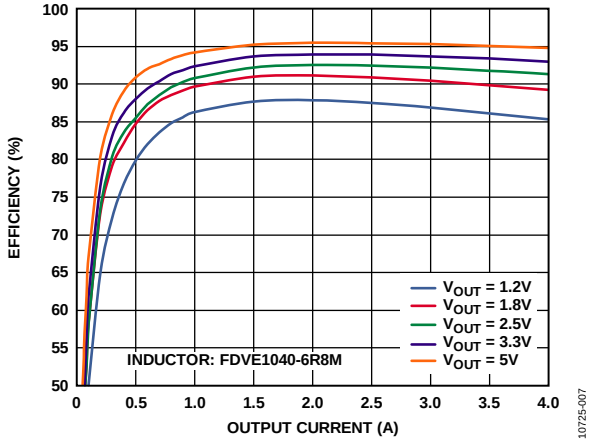

Figure 7. Efficiency at V_{IN} = 12 V, f_{SW} = 300 kHz

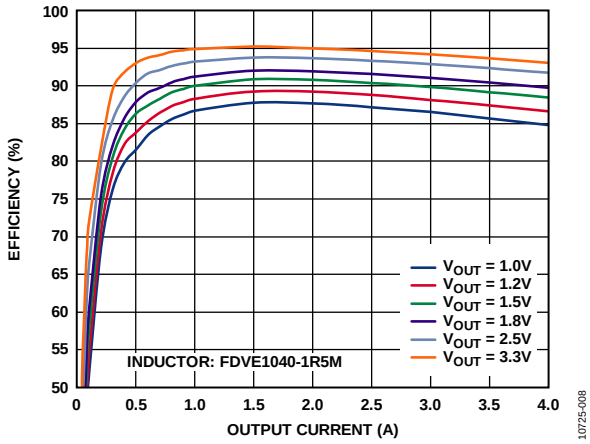

Figure 8. Efficiency at V_{IN} = 5 V, f_{SW} = 600 kHz

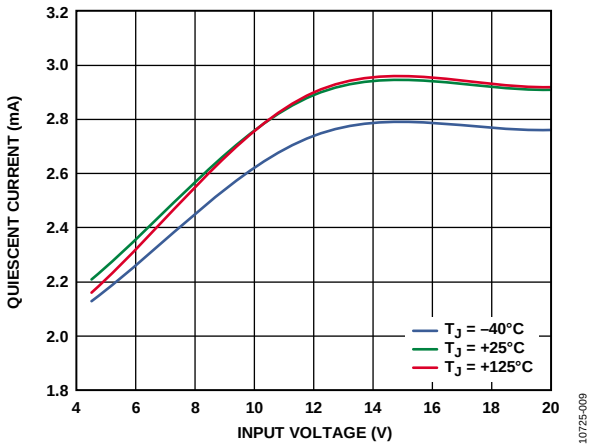

Figure 9. Quiescent Current vs. V_{IN}

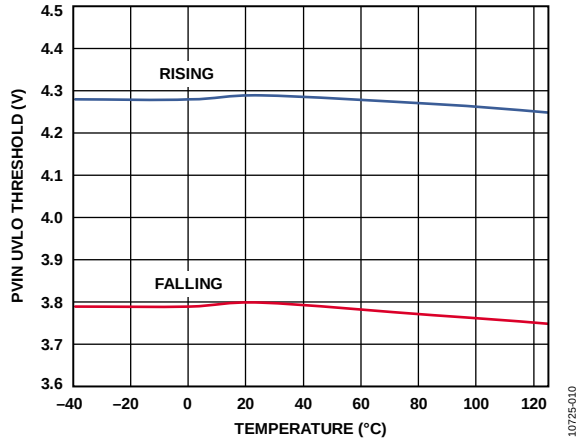

Figure 10. UVLO Threshold vs. Temperature

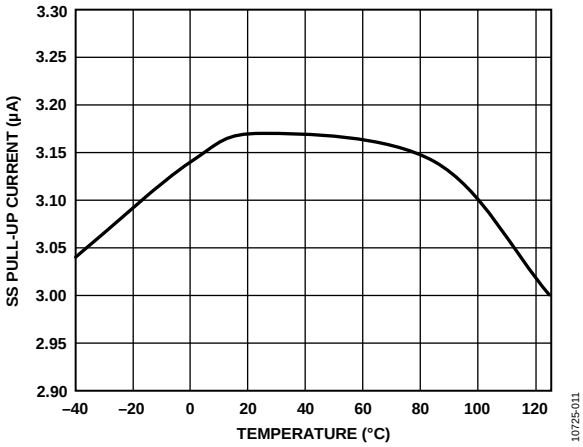

Figure 11. SS Pin Pull-Up Current vs. Temperature

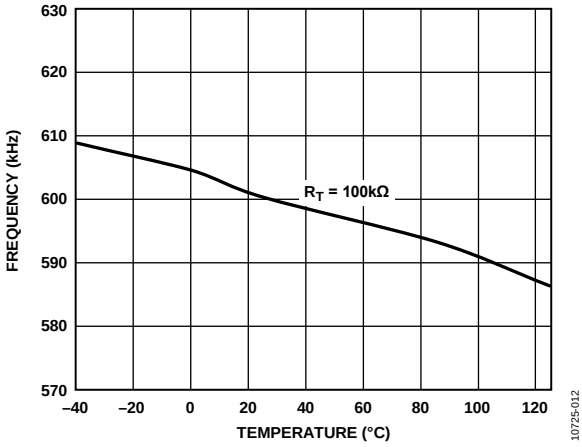

Figure 12. Frequency vs. Temperature

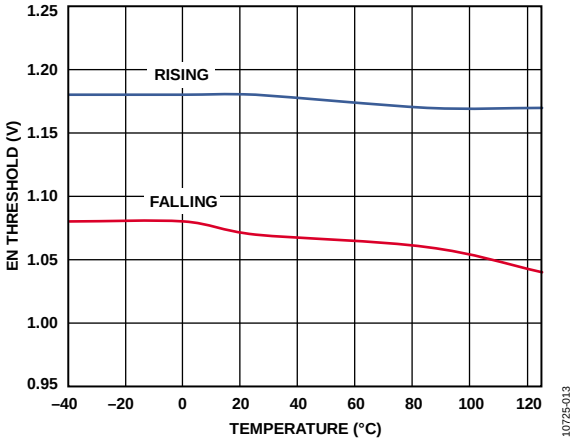

Figure 13. EN Threshold vs. Temperature

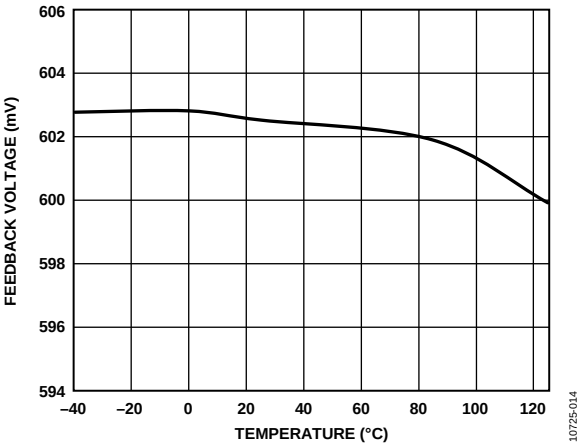

Figure 14. FB Voltage vs. Temperature

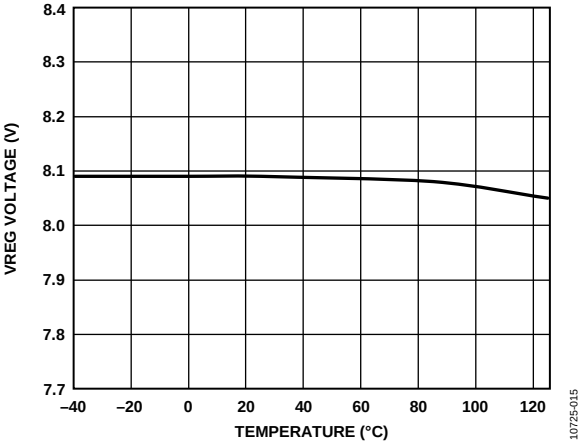

Figure 15. VREG Voltage vs. Temperature

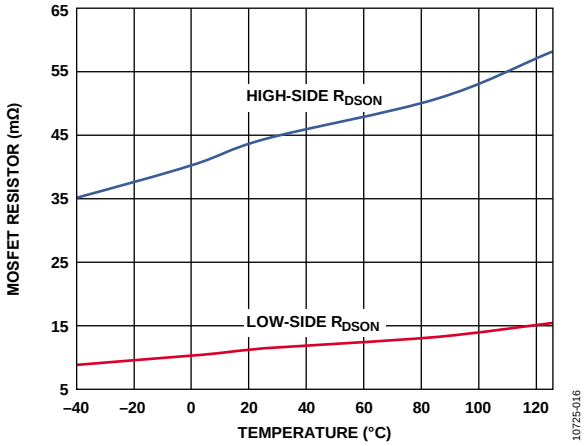

Figure 16. MOSFET R_{DSON} vs. Temperature

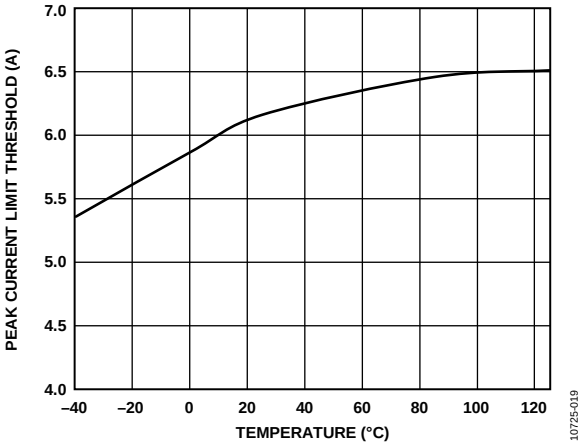

Figure 19. Current-Limit Threshold vs. Temperature

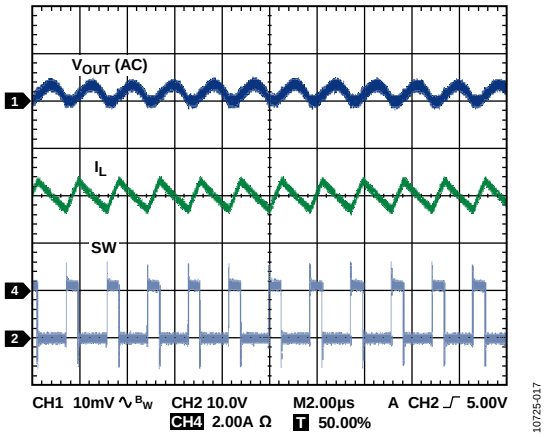

Figure 17. Working Mode Waveform

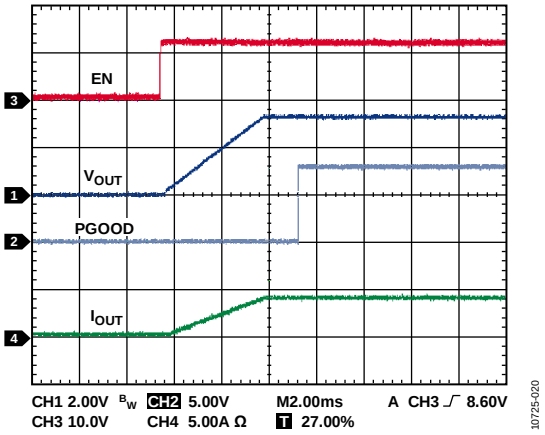

Figure 20. Soft Start with Full Load

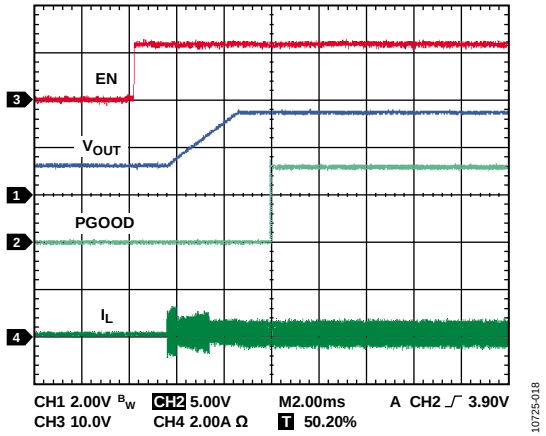

Figure 18. Voltage Precharged Output

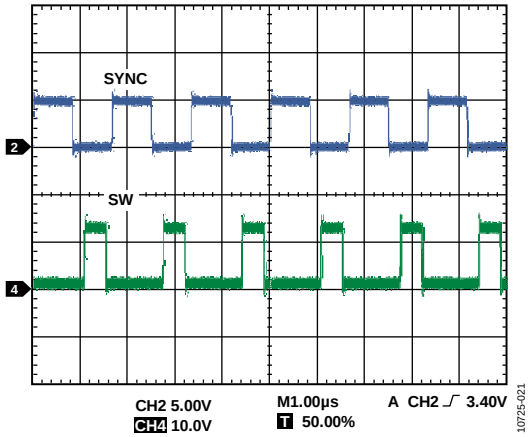

Figure 21. External Synchronization

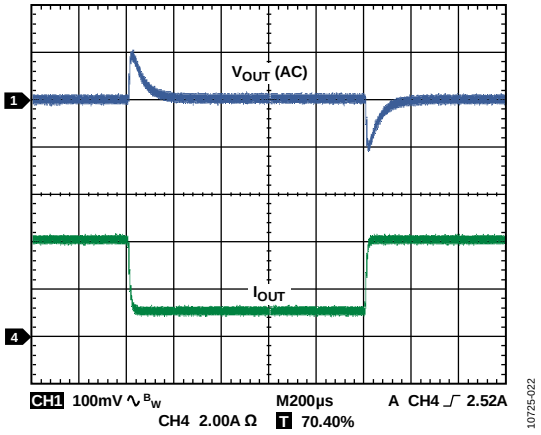

Figure 22. Load Transient Response, 1 A to 4 A

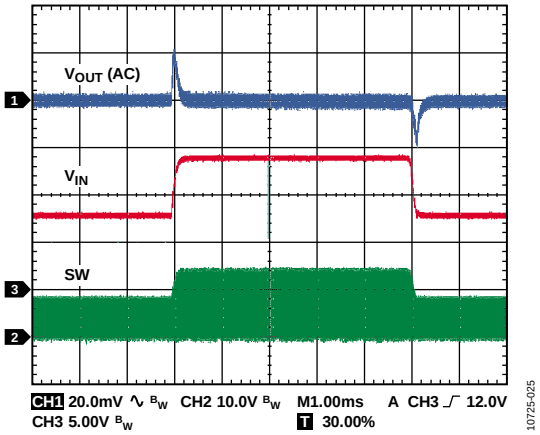

Figure 25. Line Transient Response, V_{IN} from 8 V to 14 V, I_{OUT} = 4 A

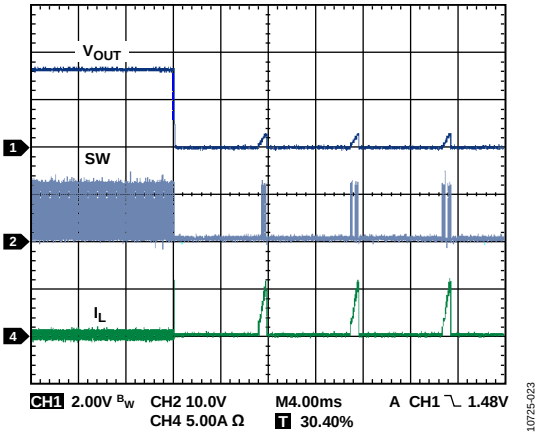

Figure 23. Output Short Entry

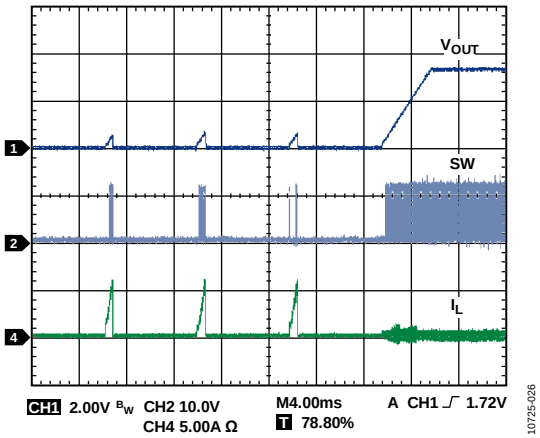

Figure 26. Output Short Recovery

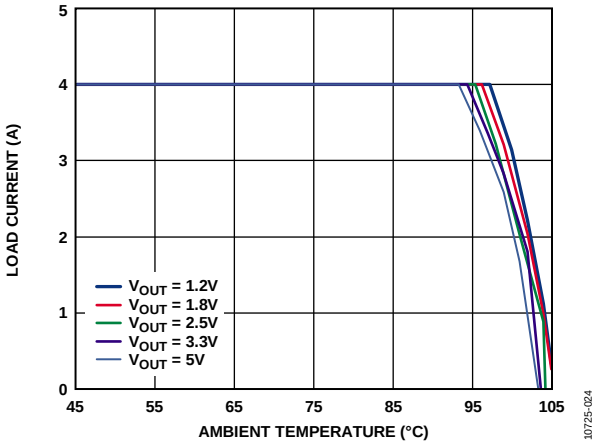

Figure 24. Output Current vs. Ambient Temperature at V_{IN} = 12 V, f_{SW} = 600 kHz

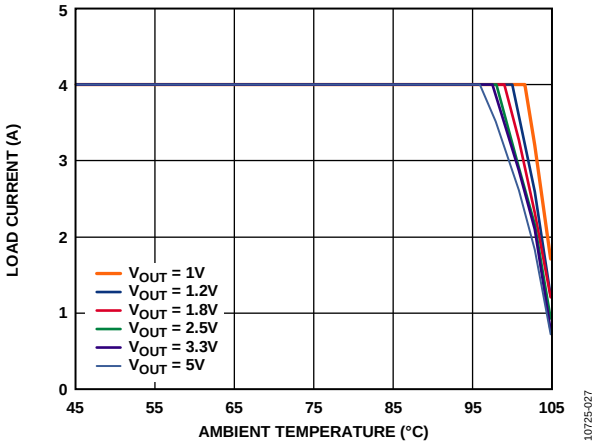

Figure 27. Output Current vs. Ambient Temperature at V_{IN} = 12 V, f_{SW} = 300 kHz

FUNCTIONAL BLOCK DIAGRAM

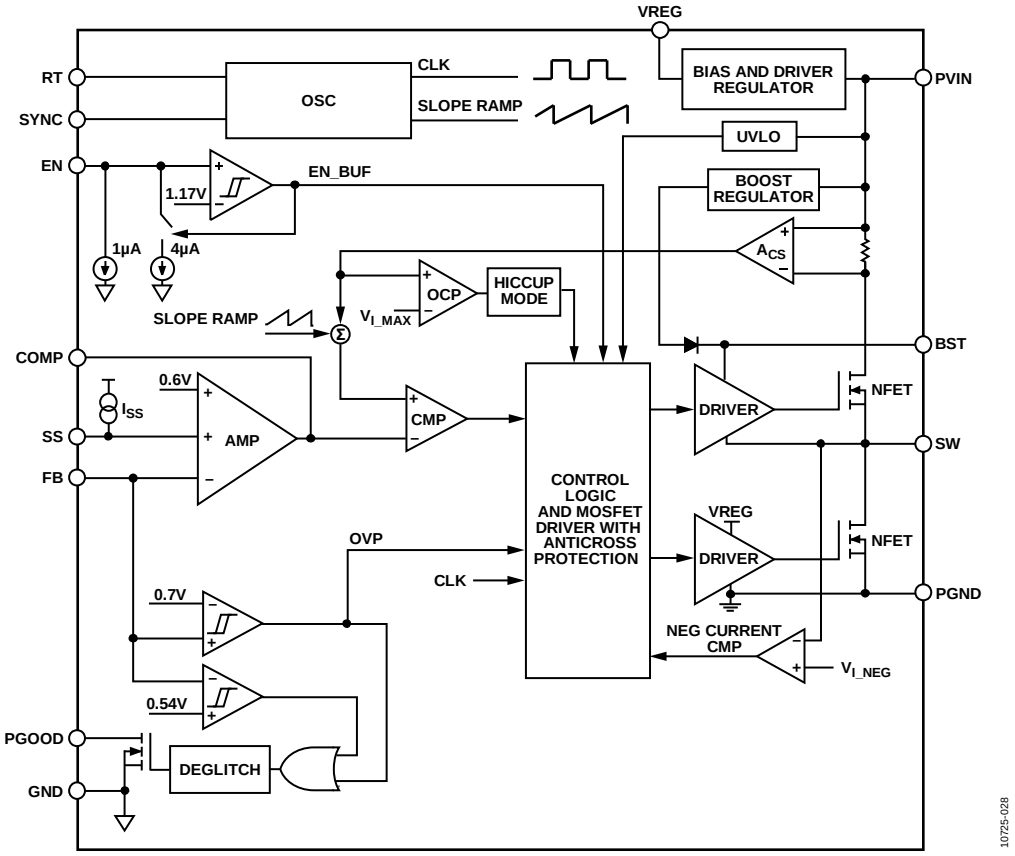

Figure 28. Functional Block Diagram

THEORY OF OPERATION

The ADP2384 is a synchronous step-down, dc-to-dc regulator that uses a current mode architecture with an integrated high-side power switch and a low-side synchronous rectifier. The regulator targets high performance applications that require high efficiency and design flexibility.

The ADP2384 operates from an input voltage that ranges from 4.5 V to 20 V and regulates the output voltage from 0.6 V to 90% of the input voltage. Additional features that maximize design flexibility include the following: programmable switching frequency, programmable soft start, external compensation, precision enable, and a power-good output.

CONTROL SCHEME

The ADP2384 uses a fixed frequency, peak current mode PWM control architecture. At the start of each oscillator cycle, the high-side N-MOSFET is turned on, putting a positive voltage across the inductor. When the inductor current crosses the peak inductor current threshold, the high-side N-MOSFET is turned off and the low-side N-MOSFET is turned on. This puts a negative voltage across the inductor, causing the inductor current to decrease. The low-side N-MOSFET stays on for the rest of the cycle (see Figure 17).

PRECISION ENABLE/SHUTDOWN

The EN input pin has a precision analog threshold of 1.17 V (typical) with 100 mV of hysteresis. When the enable voltage exceeds 1.17 V, the regulator turns on; when it falls below 1.07 V (typical), the regulator turns off. To force the regulator to automatically start when input power is applied, connect EN to PVIN.

The precision EN pin has an internal pull-down current source (5 µA) that provides a default turn-off when the EN pin is open.

When the EN pin voltage exceeds 1.17 V (typical), the ADP2384 is enabled and the internal pull-down current source at the EN pin decreases to 1 µA, which allows users to program the PVIN UVLO and hysteresis.

INTERNAL REGULATOR (VREG)

The on-board regulator provides a stable supply for the internal circuits. It is recommended that a 1 µF ceramic capacitor be placed between the VREG pin and GND. The internal regulator includes a current-limit circuit to protect the output if the maximum external load current is exceeded.

BOOTSTRAP CIRCUITRY

The ADP2384 includes a regulator to provide the gate drive voltage for the high-side N-MOSFET. It uses differential sensing to generate a 5 V bootstrap voltage between the BST and SW pins.

It is recommended that a 0.1 µF, X7R or X5R ceramic capacitor be placed between the BST pin and the SW pin.

OSCILLATOR

The ADP2384 switching frequency is controlled by the RT pin. A resistor from RT to GND can program the switching frequency according to the following equation:

$$f_{SW}\,(\text{kHz}) = \frac{69{,}120}{R_T\,(\text{k}\Omega) + 15}$$

A 100 kΩ resistor sets the frequency to 600 kHz, and a 42.2 kΩ resistor sets the frequency to 1.2 MHz. Figure 29 shows the typical relationship between f_{SW} and R_T.

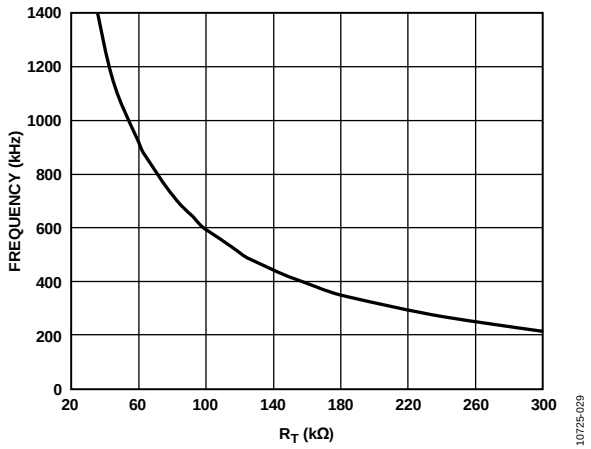

Figure 29. Switching Frequency vs. R_T

SYNCHRONIZATION

To synchronize the ADP2384, connect an external clock to the SYNC pin. The frequency of the external clock can be in the range of 200 kHz to 1.4 MHz. During synchronization, the regulator operates in continuous conduction mode (CCM), and the rising edge of the switching waveform runs 180° out of phase to the rising edge of the external clock.

When the ADP2384 operates in synchronization mode, a resistor must be connected from the RT pin to GND to program the internal oscillator to run at 90% to 110% of the external synchronization clock.

SOFT START

The ADP2384 has integrated soft start circuitry to limit the output voltage rising time and reduce inrush current at startup. The internal soft start time is calculated using the following equation:

$$t_{SS\_INT} = \frac{1600}{f_{SW}\ (\text{kHz})}\ (\text{ms})$$

A slower soft start time can be programmed by using the SS pin. When a capacitor is connected between the SS pin and GND, an internal current charges the capacitor to establish the soft start ramp. The soft start time is calculated using the following equation:

$$t_{SS\_EXT} = \frac{0.6\ \text{V} \times C_{SS}}{I_{SS\_UP}}$$

where:
C_{SS} is the soft start capacitance.
I_{SS_UP} is the soft start pull-up current (3.2 µA).

The internal error amplifier includes three positive inputs: the internal reference voltage, the internal digital soft start voltage, and the SS pin voltage. The error amplifier regulates the FB voltage to the lowest of the three voltages.

If the output voltage is charged prior to turn-on, the ADP2384 prevents reverse inductor current that would discharge the output capacitor. This function remains active until the soft start voltage exceeds the voltage on the FB pin.

POWER GOOD

The power-good pin (PGOOD) is an active high, open-drain output that requires an external resistor to pull it up to a voltage. A logic high on the PGOOD pin indicates that the voltage on the FB pin (and, therefore, the output voltage) is within regulation.

The power-good circuitry monitors the output voltage on the FB pin and compares it to the rising and falling thresholds that are specified in Table 1. If the rising output voltage exceeds the target value, the PGOOD pin is held low. The PGOOD pin continues to be held low until the falling output voltage returns to the target value.

If the output voltage falls below the target output voltage, the PGOOD pin is held low. The PGOOD pin continues to be held low until the rising output voltage returns to the target value.

The power-good rising and falling thresholds are shown in Figure 30. There is a 1024-cycle waiting period before the PGOOD pin is pulled from low to high, and there is a 16-cycle waiting period before the PGOOD pin is pulled from high to low.

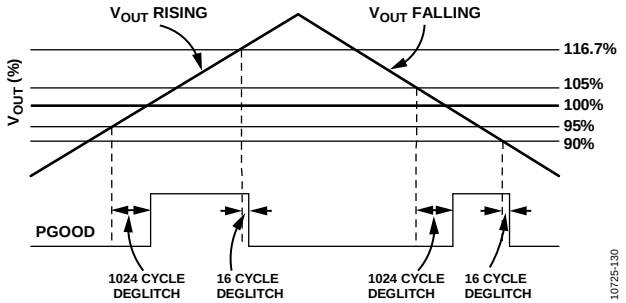

Figure 30. PGOOD Rising and Falling Thresholds

PEAK CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2384 has a peak current-limit protection circuit to prevent current runaway. During the initial soft start, the ADP2384 uses frequency foldback to prevent output current runaway. The switching frequency is reduced according to the voltage on the FB pin, which allows more time for the inductor to discharge. The correlation between the switching frequency and the FB pin voltage is shown in Table 5.

Table 5. FB Pin Voltage and Switching Frequency

FB Pin Voltage	Switching Frequency
$V_{FB} \geq 0.4$ V	f_{SW}
$0.4\ \text{V} > V_{FB} \geq 0.2$ V	$f_{SW}/2$
$V_{FB} < 0.2$ V	$f_{SW}/4$

For protection against heavy loads, the ADP2384 uses a hiccup mode for overcurrent protection. When the inductor peak current reaches the current-limit value, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle. The overcurrent counter increments during this process. If the overcurrent counter reaches 10 or the FB pin voltage falls to 0.4 V after the soft start, the regulator enters hiccup mode. The high-side and low-side MOSFETs are both turned off. The regulator remains in hiccup mode for 4096 clock cycles and then attempts to restart. If the current-limit fault has cleared, the regulator resumes normal operation. Otherwise, it reenters hiccup mode.

The ADP2384 also provides a sink current limit to prevent the low-side MOSFET from sinking a lot of current from the load. When the voltage across the low-side MOSFET exceeds the sink current-limit threshold, which is typically 20 mV, the low-side MOSFET turns off immediately for the rest of the cycle. Both high-side and low-side MOSFETs turn off until the next clock cycle.

In some cases, the input voltage (V_{PVIN}) ramp rate is too slow or the output capacitor is too large for the output to reach regulation during the soft start process, which causes the regulator to enter the hiccup mode. To avoid such occurrences, use a resistor divider at the EN pin to program the input voltage UVLO, or use a longer soft start time.

OVERVOLTAGE PROTECTION (OVP)

The ADP2384 includes an overvoltage protection feature to protect the regulator against an output short to a higher voltage supply or when a strong load disconnect transient occurs. If the feedback voltage increases to 0.7 V, the internal high-side and low-side MOSFETs are turned off until the voltage at the FB pin decreases to 0.63 V. At that time, the ADP2384 resumes normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout circuitry is integrated in the ADP2384 to prevent the occurrence of power-on glitches. If the V_{PVIN} voltage falls below 3.8 V typical, the part shuts down and both the power switch and synchronous rectifier turn off. When the V_{PVIN} voltage rises above 4.3 V typical, the soft start period is initiated and the part is enabled.

THERMAL SHUTDOWN

If the ADP2384 junction temperatures rises above 150°C, the internal thermal shutdown circuit turns off the regulator for self-protection. Extreme junction temperatures can be the result of high current operation, poor circuit board thermal design, and/or high ambient temperature. A 25°C hysteresis is included in the thermal shutdown circuit so that, if an overtemperature event occurs, the ADP2384 does not return to normal operation until the on-chip temperature falls below 125°C. Upon recovery, a soft start is initiated before normal operation begins.

APPLICATIONS INFORMATION

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVIN. Place the input capacitor as close as possible to the PVIN pin. A ceramic capacitor in the 10 µF to 47 µF range is recommended. The loop that is composed of this input capacitor, the high-side N-MOSFET, and the low-side N-MOSFET must be kept as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor should be larger than the value calculated from the following equation:

$$I_{C_{IN\_RMS}} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

OUTPUT VOLTAGE SETTING

The output voltage of the ADP2384 is set by an external resistive divider. The resistor values are calculated using

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

To limit output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} < 30 kΩ.

Table 6 lists the recommended resistor divider values for various output voltages.

Table 6. Resistor Divider Values for Various Output Voltages

V_{OUT} (V)	R_{TOP} ± 1% (kΩ)	R_{BOT} ± 1% (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	47.5	15
3.3	10	2.21
5.0	22	3

VOLTAGE CONVERSION LIMITATIONS

The minimum output voltage for a given input voltage and switching frequency is constrained by the minimum on time. The minimum on time of the ADP2384 is typically 125 ns. The minimum output voltage for a given input voltage and switching frequency can be calculated using the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON_HS} is the high-side MOSFET on resistance.
R_{DSON_LS} is the low-side MOSFET on resistance.
I_{OUT_MIN} is the minimum output current.
R_L is the series resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is constrained by the minimum off time and the maximum duty cycle. The minimum off time is typically 200 ns, and the maximum duty cycle of the ADP2384 is typically 90%.

The maximum output voltage, limited by the minimum off time at a given input voltage and frequency, can be calculated using the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

The maximum output voltage, limited by the maximum duty cycle at a given input voltage, can be calculated by using the following equation:

$$V_{OUT\_MAX} = D_{MAX} \times V_{IN} \quad (3)$$

where D_{MAX} is the maximum duty cycle.

As shown in Equation 1 to Equation 3, reducing the switching frequency alleviates the minimum on time and minimum off time limitation.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor value leads to a faster transient response but degrades efficiency, due to a larger inductor ripple current; using a large inductor value leads to smaller ripple current and better efficiency but results in a slower transient response.

As a guideline, the inductor ripple current, ΔI_L, is typically set to one-third of the maximum load current. The inductor value is calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
ΔI_L is the inductor current ripple.
f_{SW} is the switching frequency.

The ADP2384 uses adaptive slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

For a duty cycle that is larger than 50%, the minimum inductor value is determined using the following equation:

$$L\ (Minimum) = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW}}$$

The peak inductor current is calculated by

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor should be higher than the current-limit threshold of the switch. This prevents the inductor from reaching saturation.

The rms current of the inductor is calculated as follows:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI. Table 7 lists some recommended inductors.

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects the output ripple voltage load step transient and the loop stability of the regulator.

For example, during a load step transient where the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current. The delay caused by the control loop causes output undershoot. The output capacitance that is required to satisfy the voltage droop requirement can be calculated using the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times {\Delta I_{STEP}}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor, with a typical setting of K_{UV} = 2.
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example occurs when a load is suddenly removed from the output, and the energy stored in the inductor rushes into the output capacitor, causing the output to overshoot.

The output capacitance that is required to meet the overshoot requirement can be calculated using the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times {\Delta I_{STEP}}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - {V_{OUT}}^2}$$

where:
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.
K_{OV} is a factor, with a typical setting of K_{OV} = 2.

The output ripple is determined by the ESR and the value of the capacitance. Use the following equation to select a capacitor that can meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where:
ΔV_{OUT_RIPPLE} is the allowable output ripple voltage.
R_{ESR} is the equivalent series resistance of the output capacitor in ohms (Ω).

Table 7. Recommended Inductors

Vendor	Part No.	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)
Toko	FDVE1040-1R5M	1.5	13.7	14.6	4.6
	FDVE1040-2R2M	2.2	11.4	11.6	6.8
	FDVE1040-3R3M	3.3	9.8	9.0	10.1
	FDVE1040-4R7M	4.7	8.2	8.0	13.8
	FDVE1040-6R8M	6.8	7.1	7.1	20.2
	FDVE1040-100M	10	6.1	5.2	34.1
Vishay	IHLP4040DZ-1R0M-01	1.0	36	17.5	4.1
	IHLP4040DZ-1R5M-01	1.5	27.5	15	5.8
	IHLP4040DZ-2R2M-01	2.2	25.6	12	9
	IHLP4040DZ-3R3M-01	3.3	18.6	10	14.4
	IHLP4040DZ-4R7M-01	4.7	17	9.5	16.5
	IHLP4040DZ-6R8M-01	6.8	13.5	8.0	23.3
	IHLP4040DZ-100M-01	10	12	6.8	36.5
Wurth Elektronik	744325120	1.2	25	20	1.8
	744325180	1.8	18	16	3.5
	744325240	2.4	17	14	4.75
	744325330	3.3	15	12	5.9
	744325420	4.2	14	11	7.1
	744325550	5.5	12	10	10.3

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple performance.

The selected output capacitor voltage rating should be greater than the output voltage. The rms current rating of the output capacitor must be larger than the value that is calculated by

$$I_{C_{OUT}\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

PROGRAMMING THE INPUT VOLTAGE UVLO

The ADP2384 has a precision enable input that can be used to program the UVLO threshold of the input voltage (see Figure 31).

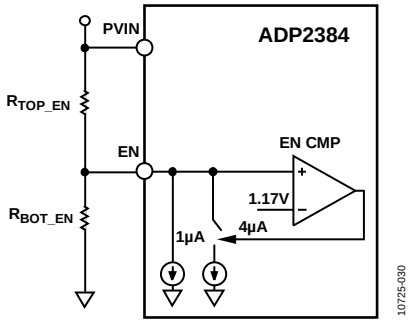

Figure 31. Programming the Input Voltage UVLO

Use the following equation to calculate R_{TOP_EN} and R_{BOT_EN}:

$$R_{TOP\_EN} = \frac{1.07\,V \times V_{IN\_RISING} - 1.17\,V \times V_{IN\_FALLING}}{1.07\,V \times 5\mu A - 1.17\,V \times 1\,\mu A}$$

$$R_{BOT\_EN} = \frac{1.17\,V \times R_{TOP\_EN}}{V_{IN\_RISING} - R_{TOP\_EN} \times 5\mu A - 1.17\,V}$$

where:

V_{IN_RISING} is the V_{IN} rising threshold.

$V_{IN\_FALLING}$ is the V_{IN} falling threshold.

COMPENSATION DESIGN

For peak current mode control, the power stage can be simplified as a voltage controlled current source supplying current to the output capacitor and load resistor. It is composed of one domain pole and a zero that is contributed by the output capacitor ESR. The control-to-output transfer function is based on the following:

$$G_{VD}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_Z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_P}\right)}$$

$$f_Z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_P = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:

A_{VI} = 8.7 A/V.

R is the load resistance.

C_{OUT} is the output capacitance.

R_{ESR} is the equivalent series resistance of the output capacitor.

The ADP2384 uses a transconductance amplifier for the error amplifier and to compensate the system. Figure 32 shows the simplified, peak current mode control, small signal circuit.

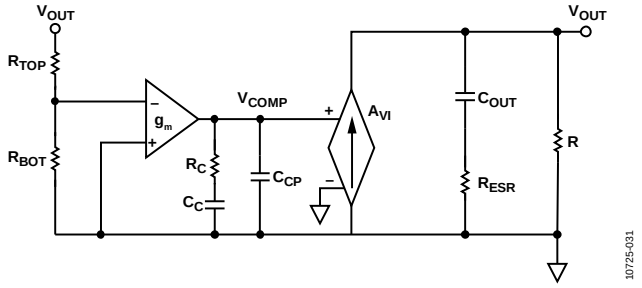

Figure 32. Simplified Peak Current Mode Control, Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero, and R_C and the optional C_{CP} contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{VD}(s)$$

The following design guideline shows how to select the R_C, C_C, and C_{CP} compensation components for ceramic output capacitor applications:

1. Determine the cross frequency, f_C. Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Calculate R_C using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.6\,V \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole, f_P; then determine C_C by using the following equation:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

ADIsimPower DESIGN TOOL

The ADP2384 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs that are optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and part count, while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about theADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can request an unpopulated board.

DESIGN EXAMPLE

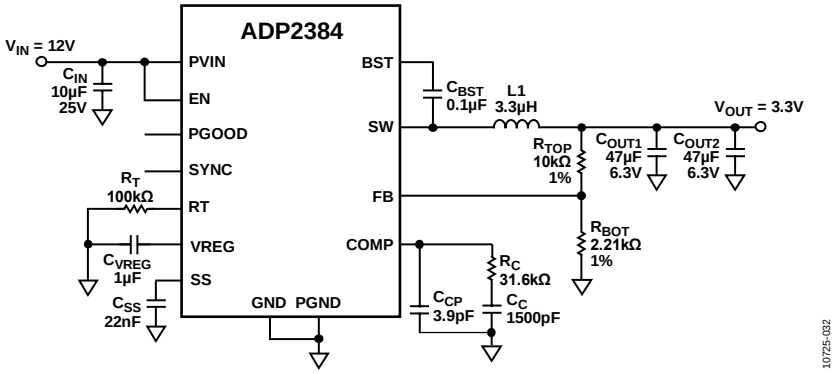

Figure 33. Schematic for Design Example

This section describes the procedures for selecting the external components, based on the example specifications that are listed in Table 8. See Figure 33 for the schematic of this design example.

Table 8. Step-Down DC-to-DC Regulator Requirements

Parameter	Specification
Input Voltage	V_{IN} = 12.0 V ± 10%
Output Voltage	V_{OUT} = 3.3 V
Output Current	I_{OUT} = 4 A
Output Voltage Ripple	ΔV_{OUT_RIPPLE} = 33 mV
Load Transient	±5%, 1 A to 4 A, 2 A/µs
Switching Frequency	f_{SW} = 600 kHz

OUTPUT VOLTAGE SETTING

Choose a 10 kΩ resistor as the top feedback resistor (R_{TOP}), and calculate the bottom feedback resistor (R_{BOT}) by using the following equation:

$$R_{BOT} = R_{TOP} \times \left(\frac{0.6}{V_{OUT} - 0.6} \right)$$

To set the output voltage to 3.3 V, the resistors values are as follows: R_{TOP} = 10 kΩ, and R_{BOT} = 2.21 kΩ.

FREQUENCY SETTING

Connect a 100 kΩ resistor from the RT pin to GND to set the switching frequency to 600 kHz.

INDUCTOR SELECTION

The peak-to-peak inductor ripple current, ΔI_L, is set to 30% of the maximum output current. Use the following equation to estimate the inductor value:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} = 12 V.
V_{OUT} = 3.3 V.
D = 0.275.
ΔI_L = 1.2 A.
f_{SW} = 600 kHz.

This calculation results in L = 3.323 µH. Choose the standard inductor value of 3.3 µH.

The peak-to-peak inductor ripple current can be calculated using the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

This calculation results in ΔI_L = 1.21 A.

Use the following equation to calculate the peak inductor current:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

This calculation results in I_{PEAK} = 4.605 A.

Use the following equation to calculate the rms current flowing through the inductor:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

This calculation results in I_{RMS} = 4.015 A.

Based on the calculated current value, select an inductor with a minimum rms current rating of 4.02 A and a minimum saturation current rating of 4.61 A.

However, to protect the inductor from reaching its saturation point under the current-limit condition, the inductor should be rated for at least a 6 A saturation current for reliable operation.

Based on the requirements described previously, select a 3.3 µH inductor, such as the FDVE1040-3R3M from Toko, which has a 10.1 mΩ DCR and a 9.8 A saturation current.

OUTPUT CAPACITOR SELECTION

The output capacitor is required to meet both the output voltage ripple and load transient response requirements.

To meet the output voltage ripple requirement, use the following equation to calculate the ESR and capacitance value of the output capacitor:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_S \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

This calculation results in C_{OUT_RIPPLE} = 7.6 µF, and R_{ESR} = 27 mΩ.

To meet the ±5% overshoot and undershoot transient requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}^2}$$

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
$K_{OV} = K_{UV} = 2$ are the coefficients for estimation purposes.
ΔI_{STEP} = 3 A is the load transient step.
$\Delta V_{OUT\_OV} = 5\% V_{OUT}$ is the overshoot voltage.
$\Delta V_{OUT\_UV} = 5\% V_{OUT}$ is the undershoot voltage.

This calculation results in C_{OUT_OV} = 53.2 µF, and C_{OUT_UV} = 20.7 µF.

According to the calculation, the output capacitance must be greater than 53 µF, and the ESR of the output capacitor must be smaller than 27 mΩ. It is recommended that two pieces of 47 µF/X5R/6.3 V ceramic capacitors be used, such as the GRM32ER60J476ME20 from Murata, with an ESR of 2 mΩ.

COMPENSATION COMPONENTS

For better load transient and stability performance, set the cross frequency, f_C, to f_{SW}/10. In this case, f_{SW} is running at 600 kHz; therefore, the f_C is set to 60 kHz.

The 47 µF ceramic output capacitor has a derated value of 32 µF.

$$R_C = \frac{2 \times \pi \times 3.3\,V \times 2 \times 32\,\mu F \times 60\,kHz}{0.6\,V \times 470\,\mu s \times 8.7\,A/V} = 32.5\,k\Omega$$

$$C_C = \frac{(0.825\,\Omega + 0.002\,\Omega) \times 2 \times 32\,\mu F}{32.5\,k\Omega} = 1629\,pF$$

$$C_{CP} = \frac{0.002\,\Omega \times 2 \times 32\,\mu F}{32.5\,k\Omega} = 3.9\,pF$$

Choose standard components, as follows: R_C = 31.6 kΩ, C_C = 1500 pF, and C_{CP} = 3.9 pF.

Figure 34 shows the bode plot at 4 A. The cross frequency is 59 kHz, and the phase margin is 55°.

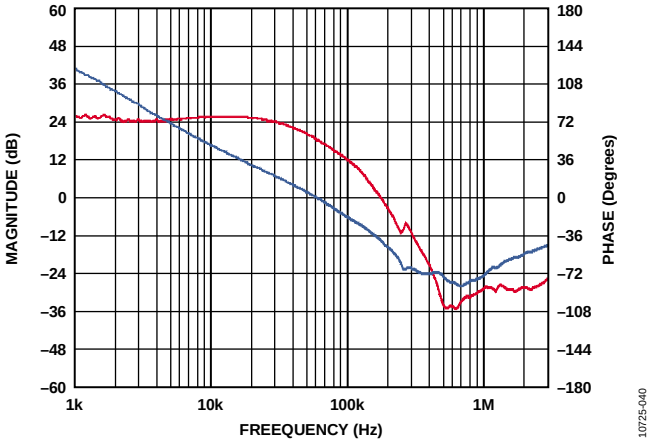

Figure 34. Bode Plot at 4 A

SOFT START TIME PROGRAM

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current. Set the soft start time to 4 ms.

$$C_{SS} = \frac{T_{SS\_EXT} \times I_{SS\_UP}}{0.6} = \frac{4\,ms \times 3.2\,\mu A}{0.6\,V} = 21.3\,nF$$

Choose a standard component value, as follows: C_{SS} = 22 nF.

INPUT CAPACITOR SELECTION

A minimum 10 µF ceramic capacitor must be placed near the PVIN pin. In this application, it is recommended that one 10 µF, X5R, 25 V ceramic capacitor be used.

RECOMMENDED EXTERNAL COMPONENTS

Table 9. Recommended External Components for Typical Applications with 4 A Output Current

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)[1]	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)	C_{CP} (pF)
300	12	1	2.2	680	10	15	47	3300	150
	12	1.2	3.3	680	10	10	59	3300	100
	12	1.5	3.3	470	15	10	47	3300	100
	12	1.8	4.7	470	20	10	60.4	3300	68
	12	2.5	4.7	2 × 100	47.5	15	22	3300	10
	12	3.3	6.8	2 × 100	10	2.21	29.4	3300	8.2
	12	5	10	100 + 47	22	3	34	3300	4.7
	5	1	2.2	680	10	15	47	3300	150
	5	1.2	2.2	470	10	10	39	3300	100
	5	1.5	3.3	470	15	10	47	3300	100
	5	1.8	3.3	3 × 100	20	10	24	3300	15
	5	2.5	3.3	2 × 100	47.5	15	22	3300	10
	5	3.3	3.3	2 × 100	10	2.21	29.4	3300	8.2
600	12	1.5	2.2	3 × 100	15	10	39	1500	10
	12	1.8	2.2	2 × 100	20	10	31.6	1500	8.2
	12	2.5	2.2	2 × 47	47.5	15	24	1500	4.7
	12	3.3	3.3	2 × 47	10	2.21	31.6	1500	4.7
	12	5	4.7	100	22	3	44.2	1500	2.2
	5	1	1	3 × 100	10	15	26.7	1500	10
	5	1.2	1	2 × 100	10	10	21	1500	10
	5	1.5	1.5	2 × 100	15	10	26.7	1500	10
	5	1.8	1.5	100 + 47	20	10	24	1500	8.2
	5	2.5	1.5	100	47.5	15	22	1500	4.7
	5	3.3	1.5	100	10	2.21	28	1500	4.7
1000	12	2.5	1.5	100	47.5	15	37.4	1000	3.3
	12	3.3	2.2	100	10	2.21	47	1000	2.2
	12	5	2.2	100	22	3	69	1000	1
	5	1	1	3 × 100	10	15	43.2	1000	8.2
	5	1.2	1	2 × 100	10	10	33	1000	6.8
	5	1.5	1	100 + 47	15	10	33	1000	4.7
	5	1.8	1	2 × 47	20	10	30	1000	4.7
	5	2.5	1	100	47.5	15	37.4	1000	3.3
	5	3.3	1	100	10	2.21	47	1000	2.2

[1] 680 µF: 4 V, Sanyo 4TPF680M; 470 µF: 6.3 V, Sanyo 6TPF470M; 100 µF: 6.3 V, X5R, Murata GRM32ER60J107ME20; 47 µF: 6.3 V, X5R, Murata GRM32ER60J476ME20.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good printed circuit board (PCB) layout is essential for obtaining the best performance from the ADP2384. Poor PCB layout can degrade the output regulation, as well as the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance. Figure 36 shows an example of a good PCB layout for the ADP2384. For optimum layout, refer to the following guidelines:

- Use separate analog ground planes and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to analog ground. In addition, connect the ground reference of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed GND pad of the ADP2384.
- Place the input capacitor, inductor, and output capacitor as close as possible to the IC, and use short traces.
- Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane.
- In addition, ensure that the high current path from the power ground plane through the inductor and output capacitor back to the power ground plane is as short as possible by tying the PGND pins of the ADP2384 to the PGND plane as close as possible to the input and output capacitors.
- Connect the exposed GND pad of the ADP2384 to a large, external copper ground plane to maximize its power dissipation capability and minimize junction temperature. In addition, connect the exposed SW pad to the SW pins of the ADP2384 using short, wide traces; or connect the exposed SW pad to a large copper plane of the switching node for high current flow.
- Place the feedback resistor divider network as close as possible to the FB pin to prevent noise pickup. Minimize the length of the trace that connects the top of the feedback resistor divider to the output while keeping the trace away from the high current traces and the switching node to avoid noise pickup. To further reduce noise pickup, place an analog ground plane on either side of the FB trace and ensure that the trace is as short as possible to reduce the parasitic capacitance pickup.

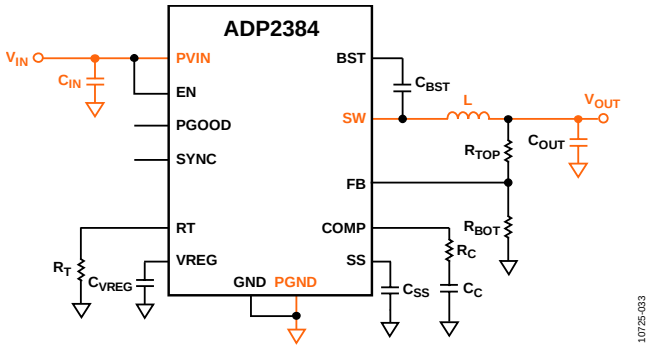

Figure 35. High Current Path in the PCB Circuit

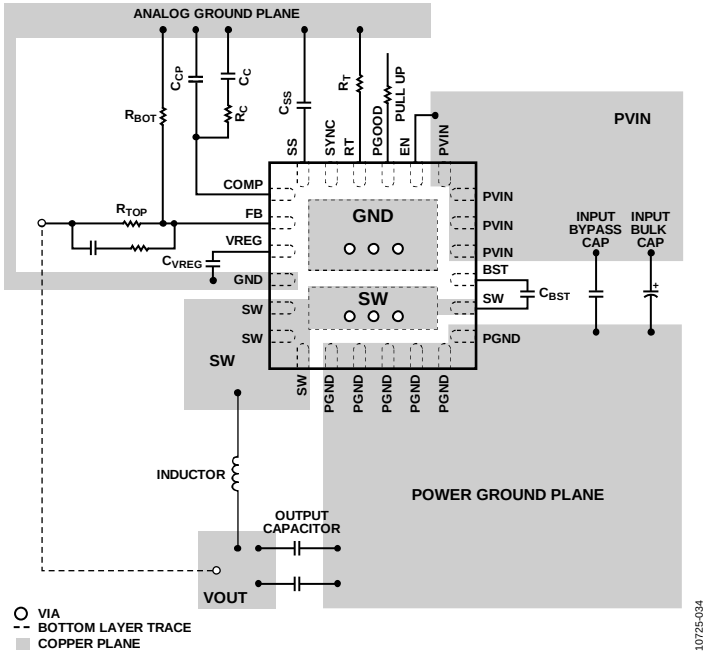

Figure 36. Recommended PCB Layout

TYPICAL APPLICATIONS CIRCUITS

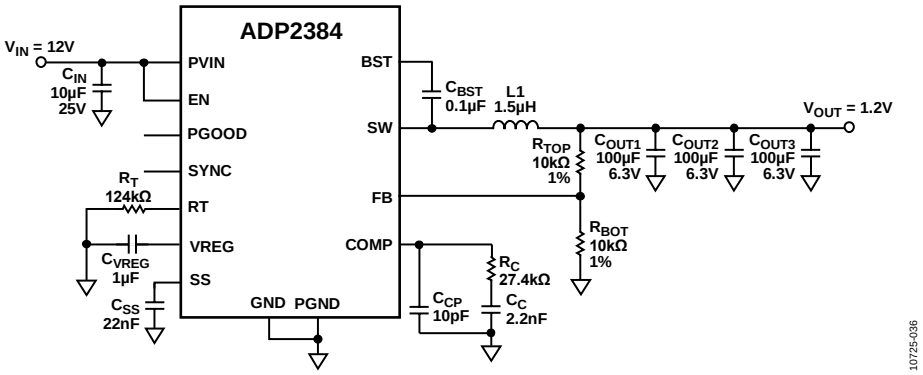

Figure 37. Typical Applications Circuit, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 4 A, f_{SW} = 500 kHz

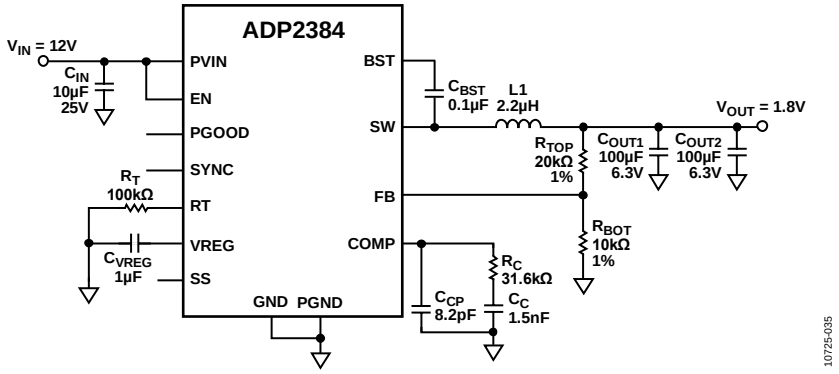

Figure 38. Typical Applications Circuit Using Internal Soft Start, V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 4 A, f_{SW} = 600 kHz

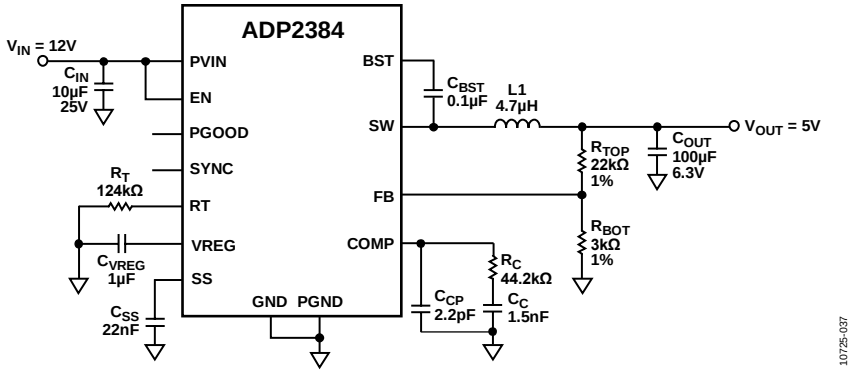

Figure 39. Typical Applications Circuit with Programming Switching Frequency at 500 kHz, V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 4 A, f_{SW} = 500 kHz

OUTLINE DIMENSIONS

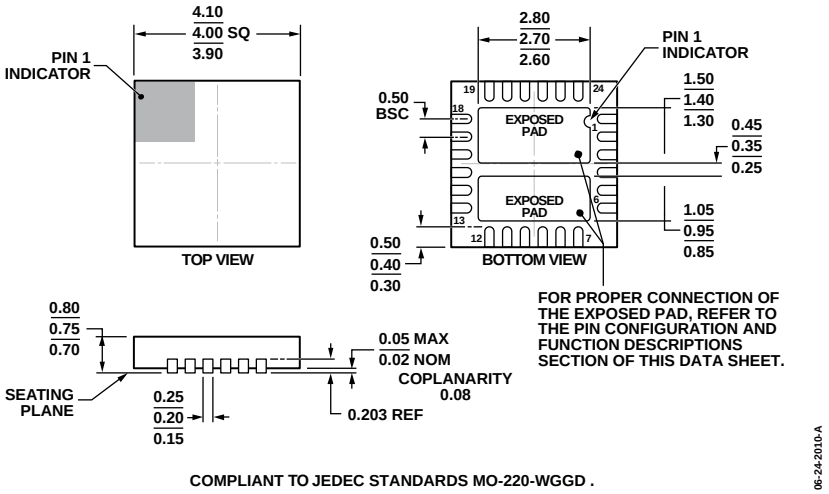

Figure 40. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Packing
ADP2384ACPZN-R7	−40°C to +125°C	24-Lead LFCSP_WQ	CP-24-12	7″ Tape and Reel
ADP2384-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES