Integrated Device Technology, Inc.

128K x 16
64K x 16
32K x 16
CMOS DUAL-PORT RAM
(SHARED MEMORY MODULE)

IDT7MB6036
IDT7MB6046
IDT7MB6056

FEATURES:

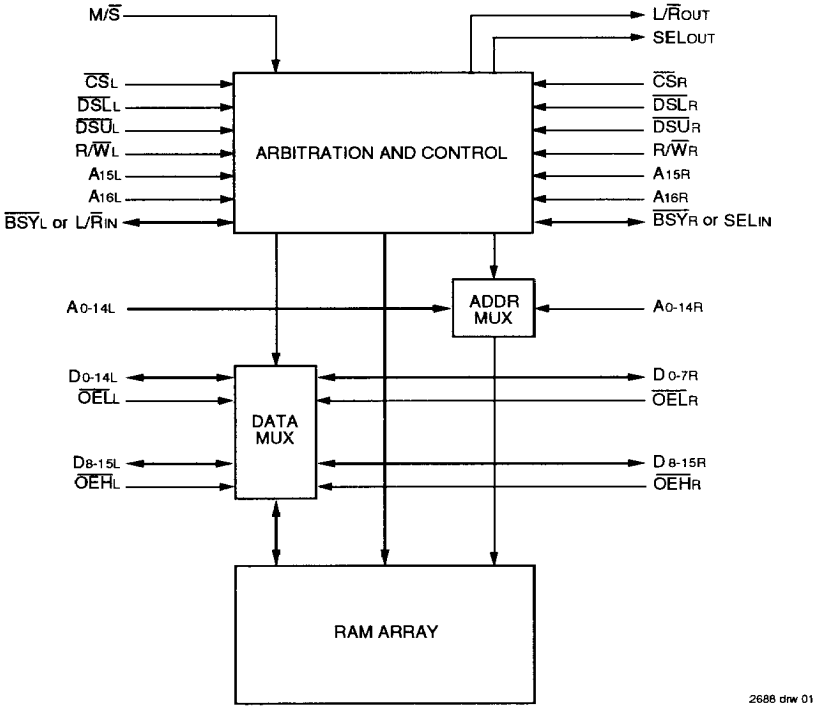
- High density 2 megabit/1 megabit/512K-bit CMOS Dual-Port static RAM (shared memory modules)
- Fully asynchronous read/write operation from either port
- Port arbitration/multiplexing logic by custom FCT chip set
- Memory array comprised of industry standard static RAM component
- Fast access time
  - 40ns (max.)
- Versatile controls: $\overline{BUSY}$ output flag and separate controls for lower and upper byte writes on each port
- Master/Slave control on-board for expanding word width
- Multiple GND and Vcc pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply

DESCRIPTION:

The Shared Memory Module provides two ports with separate control, address and Data I/O pins that permit independent access for read or writes to any location in the memory array. Using the on-board Master/Slave input allows these modules to be used as building blocks in 32-bit or more-bit systems requiring full speed operation without additional discrete logic.

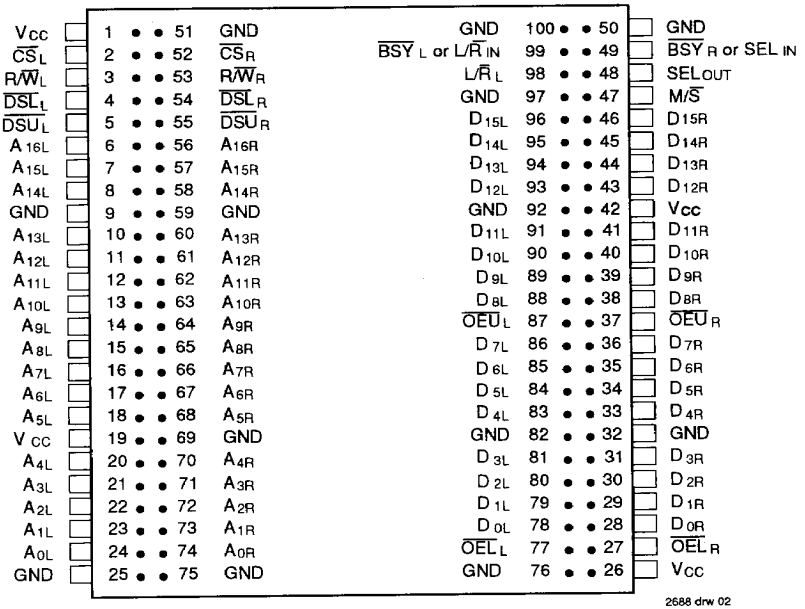
In the Master Mode, the Shared Memory Module arbitrates asynchronously between the left and right ports $\overline{CS}$ inputs. The first to arrive is granted exclusive access to the entire RAM array for as long as its $\overline{CS}$ is asserted. If both ports attempt simultaneous access, the losing port will have its $\overline{BUSY}$ asserted until the winning port completes it access, at which time the second port will be granted its own exclusive access to the entire RAM array. See application note AN-74 for more details regarding proper module operating modes.

FUNCTIONAL BLOCK DIAGRAM[1]



7-6-1

PIN CONFIGURATION (1, 2)



2688 drw 02

NOTES:
1. Pins 7 and 57 must be grounded for proper operation of the 7MB6046 module.
2. Pins 6, 7, 56 and 57 must be grounded for proper operation of the 7MB6056 module.

PIN DESCRIPTION

Symbol	Description
Vcc	Power
GND	Ground
A0-16L	Left Port Address
D0-15L	Left Port Data
A0-16R	Right Port Address
D0-15R	Right Port Data
R/W	Read/Write Control
CS	Active Low Chip Select
DSL	Data Strobe for Lower Byte
DSU	Data Strobe for Upper Byte
OEL	Output Enable for Lower Byte
OEU	Output Enable for Upper Byte
BSYL or L/RIN	Left Busy Output for Stand Alone or Master Mode. Left or Right Port Select Input for Slave Mode.
BSYR or SELIN	Right Busy Output for Stand Alone or Master Mode. RAM Array Select Input for Slave Mode.
L/ROUT	Left or Right Port Select Output on Master to be Connected to L/R_IN Input on One or More Slaves when Width Expansion is Required.
SELOUT	RAM Array Select Output on Master to be Connected to SEL_IN Input on One or More Slaves when Width Expansion is Required.
M/S	Master/Slave signal for cascading master w/one or more slaves.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2688 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

2688 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2688 tbl 04

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2688 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	15	µA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, f = f_{MAX}, Output Open	—	520	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$, V_{CC}= MAX. Outputs Open, f = f_{MAX}.	—	200	mA
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = –8mA	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 16mA		0.4	V

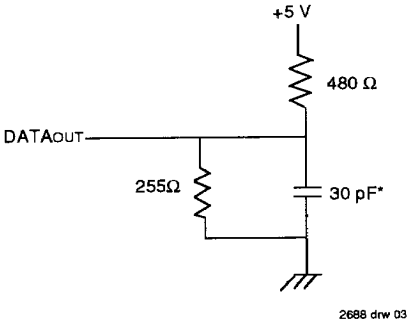
2688 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2688 tbl 07

1-7-3



*Including scope and jig.

Figure 1. Output Load

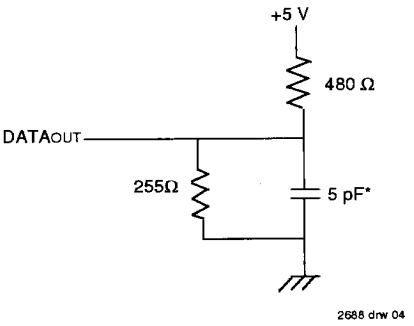


Figure 1. Output Load (for tOHZ and tOLZ)

AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V + 10%, TA = 0°C to +70°C)

Symbol	Parameter	-40		-50		-60		-70		-85		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
No Contention Read														
tRC	Read Cycle Time	40	—	50	—	60	—	70	—	85	—	100	—	ns
tAA	Address Access Time	—	40	—	50	—	60	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	40	—	50	—	60	—	70	—	85	—	100	ns
tOE	Output Enable to Data Valid	22	—	—	27	—	32	—	37	—	42	—	47	ns
tOH	O/P Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOLZ(1)	$\overline{OE}$ to Output in Low-Z	8	—	8	—	8	—	8	—	8	—	8	—	ns
tOHZ(1)	$\overline{OE}$ to Output in High-Z	—	7.5	—	7.5	—	7.5	—	7.5	—	7.5	—	7.5	ns
No Contention Write														
tWC	Write Cycle Time	40	—	50	—	60	—	70	—	85	—	100	—	ns
tAW	Address Valid to End of Write	35	—	45	—	50	—	60	—	75	—	90	—	ns
tCW	$\overline{CS}$ to End of Write	35	—	45	—	50	—	60	—	75	—	90	—	ns
tAS	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tCDS	$\overline{CS}$ to Data Strobe	15	—	15	—	15	—	15	—	15	—	15	—	ns
tDS	Data Strobe Width	20	—	25	—	30	—	35	—	50	—	60	—	ns
tWR	Write Recovery Time	3	—	3	—	5	—	5	—	5	—	5	—	ns
tDW	Data Valid to End of Write	22	—	22	—	25	—	30	—	45	—	50	—	ns
tDH	Data Hold from End of Write	5	—	5	—	5	—	5	—	10	—	10	—	ns
Contention Read														
tCB	$\overline{CS}$ to BUSY	—	12	—	12	—	12	—	15	—	20	—	20	ns
tBD	Busy Negate to Data Valid	—	40	—	50	—	60	—	70	—	85	—	100	ns
Contention Write														
tCB	$\overline{CS}$ to BUSY	—	12	—	12	—	12	—	15	—	20	—	20	ns
tBDS	Busy Negate to Data Strobe	7	—	7	—	7	—	10	—	15	—	15	—	ns
Slave Timing														
tLR	$\overline{CS}$ to L/R Output	—	11	—	11	—	11	—	15	—	20	—	20	ns
tSEL	$\overline{CS}$ to Select Output	—	14	—	14	—	14	—	15	—	20	—	20	ns
tAPS	Arbitration Priority Set-up Time	5	—	5	—	5	—	5	—	5	—	5	—	ns

2688 tbl 08

NOTE:
1. This parameter guaranteed by design but not tested.

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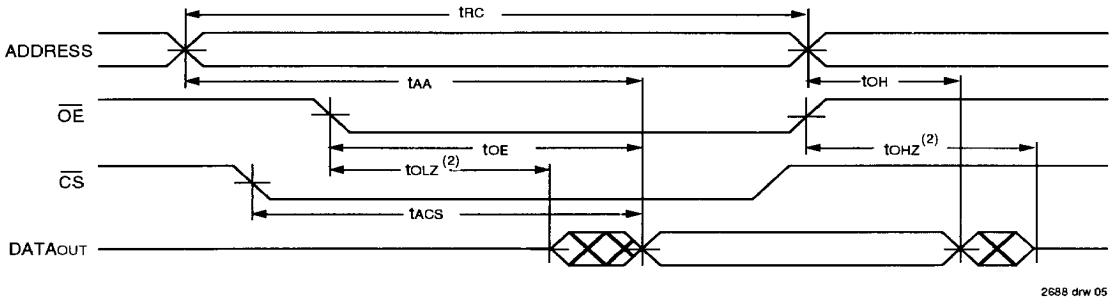
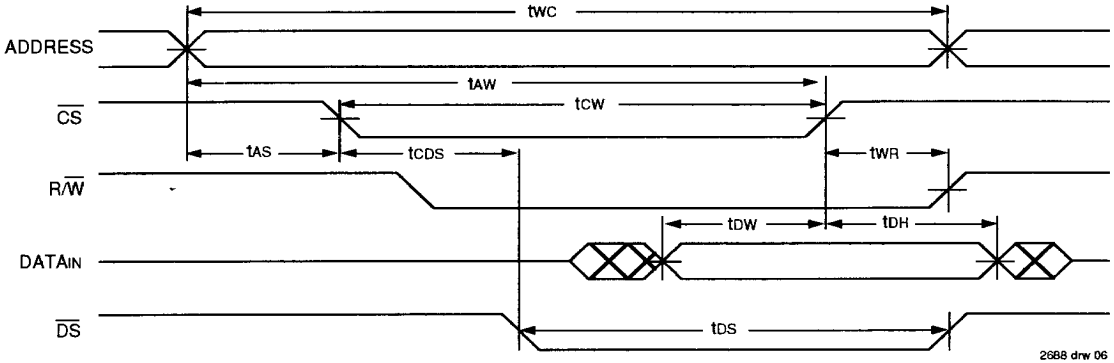
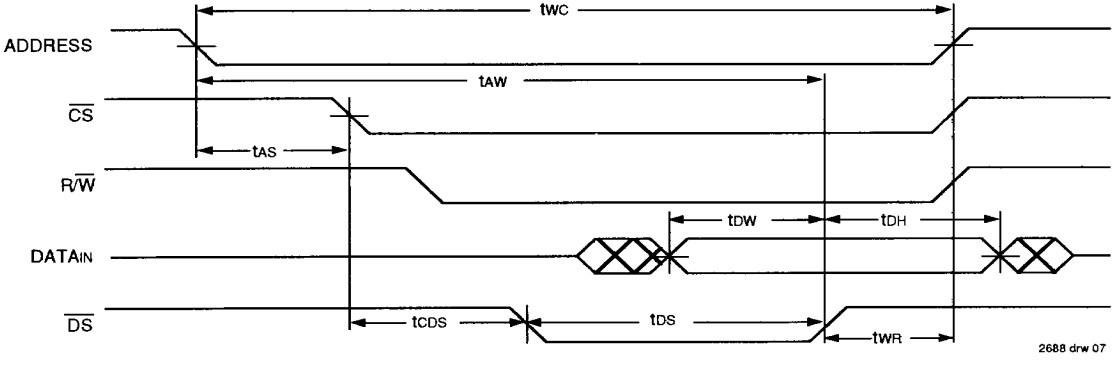
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF WRITE CYCLE (CS CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE (DS CONTROLLED)



NOTES:
1. R/W = VIH.
2. Transition is measured +200mV from steady state with 5pF load (including scope and jig. This parameter guaranteed by design, but not tested.

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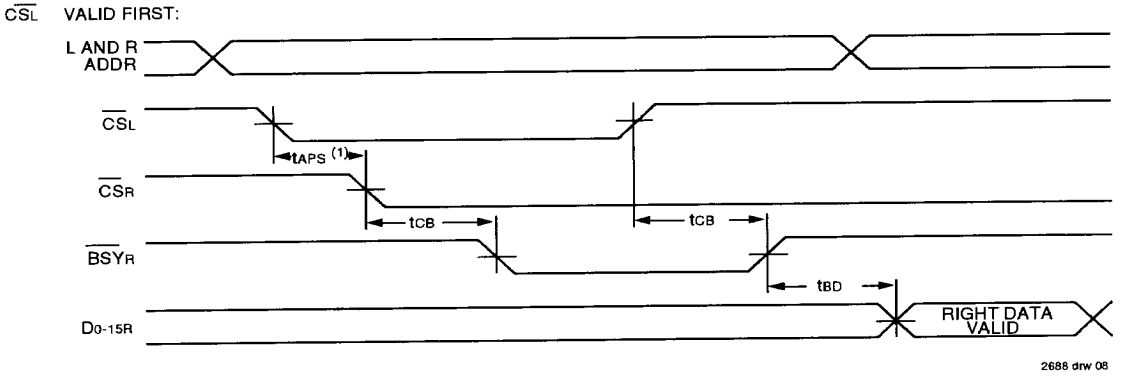
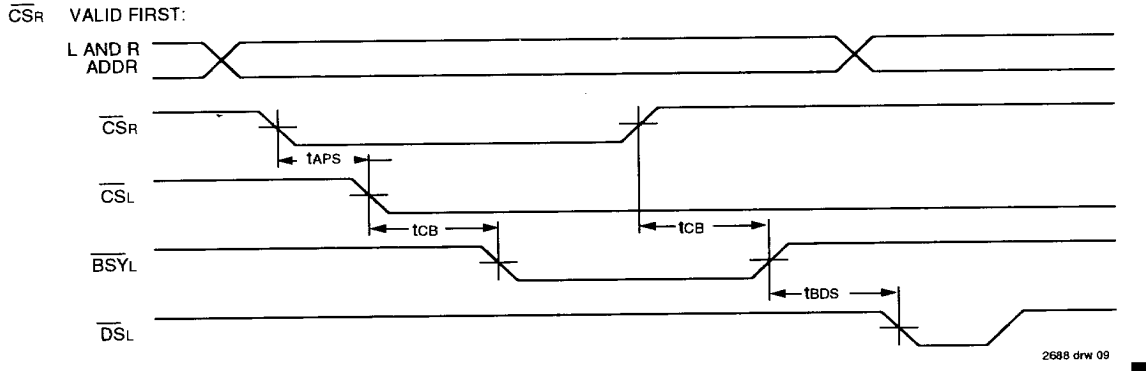
TIMING WAVEFORM OF CONTENTION READ, ($\overline{CS}$ ARBITRATION)



TIMING WAVEFORM OF CONTENTION WRITE, ($\overline{CS}$ ARBITRATION)



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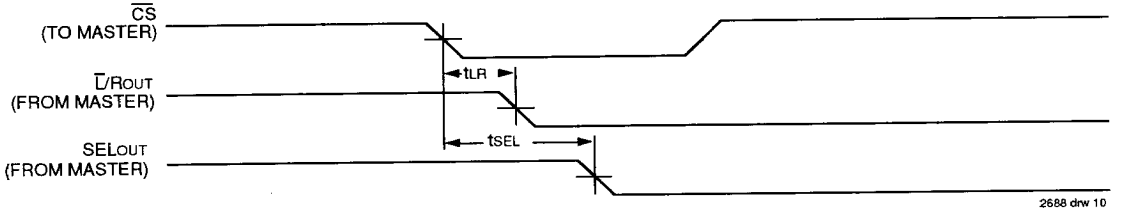
TIMING WAVEFORM OF SLAVE(2)

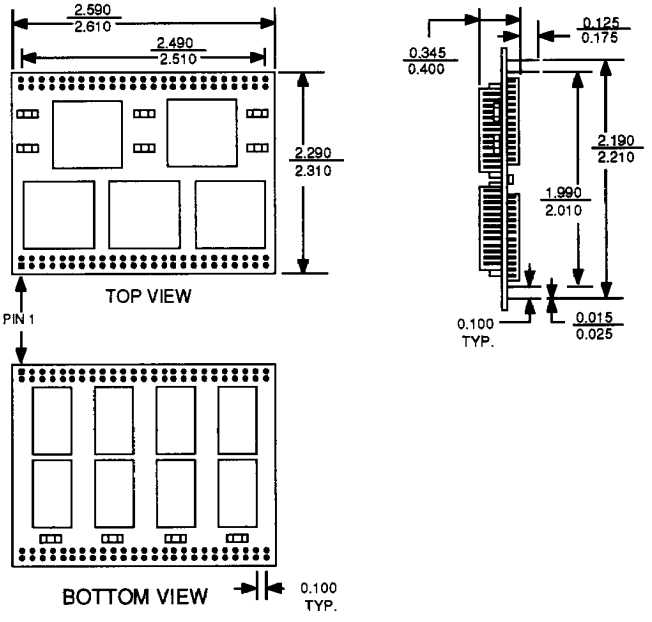


NOTES:
1. tAPS is only necessary to guarantee left side access. Within this set-up time, one side or the other will gain access, but neither will have priority.
2. $\overline{CS}$ inputs are ignored when configured as a Slave, allowing the Master to control port selection with L/$\overline{R}$_OUT and SEL_OUT signals.

7-7-6

PACKAGE DIMENSIONS

7MB6036



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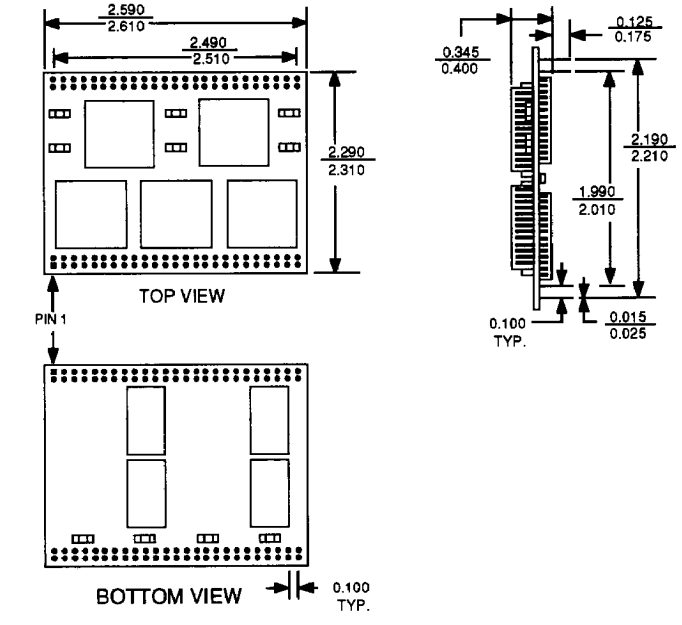
7MB6046



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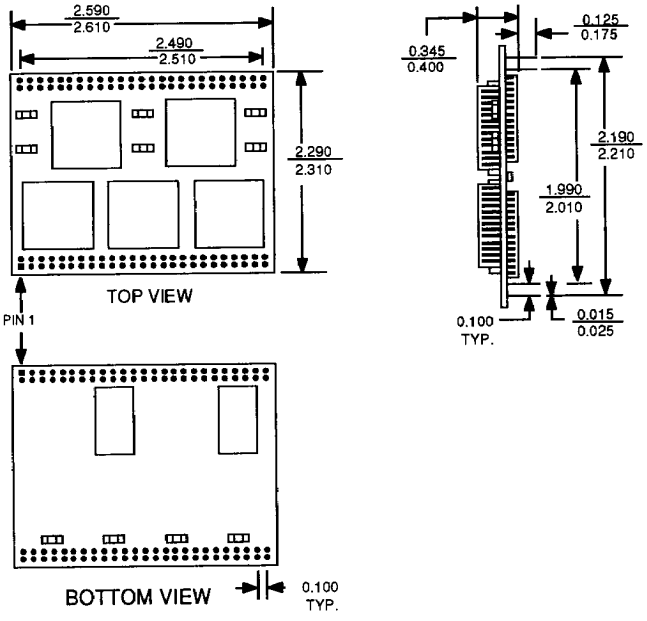
7MB6056



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