

### Features

- PCB area: 0.09 mm<sup>2</sup>
- Bidirectional device
- Low capacitance: 8 pF max.
- Minimum breakdown voltage  $V_{BR} = 6\text{ V}$
- Low leakage current: lower than 50 nA at 3 V
- RoHS compliant

### Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Portable multimedia devices and accessories
- MID, netbooks and notebooks
- Digital cameras and camcorders
- Communication systems
- Smart phones and accessories

### Description

The ESDAVLC6-1BV2 is a single line bidirectional transil diode designed specially for the protection of integrated circuits into portable equipment and miniaturized electronics devices subject to ESD transient overvoltage.

The device is ideal for applications where both reduced printed circuit board space and high ESD protection level are required.

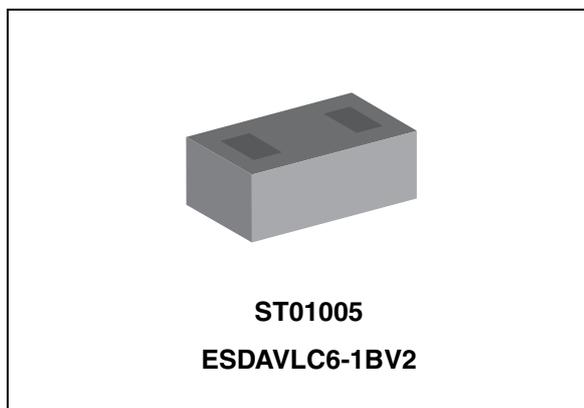
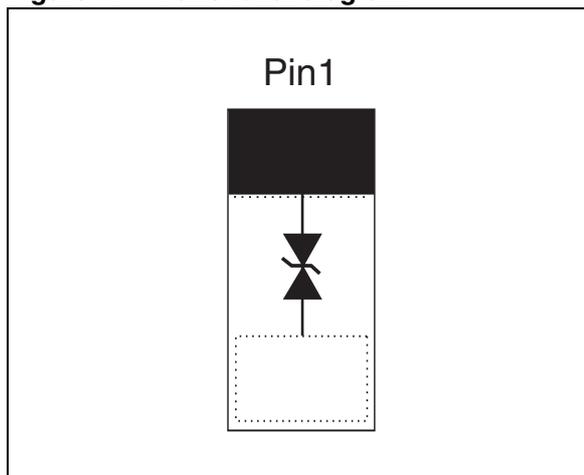


Figure 1. Functional diagram



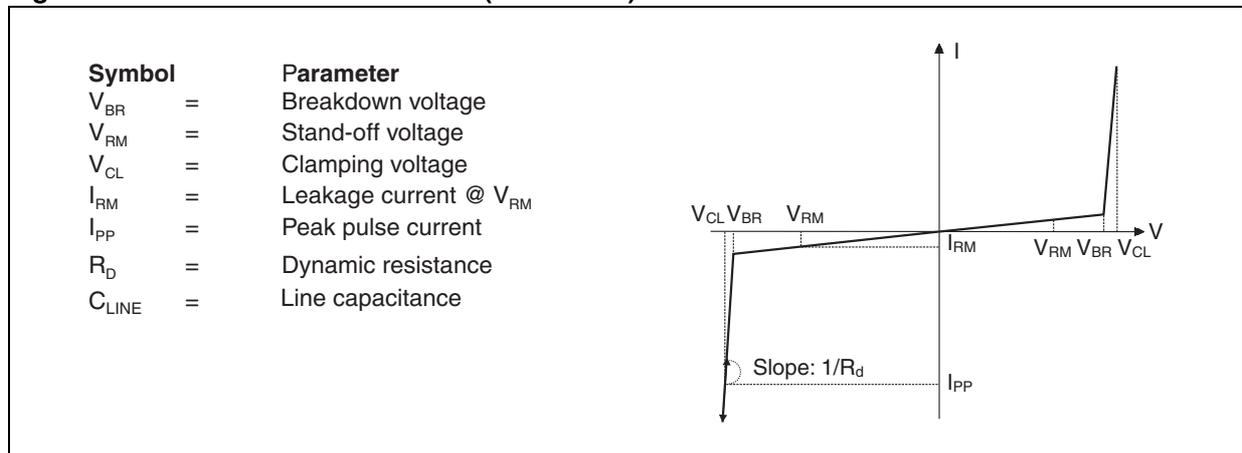
# 1 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter		Value	Unit
$V_{PP}$	Peak pulse voltage	IEC 61000-4-2 contact discharge	12	kV
		IEC 61000-4-2 air discharge	15	
$I_{PP}$	Peak pulse current (8/20 $\mu\text{s}$ ) <sup>(1)</sup>		2.5	A
$P_{PP}$	Peak pulse power (8/20 $\mu\text{s}$ ) <sup>(1)</sup>		45	W
$T_j$	Operating temperature range		-55 to +150	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range		- 65 to +150	$^{\circ}\text{C}$
$T_L$	Maximum lead temperature for soldering during 10 s		260	$^{\circ}\text{C}$

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

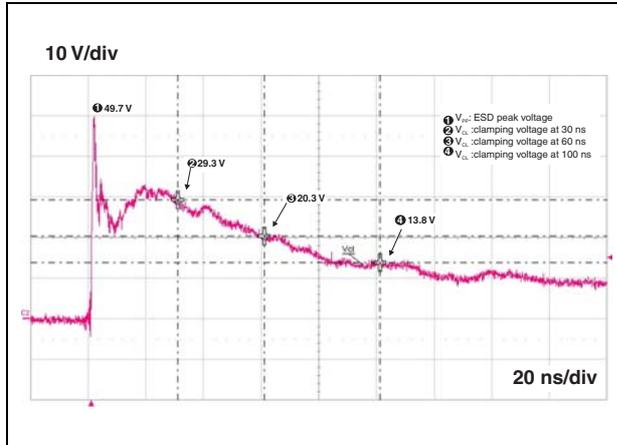
**Figure 2. Electrical characteristics (definitions)**



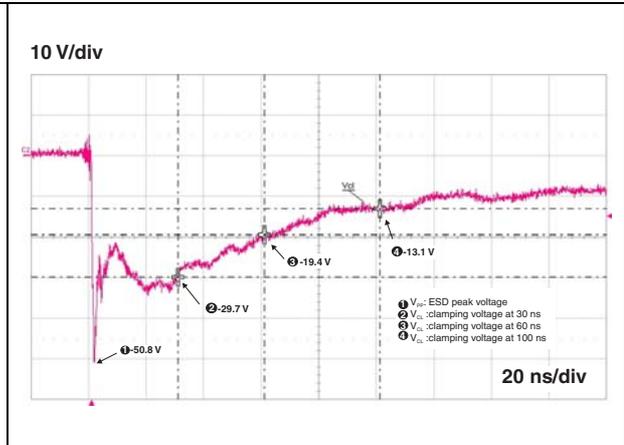
**Table 2. Electrical characteristics (values,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{BR}$	Breakdown voltage	$I_R = 1\text{ mA}$	6			V
$I_{RM}$	Leakage current	$V_{RM} = 3\text{ V}$			50	nA
$V_{CL}$	Clamping voltage	$I_{PP} = 1\text{ A}, 8/20\text{ }\mu\text{s}$			12	V
		$I_{PP} = 2.5\text{ A maximum}, 8/20\text{ }\mu\text{s}$			18	
$C_{line}$	Line capacitance, I/O to GND	$V_R = 0\text{ V}, F = 1\text{ MHz}, V_{osc} = 30\text{ mV}$		7.5	8	pF

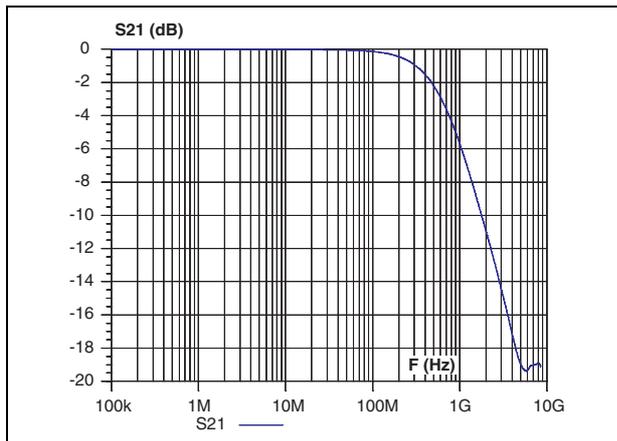
**Figure 3. ESD response to IEC 61000-4-2 (typical values, +8 kV contact discharge)**



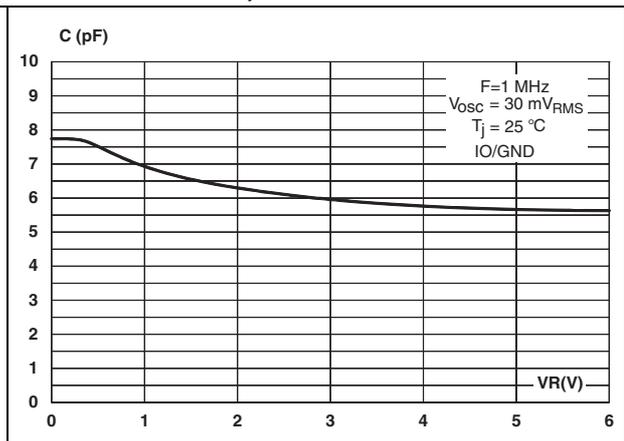
**Figure 4. ESD response to IEC 61000-4-2 (typical values, -8 kV contact discharge)**



**Figure 5. S21 attenuation measurement**

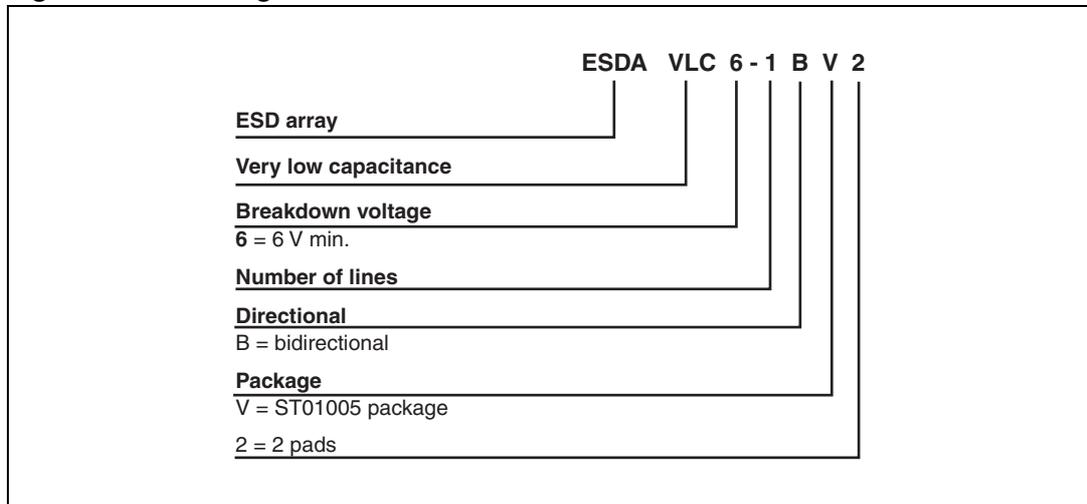


**Figure 6. Junction capacitance versus reverse applied voltage (typical values)**



## 2 Ordering information scheme

Figure 7. Ordering information scheme

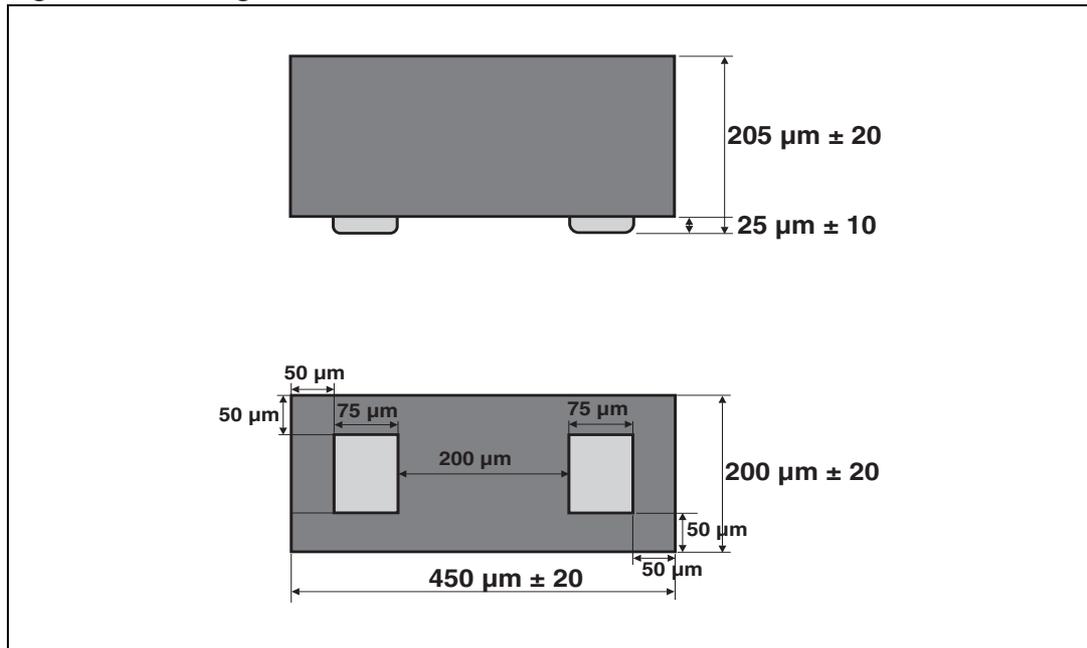


### 3 Package information

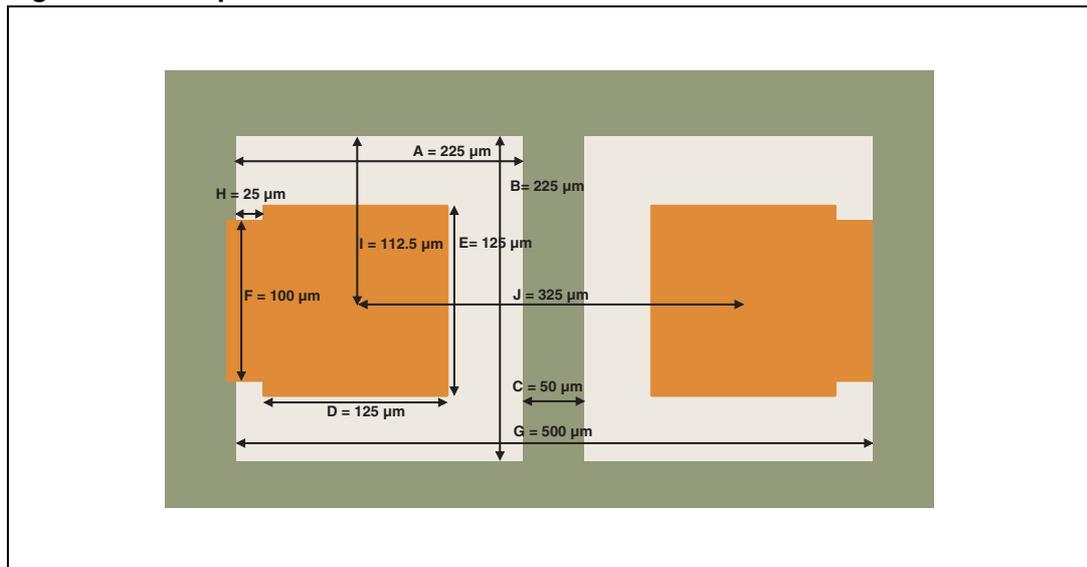
- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Figure 8. Package dimensions**



**Figure 9. Footprint recommendation**

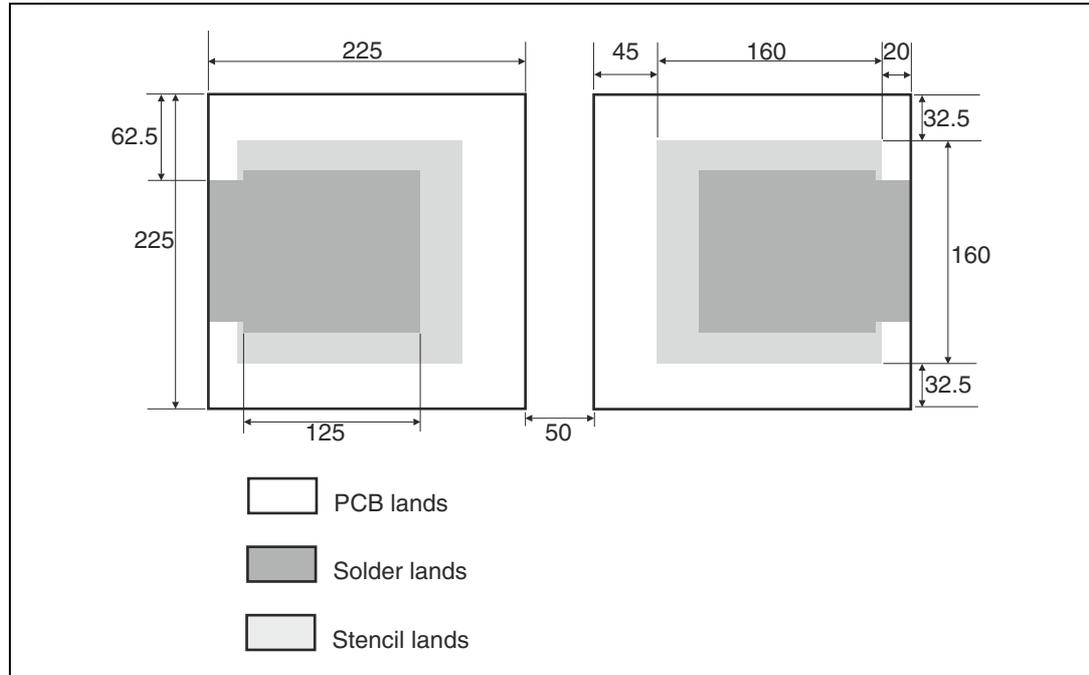


## 4 Recommendation on PCB assembly

### 4.1 Stencil opening design

Stencil opening thickness: 80 µm

**Figure 10. Recommended stencil window position**



### 4.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Solder paste with fine particles: type 4 (powder particle size 20-38 µm per IPC J-STD-005).

### 4.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Tolerance of ± 0.02 mm is recommended.

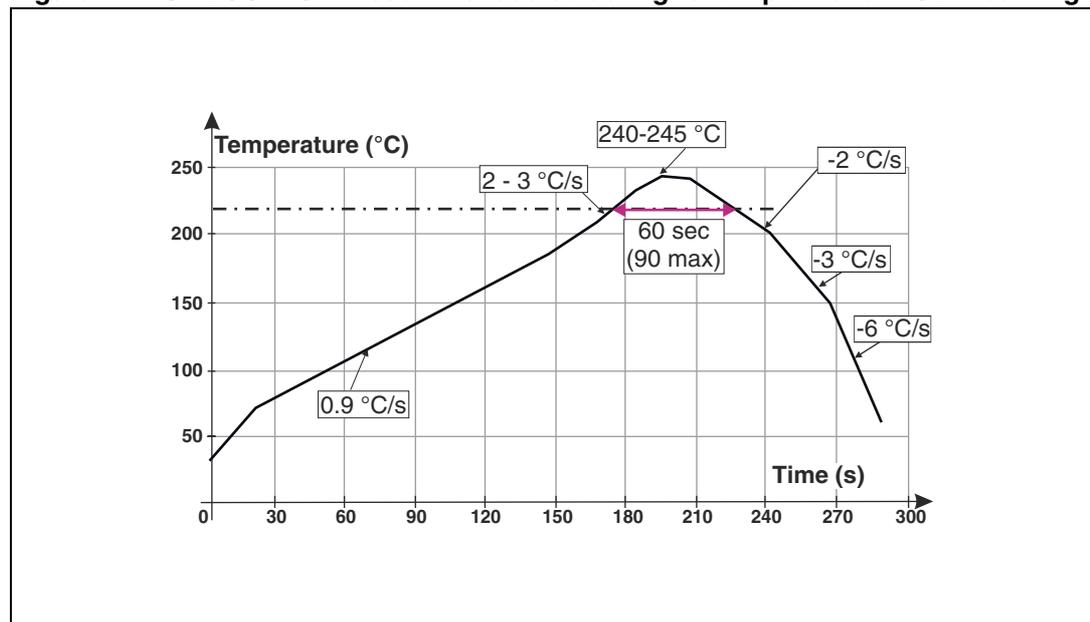
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

#### 4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

#### 4.5 Reflow profile

Figure 11. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

## 5 Ordering information

Table 3. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDAVLC6-1BV2	No marking	0.041 mg	20 000	Tape and reel

## 6 Revision history

Table 4. Document revision history

Date	Revision	Changes
05-Dec-2012	1	First issue

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