CY7C1480V25
CY7C1482V25
CY7C1486V25

72-Mbit (2M x 36/4M x 18/1M x 72) Pipelined Sync SRAM

Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250, 200, and 167 MHz
- Registered inputs and outputs for pipelined operation
- 2.5V core power supply
- 2.5V/1.8V IO operation
- Fast clock-to-output time
  — 3.0 ns (for 250-MHz device)
- Provide high-performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed writes
- Asynchronous output enable
- Single cycle chip deselect
- CY7C1480V25, CY7C1482V25 available in JEDEC-standard Pb-free 100-pin TQFP, Pb-free and non-Pb-free 165-ball FBGA package. CY7C1486V25 available in Pb-free and non-Pb-free 209-ball FBGA package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- “ZZ” Sleep Mode option

Functional Description[1]

The CY7C1480V25/CY7C1482V25/CY7C1486V25 SRAM integrates 2M x 36/4M x 18/1M × 72 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE_1}$), depth-expansion Chip Enables (CE_2 and $\overline{CE_3}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW_X}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) is active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. This part supports Byte Write operations (see “Pin Definitions” on page 7 and “Truth Table” on page 10 for further details). Write cycles can be one to two or four bytes wide, as controlled by the byte write control inputs. When it is active LOW, $\overline{GW}$ causes all bytes to be written.

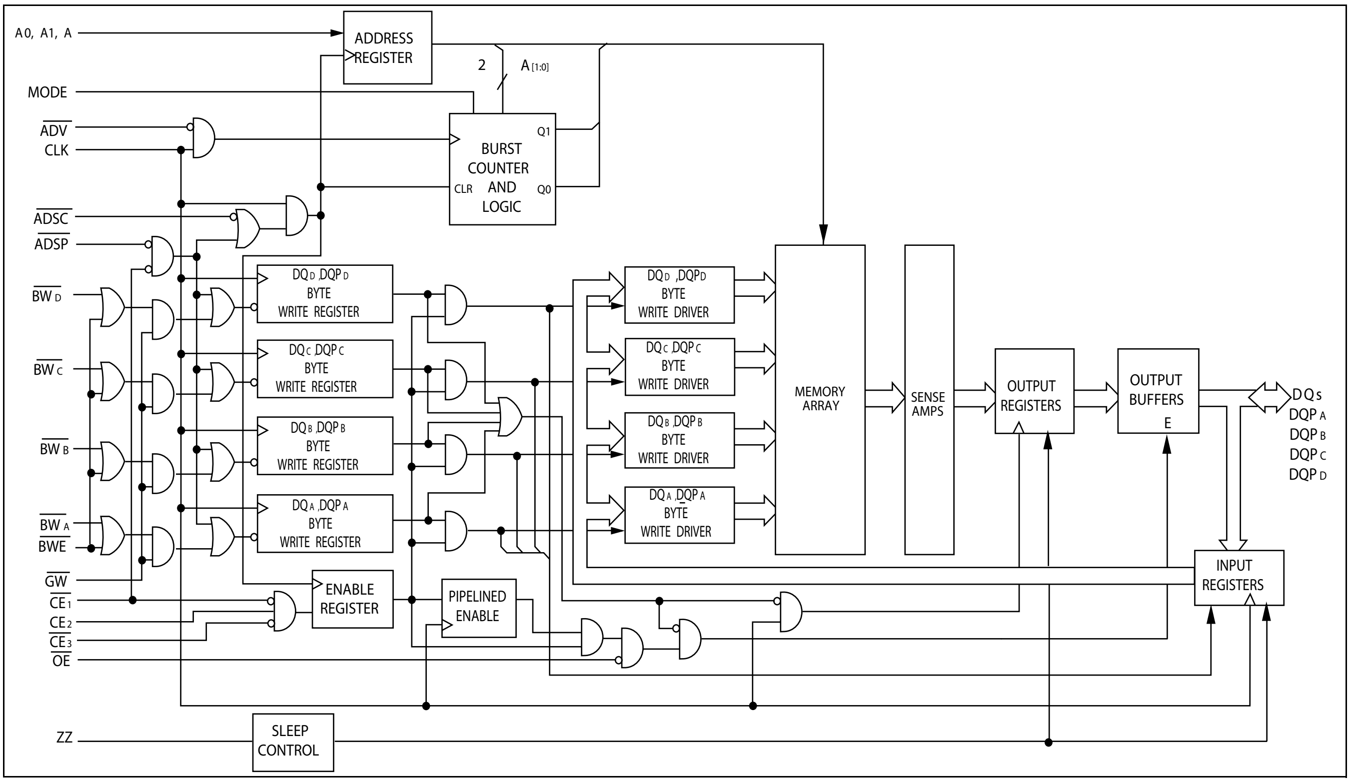
The CY7C1480V25/CY7C1482V25/CY7C1486V25 operates from a +2.5V core power supply while all outputs may operate with either a +2.5 or +1.8V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

Selection Guide

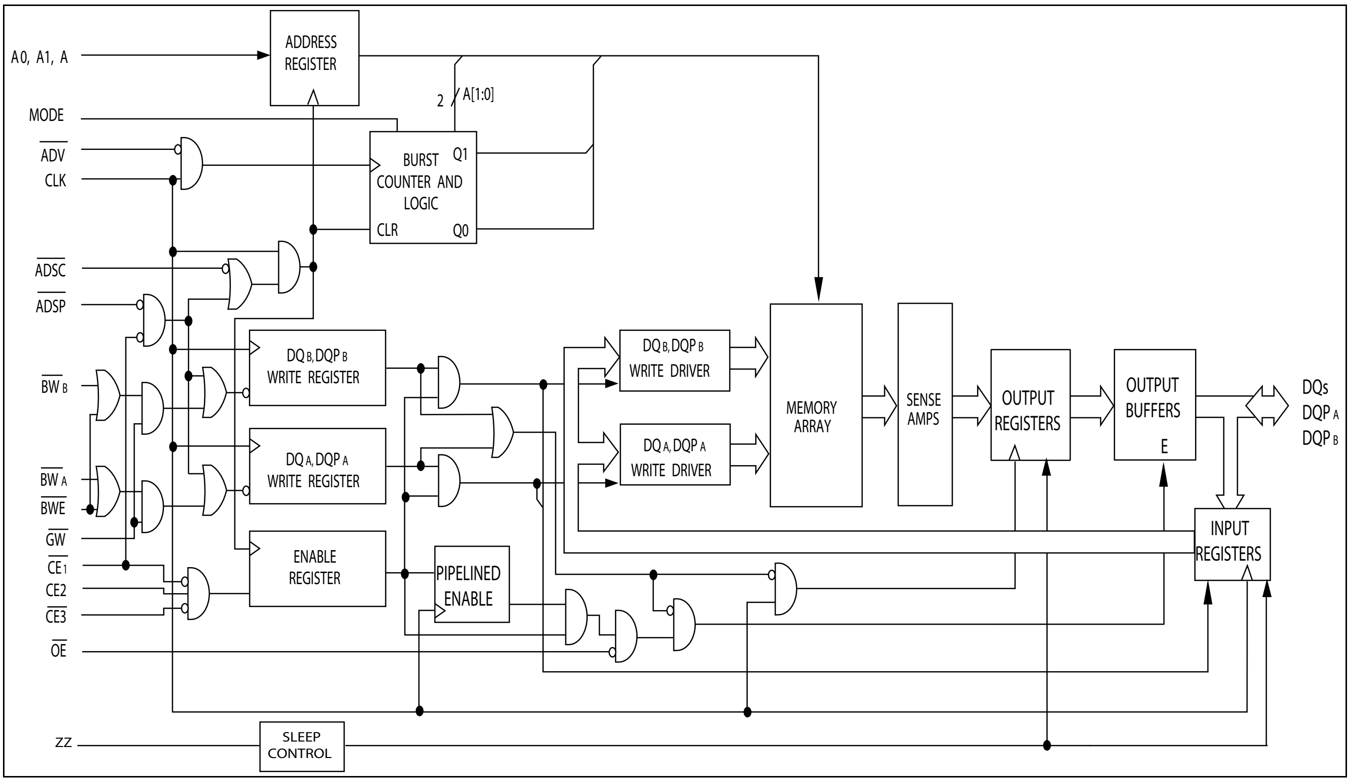
	250 MHz	200 MHz	167 MHz	Unit
Maximum Access Time	3.0	3.0	3.4	ns
Maximum Operating Current	450	450	400	mA
Maximum CMOS Standby Current	120	120	120	mA

Note
1. For best practices recommendations, refer to the Cypress application note *System Design Guidelines* at www.cypress.com.

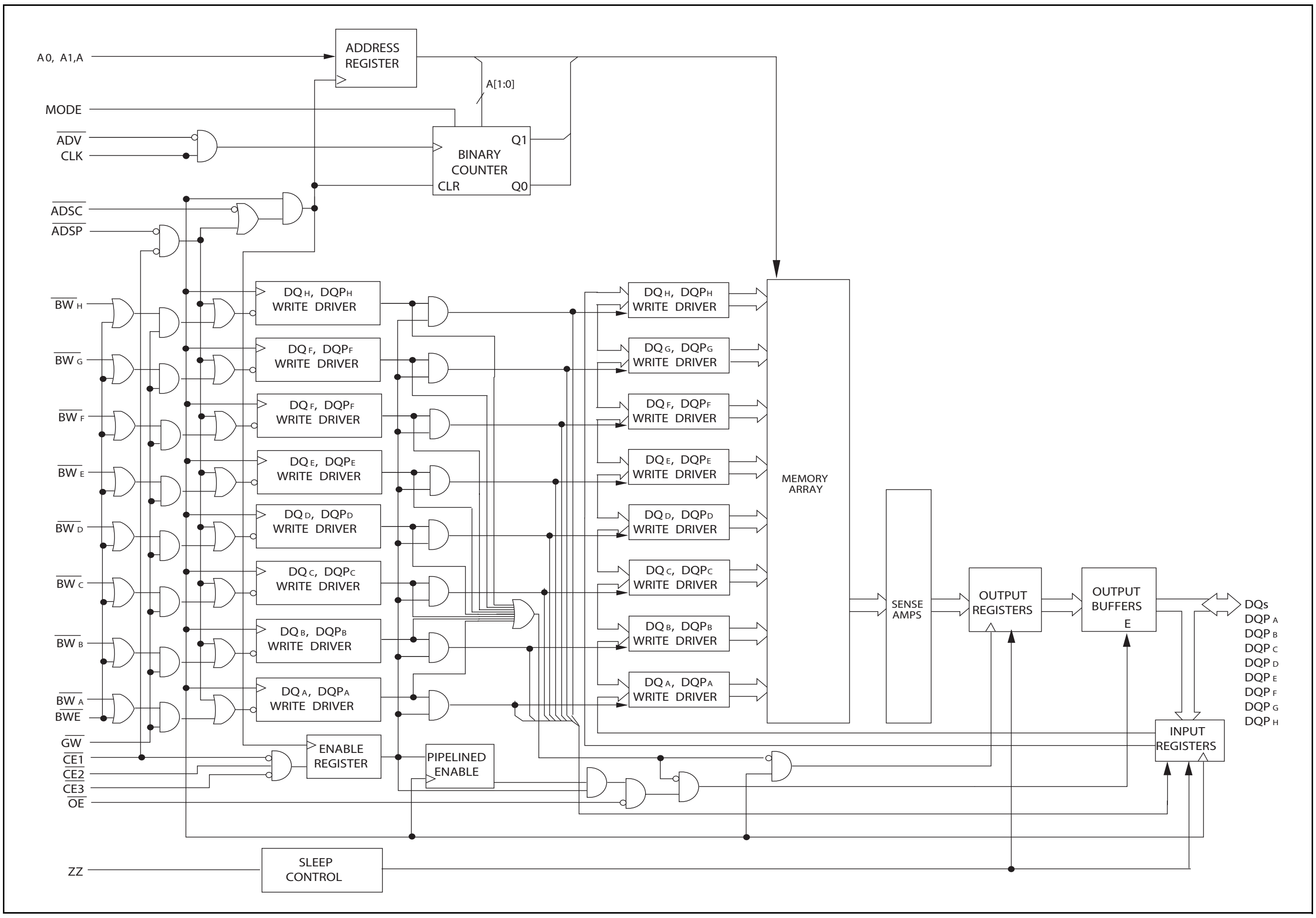
Logic Block Diagram – CY7C1480V25 (2M x 36)



Logic Block Diagram – CY7C1482V25 (4M x 18)

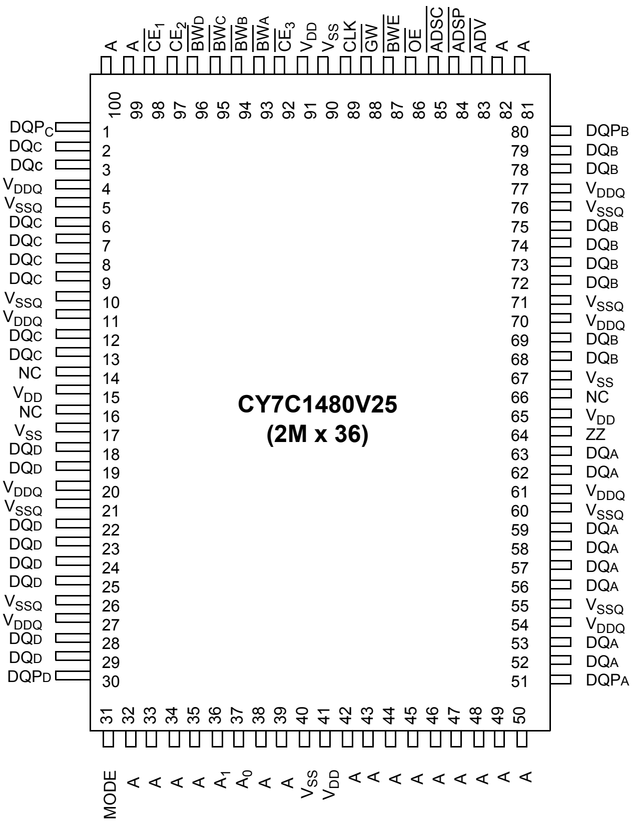


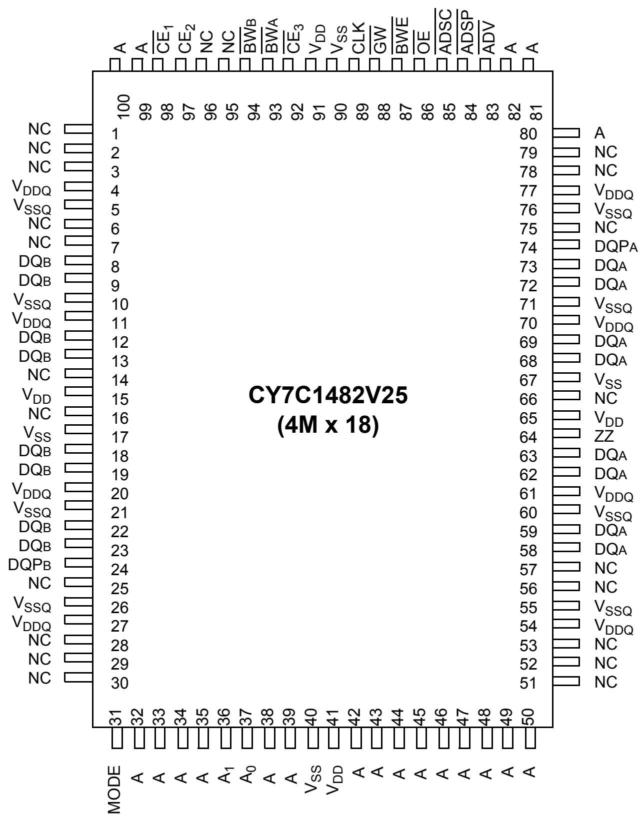
Logic Block Diagram – CY7C1486V25 (1M x 72)



Pin Configurations

100-Pin TQFP Pinout





Pin Configurations (continued)

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

CY7C1480V25 (2M x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	A	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

CY7C1482V25 (4M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC/144M	A	CE2	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_A
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	A	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Configurations (continued)

209-Ball FBGA (14 x 22 x 1.76 mm) Pinout

CY7C1486V25 (1M × 72)

	1	2	3	4	5	6	7	8	9	10	11
A	DQ_G	DQ_G	A	CE_2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{CE}_3$	A	DQ_B	DQ_B
B	DQ_G	DQ_G	$\overline{BWS}_C$	$\overline{BWS}_G$	NC/288M	$\overline{BWE}$	A	$\overline{BWS}_B$	$\overline{BWS}_F$	DQ_B	DQ_B
C	DQ_G	DQ_G	$\overline{BWS}_H$	$\overline{BWS}_D$	NC/144M	$\overline{CE}_1$	NC/576M	$\overline{BWS}_E$	$\overline{BWS}_A$	DQ_B	DQ_B
D	DQ_G	DQ_G	V_{SS}	NC	NC/1G	$\overline{OE}$	$\overline{GW}$	NC	V_{SS}	DQ_B	DQ_B
E	DQP_G	DQP_C	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_F	DQP_B
F	DQ_C	DQ_C	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_F	DQ_F
G	DQ_C	DQ_C	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_F	DQ_F
H	DQ_C	DQ_C	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_F	DQ_F
J	DQ_C	DQ_C	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_F	DQ_F
K	NC	NC	CLK	NC	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC	NC
L	DQ_H	DQ_H	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_A	DQ_A
M	DQ_H	DQ_H	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQ_A	DQ_A
N	DQ_H	DQ_H	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_A	DQ_A
P	DQ_H	DQ_H	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQ_A	DQ_A
R	DQP_D	DQP_H	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_A	DQP_E
T	DQ_D	DQ_D	V_{SS}	NC	NC	MODE	NC	NC	V_{SS}	DQ_E	DQ_E
U	DQ_D	DQ_D	A	A	A	A	A	A	A	DQ_E	DQ_E
V	DQ_D	DQ_D	A	A	A	A1	A	A	A	DQ_E	DQ_E
W	DQ_D	DQ_D	TMS	TDI	A	A0	A	TDO	TCK	DQ_E	DQ_E

Pin Definitions

Pin Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. A1: A0 are fed to the two-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$, $\overline{BW}_E$, $\overline{BW}_F$, $\overline{BW}_G$, $\overline{BW}_H$	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock Input**. Captures all synchronous inputs to the device. Also increments the burst counter when $\overline{ADV}$ is asserted LOW during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the IO pins. When LOW, the IO pins behave as outputs. When deasserted HIGH, IO pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ "sleep" Input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQs, DQPs	I/O-Synchronous	**Bidirectional Data IO lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device.**
V_{SSQ}[2]	I/O Ground	**Ground for the I/O circuitry.**
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.

Note

2. Applicable for TQFP package. For BGA package V_{SS} serves as ground for the core and the IO circuitry.

Pin Definitions (continued)

Pin Name	I/O	Description
MODE	Input Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull up.
TDO	JTAG Serial Output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be disconnected. This pin is not available on TQFP packages.
TDI	JTAG Serial Input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TMS	JTAG Serial Input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not used, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	-	**No Connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.0 ns (250 MHz device).

The CY7C1480V25/CY7C1482V25/CY7C1486V25 supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW_X) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable (OE) provide easy bank selection and output tri-state control. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (3) the write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the Address Register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.0 ns (250-MHz device) if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single read cycles are supported. After the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will tri-state immediately.

Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The write signals (GW, BWE, and BW_X) and ADV inputs are ignored during this first cycle.

ADSP-triggered write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the write operation is controlled by the BWE and BW_X signals.

The CY7C1480V25/CY7C1482V25/CY7C1486V25 provides Byte Write capability that is described in the "Truth Table for Read/Write" on page 11. Asserting the Byte Write Enable input (BWE) with the selected Byte Write (BW_X) input, will selectively write to only the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because CY7C1480V25/CY7C1482V25/CY7C1486V25 is a common IO device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs inputs. Doing so tri-states the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) CE_1, CE_2, CE_3 are all asserted active, and (4) the appropriate combination of the write inputs (GW, BWE, and BW_X) are asserted active to conduct a write to the desired byte(s). ADSC-triggered write accesses need a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because CY7C1480V25/CY7C1482V25/CY7C1486V25 is a common IO device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQs inputs. Doing so tri-states the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1480V25/CY7C1482V25/CY7C1486V25 provides a two-bit wraparound counter, fed by A1: A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting ADV LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CE_1, CE_2, CE_3, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Sleep Mode Standby Current	$ZZ \geq V_{DD} - 0.2V$		120	mA
t_{ZZS}	Device Operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ Recovery Time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ Active to Sleep Current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to Exit Sleep Current	This parameter is sampled	0		ns

Truth Table

The truth table for CY7C1480V25, CY7C1482V25, and CY7C1486V25 follows.[3, 4, 5, 6, 7]

Operation	Add. Used	$\overline{CE}_1$	CE_2	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L-H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes
3. X = “Don't Care.” H = Logic HIGH, L = Logic LOW.
4. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
5. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_X$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH before the start of the write cycle to enable the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The read/write truth table for the CY7C1480V25 follows.[5]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	H	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – (DQ_C and DQP_C)	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – (DQ_D and DQP_D)	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Truth Table for Read/Write

The read/write truth table for the CY7C1482V25 follows.[5]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	L	H
Write Bytes B, A	H	L	L	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

Truth Table for Read/Write

The read/write truth table for the CY7C1486V25 follows.[8]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_X$
Read	H	H	X
Read	H	L	All $\overline{BW}$ = H
Write Byte x – (DQ_x and DQP_x)	H	L	L
Write All Bytes	H	L	All $\overline{BW}$ = L
Write All Bytes	L	X	X

Note

8. $\overline{BW}x$ represents any byte write signal $\overline{BW}$[0..7]. To enable any byte write $\overline{BW}x$, a Logic LOW signal must be applied at clock rise. Any number of byte writes can be enabled at the same time for any given write.

IEEE 1149.1 Serial Boundary Scan (JTAG)

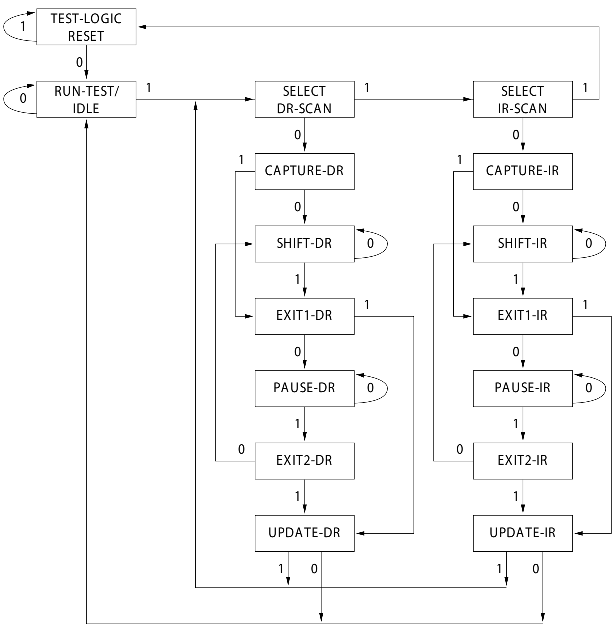
The CY7C1480V25/CY7C1482V25/CY7C1486V25 incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V or 1.8V I/O logic levels.

The CY7C1480V25/CY7C1482V25/CY7C1486V25 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent device clocking. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. At power up, the device comes up in a reset state, which does not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input gives commands to the TAP controller and is sampled on the rising edge of TCK. You can leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

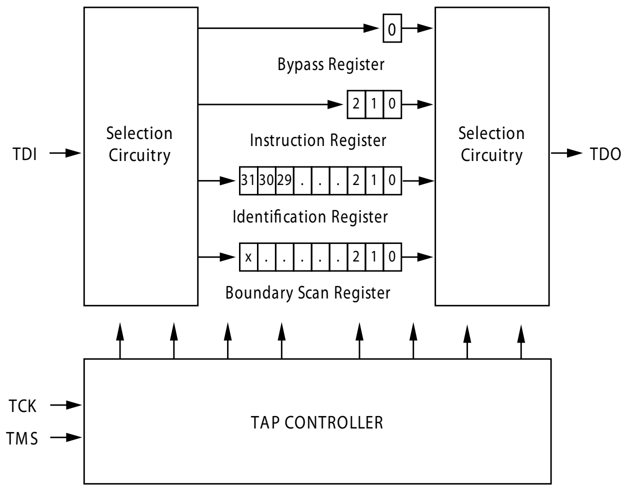
Test Data-In (TDI)

The TDI ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See TAP Controller Block Diagram.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See TAP Controller State Diagram.)

TAP Controller Block Diagram



Performing a TAP Reset

Perform a RESET by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the "TAP Controller Block Diagram" on page 12. At power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The x36 configuration has a 73-bit-long register, and the x18 configuration has a 54-bit-long register.

The boundary scan register is loaded with the contents of the RAM IO ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller moves to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the IO ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in "Identification Register Definitions" on page 15.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in "Identification Codes" on page 16. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the IO buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the IO ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction that is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is in a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

Be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that may be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that because the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR command.

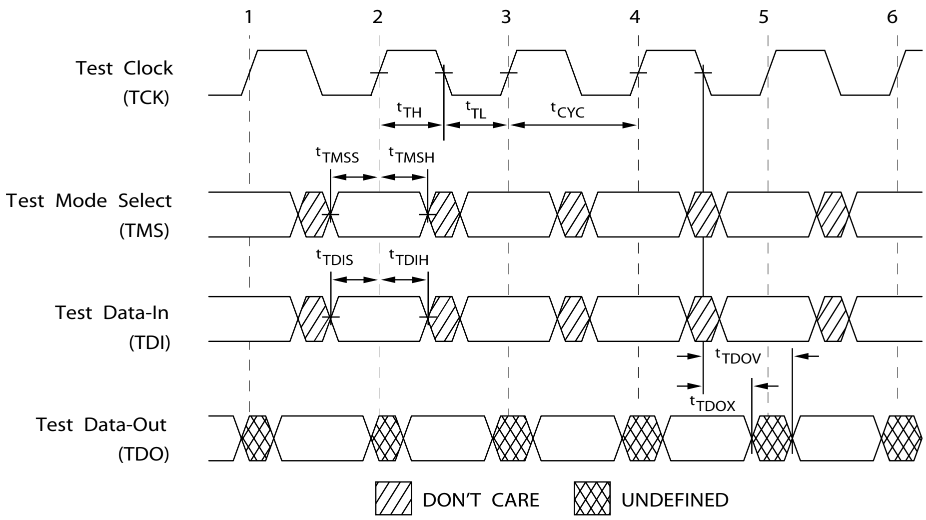
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP AC Switching Characteristics Over the Operating Range[9, 10]

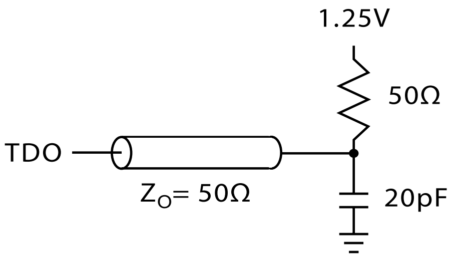
Parameter	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	20		ns
t_{TL}	TCK Clock LOW time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes
9. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
10. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

2.5V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 2.5V
Input rise and fall time .... 1 ns
Input timing reference levels 1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

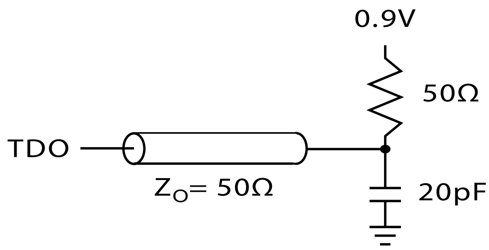
2.5V TAP AC Output Load Equivalent



1.8V TAP AC Test Conditions

Input pulse levels .... 0.2V to V_{DDQ} – 0.2
Input rise and fall time .... 1 ns
Input timing reference levels.. 0.9V
Output reference levels 0.9V
Test load termination supply voltage 0.9V

1.8V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operating Conditions

(0°C < T_A < +70°C; V_{DD} = 2.5V ±0.125V unless otherwise noted)[11]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{DDQ} = 2.5V	1.7		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 2.5V	2.1		V
			V_{DDQ} = 1.8V	1.6		V
V_{OL1}	Output LOW Voltage	I_{OL} = 1.0 mA	V_{DDQ} = 2.5V		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 2.5V		0.2	V
			V_{DDQ} = 1.8V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
			V_{DDQ} = 1.8V	1.26	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 2.5V	–0.3	0.7	V
			V_{DDQ} = 1.8V	–0.3	0.36	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA

Identification Register Definitions

Instruction Field	CY7C1480V25 (2M x36)	CY7C1482V25 (4M x 18)	CY7C1486V25 (1M x72)	Description
Revision Number (31:29)	000	000	000	Describes the version number
Device Depth (28:24)	01011	01011	01011	Reserved for internal use
Architecture/Memory Type(23:18)	000000	000000	000000	Defines memory type and architecture
Bus Width/Density(17:12)	100100	010100	110100	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	00000110100	Enables unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	1	1	Indicates the presence of an ID register

Note
11. All voltages referenced to V_{SS} (GND).

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)	Bit Size (x72)
Instruction	3	3	3
Bypass	1	1	1
ID	32	32	32
Boundary Scan Order – 165FBGA	73	54	-
Boundary Scan Order – 209BGA	-	-	112

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the IO ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures the IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the IO ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Boundary Scan Exit Order (2M x 36)

Bit #	165-Ball ID	Bit #	165-Ball ID	Bit #	165-Ball ID	Bit #	165-Ball ID
1	C1	21	R3	41	L10	61	B8
2	D1	22	P2	42	K11	62	A7
3	E1	23	R4	43	J11	63	B7
4	D2	24	P6	44	K10	64	B6
5	E2	25	R6	45	J10	65	A6
6	F1	26	N6	46	H11	66	B5
7	G1	27	P11	47	G11	67	A5
8	F2	28	R8	48	F11	68	A4
9	G2	29	P3	49	E11	69	B4
10	J1	30	P4	50	D10	70	B3
11	K1	31	P8	51	D11	71	A3
12	L1	32	P9	52	C11	72	A2
13	J2	33	P10	53	G10	73	B2
14	M1	34	R9	54	F10		
15	N1	35	R10	55	E10		
16	K2	36	R11	56	A10		
17	L2	37	N11	57	B10		
18	M2	38	M11	58	A9		
19	R1	39	L11	59	B9		
20	R2	40	M10	60	A8		

Boundary Scan Exit Order (4M x 18)

Bit #	165-Ball ID
1	D2
2	E2
3	F2
4	G2
5	J1
6	K1
7	L1
8	M1
9	N1
10	R1
11	R2
12	R3
13	P2
14	R4
15	P6
16	R6
17	N6
18	P11

Bit #	165-Ball ID
19	R8
20	P3
21	P4
22	P8
23	P9
24	P10
25	R9
26	R10
27	R11
28	M10
29	L10
30	K10
31	J10
32	H11
33	G11
34	F11
35	E11
36	D11

Bit #	165-Ball ID
37	C11
38	A11
39	A10
40	B10
41	A9
42	B9
43	A8
44	B8
45	A7
46	B7
47	B6
48	A6
49	B5
50	A4
51	B3
52	A3
53	A2
54	B2

Boundary Scan Exit Order (1M x 72)

Bit #	209-Ball ID
1	A1
2	A2
3	B1
4	B2
5	C1
6	C2
7	D1
8	D2
9	E1
10	E2
11	F1
12	F2
13	G1
14	G2
15	H1
16	H2
17	J1
18	J2
19	L1
20	L2
21	M1
22	M2
23	N1
24	N2
25	P1
26	P2
27	R2
28	R1
29	T1
30	T2
31	U1
32	U2
33	V1
34	V2
35	W1
36	W2
37	T6
38	V3
39	V4
40	U4
41	W5
42	V6
43	W6
44	U3
45	U9
46	V5
47	U5
48	U6
49	W7
50	V7
51	U7
52	V8
53	V9
54	W11
55	W10
56	V11
57	V10
58	U11
59	U10
60	T11
61	T10
62	R11
63	R10
64	P11
65	P10
66	N11
67	N10
68	M11
69	M10
70	L11
71	L10
72	P6
73	J11
74	J10
75	H11
76	H10
77	G11
78	G10
79	F11
80	F10
81	E10
82	E11
83	D11
84	D10
85	C11
86	C10
87	B11
88	B10
89	A11
90	A10
91	A9
92	U8
93	A7
94	A5
95	A6
96	D6
97	B6
98	D7
99	K3
100	A8
101	B4
102	B3
103	C3
104	C4
105	C8
106	C9
107	B9
108	B8
109	A4
110	C6
111	B7
112	A3

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ....–65°C to +150°C

Ambient Temperature with Power Applied...–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND........–0.3V to +3.6V

Supply Voltage on V_{DDQ} Relative to GND ......–0.3V to +V_{DD}

DC Voltage Applied to Outputs in Tri-State.. –0.5V to V_{DDQ} + 0.5V

DC Input Voltage ....–0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)...20 mA

Static Discharge Voltage.. >2001V (MIL-STD-883, Method 3015)

Latch Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V –5%/+5%	1.7V to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics Over the Operating Range[12, 13]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	IO Supply Voltage	for 2.5V IO		2.375	V_{DD}	V
		for 1.8V IO		1.7	1.9	V
V_{OH}	Output HIGH Voltage	for 2.5V IO, I_{OH} = –1.0 mA		2.0		V
		for 1.8V IO, I_{OH} = –100 µA		1.6		V
V_{OL}	Output LOW Voltage	for 2.5V IO, I_{OL} = 1.0 mA			0.4	V
		for 1.8V IO, I_{OL} = 100 µA			0.2	V
V_{IH}	Input HIGH Voltage[12]	for 2.5V IO		1.7	V_{DD} + 0.3V	V
		for 1.8V IO		1.26	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[12]	for 2.5V IO		–0.3	0.7	V
		for 1.8V IO		–0.3	0.36	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	4.0-ns cycle, 250 MHz		450	mA
			5.0-ns cycle, 200 MHz		450	mA
			6.0-ns cycle, 167 MHz		400	mA
I_{SB1}	Automatic CE Power Down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC}	4.0-ns cycle, 250 MHz		200	mA
			5.0-ns cycle, 200 MHz		200	mA
			6.0-ns cycle, 167 MHz		200	mA
I_{SB2}	Automatic CE Power Down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speeds		120	mA
I_{SB3}	Automatic CE Power Down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX} = 1/t_{CYC}	4.0-ns cycle, 250 MHz		200	mA
			5.0-ns cycle, 200 MHz		200	mA
			6.0-ns cycle, 167 MHz		200	mA
I_{SB4}	Automatic CE Power Down Current—TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speeds		135	mA

Notes

12. Overshoot: V_{IH}(AC) < V_{DD} +1.5V (Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC) > –2V (Pulse width less than t_{CYC}/2).
13. Power up: Assumes a linear ramp from 0V to V_{DD}(min.) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance[14]

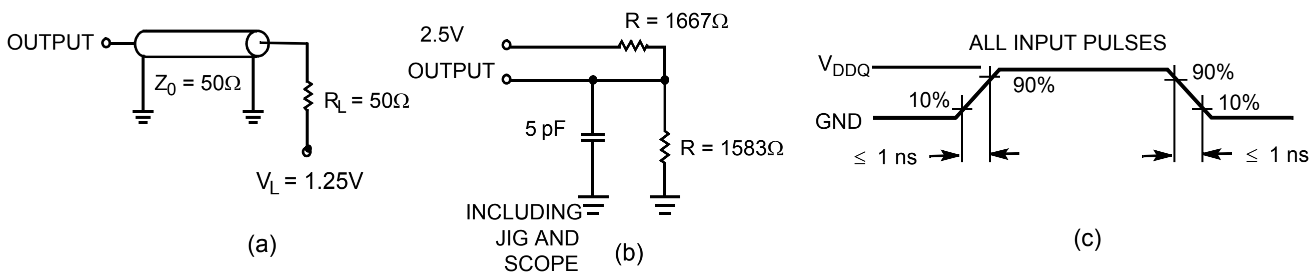
Parameter	Description	Test Conditions	100 TQFP Package	165 FBGA Package	209 FBGA Package	Unit
$C_{ADDRESS}$	Address Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 2.5V V_{DDQ} = 2.5V	6	6	6	pF
C_{DATA}	Data Input Capacitance		5	5	5	pF
C_{CTRL}	Control Input Capacitance		8	8	8	pF
C_{CLK}	Clock Input Capacitance		6	6	6	pF
$C_{I/O}$	Input/Output Capacitance		5	5	5	pF

Thermal Resistance[14]

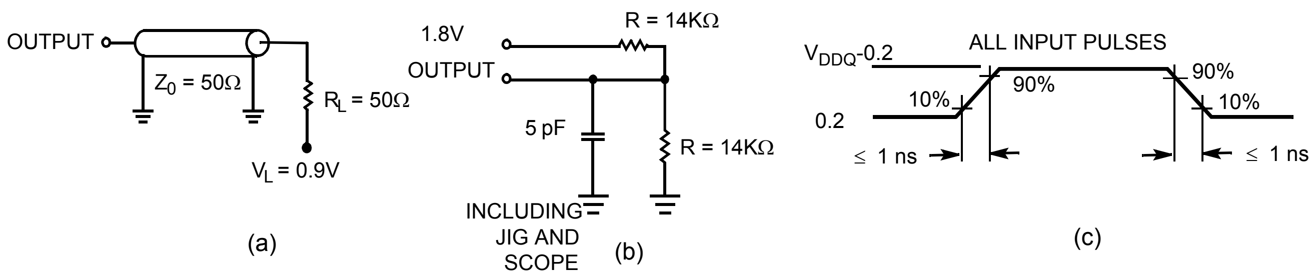
Parameter	Description	Test Conditions	100 TQFP Max.	165 FBGA Max.	209 FBGA Max.	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	24.63	16.3	15.2	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		2.28	2.1	1.7	°C/W

AC Test Loads and Waveforms

2.5V I/O Test Load



1.8V I/O Test Load



Note
14. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics Over the Operating Range[15, 16]

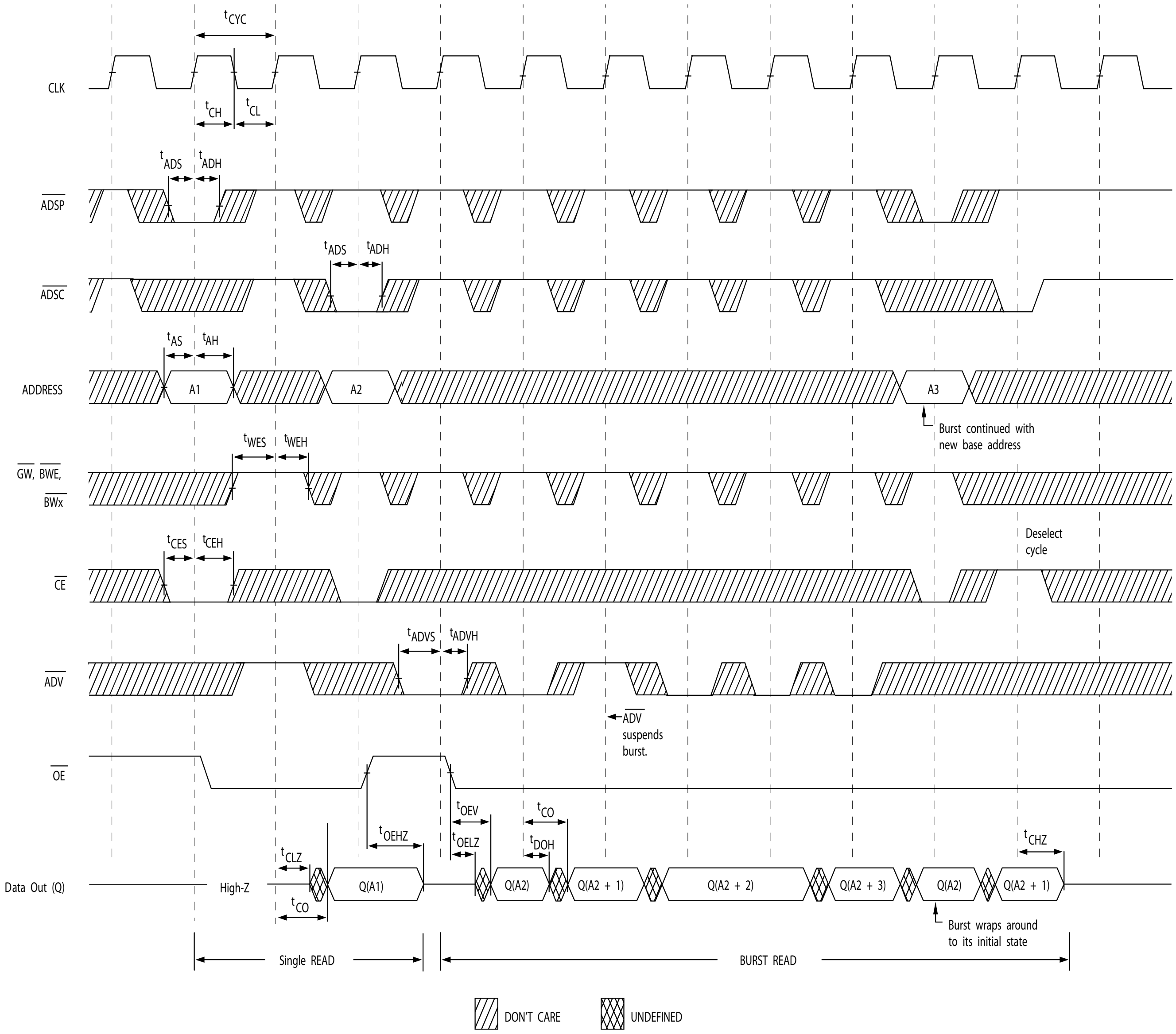
Parameter	Description	250 MHz		200 MHz		167 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{POWER}	V_{DD}(Typical) to the first access[17]	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	4.0		5.0		6.0		ns
t_{CH}	Clock HIGH	2.0		2.0		2.4		ns
t_{CL}	Clock LOW	2.0		2.0		2.4		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise		3.0		3.0		3.4	ns
t_{DOH}	Data Output Hold After CLK Rise	1.3		1.3		1.5		ns
t_{CLZ}	Clock to Low-Z[18, 19, 20]	1.3		1.3		1.5		ns
t_{CHZ}	Clock to High-Z[18, 19, 20]		3.0		3.0		3.4	ns
t_{OEV}	$\overline{\text{OE}}$ LOW to Output Valid		3.0		3.0		3.4	ns
t_{OELZ}	$\overline{\text{OE}}$ LOW to Output Low-Z[18, 19, 20]	0		0		0		ns
t_{OEHZ}	$\overline{\text{OE}}$ HIGH to Output High-Z[18, 19, 20]		3.0		3.0		3.4	ns
Setup Times								
t_{AS}	Address Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{ADS}	$\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$ Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{ADVS}	$\overline{\text{ADV}}$ Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{WES}	$\overline{\text{GW}}$, $\overline{\text{BWE}}$, $\overline{\text{BW}}_X$ Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{DS}	Data Input Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.4		1.4		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.4		0.4		0.5		ns
t_{ADH}	$\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ Hold After CLK Rise	0.4		0.4		0.5		ns
t_{ADVH}	$\overline{\text{ADV}}$ Hold After CLK Rise	0.4		0.4		0.5		ns
t_{WEH}	$\overline{\text{GW}}$, $\overline{\text{BWE}}$, $\overline{\text{BW}}_X$ Hold After CLK Rise	0.4		0.4		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.4		0.4		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.4		0.4		0.5		ns

Notes

15. Timing reference level is 1.25V when V_{DDQ} = 2.5V and is 0.9V when V_{DDQ} = 1.8V.
16. Test conditions shown in (a) of “AC Test Loads and Waveforms” on page 20 unless otherwise noted.
17. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially before a read or write operation can be initiated.
18. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads and Waveforms. Transition is measured ±200 mV from steady-state voltage.
19. At any possible voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z before Low-Z under the same system conditions.
20. This parameter is sampled and not 100% tested.

Switching Waveforms

Read Cycle Timing[21]

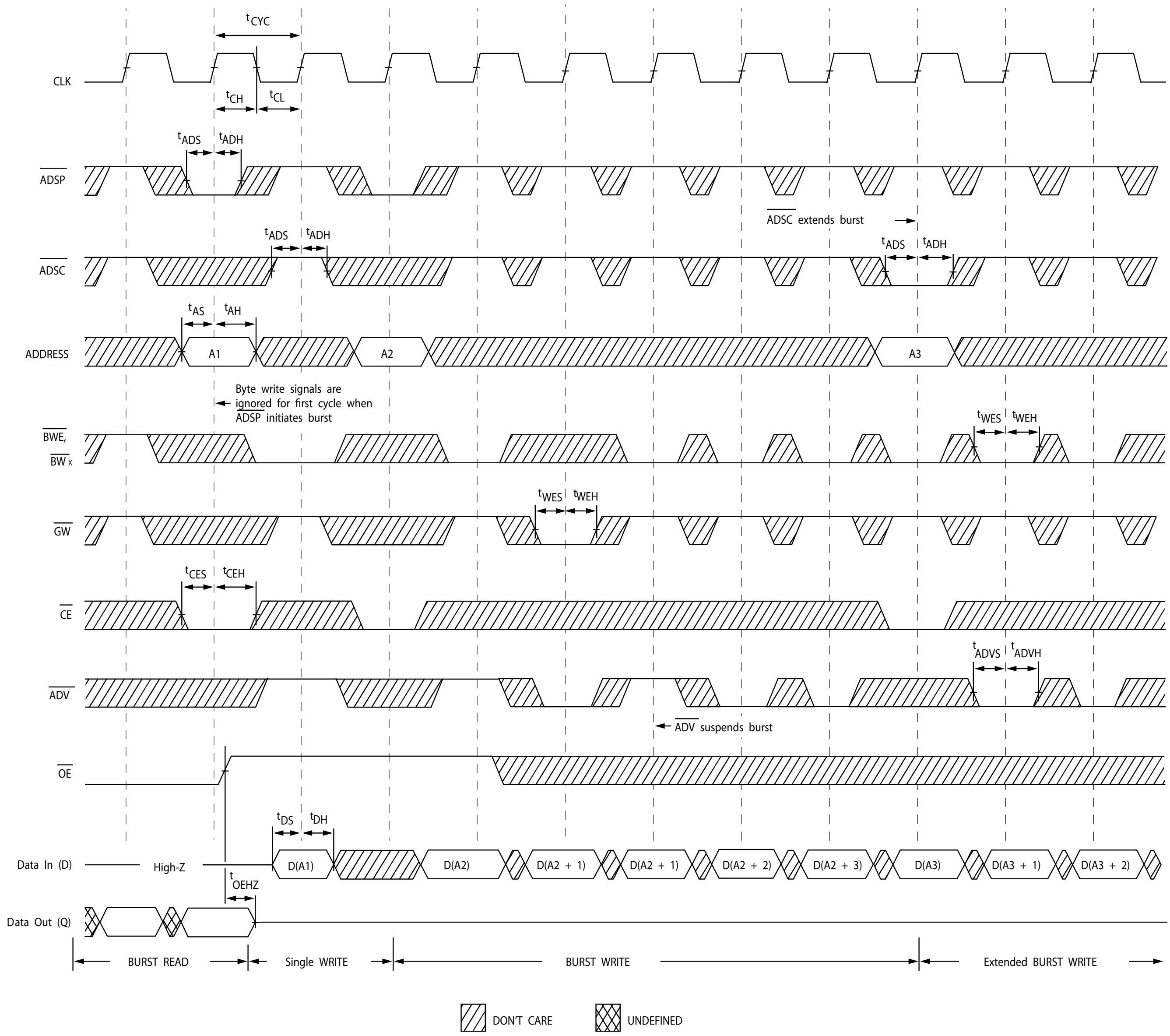


Note

21. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms (continued)

Write Cycle Timing[21, 22]

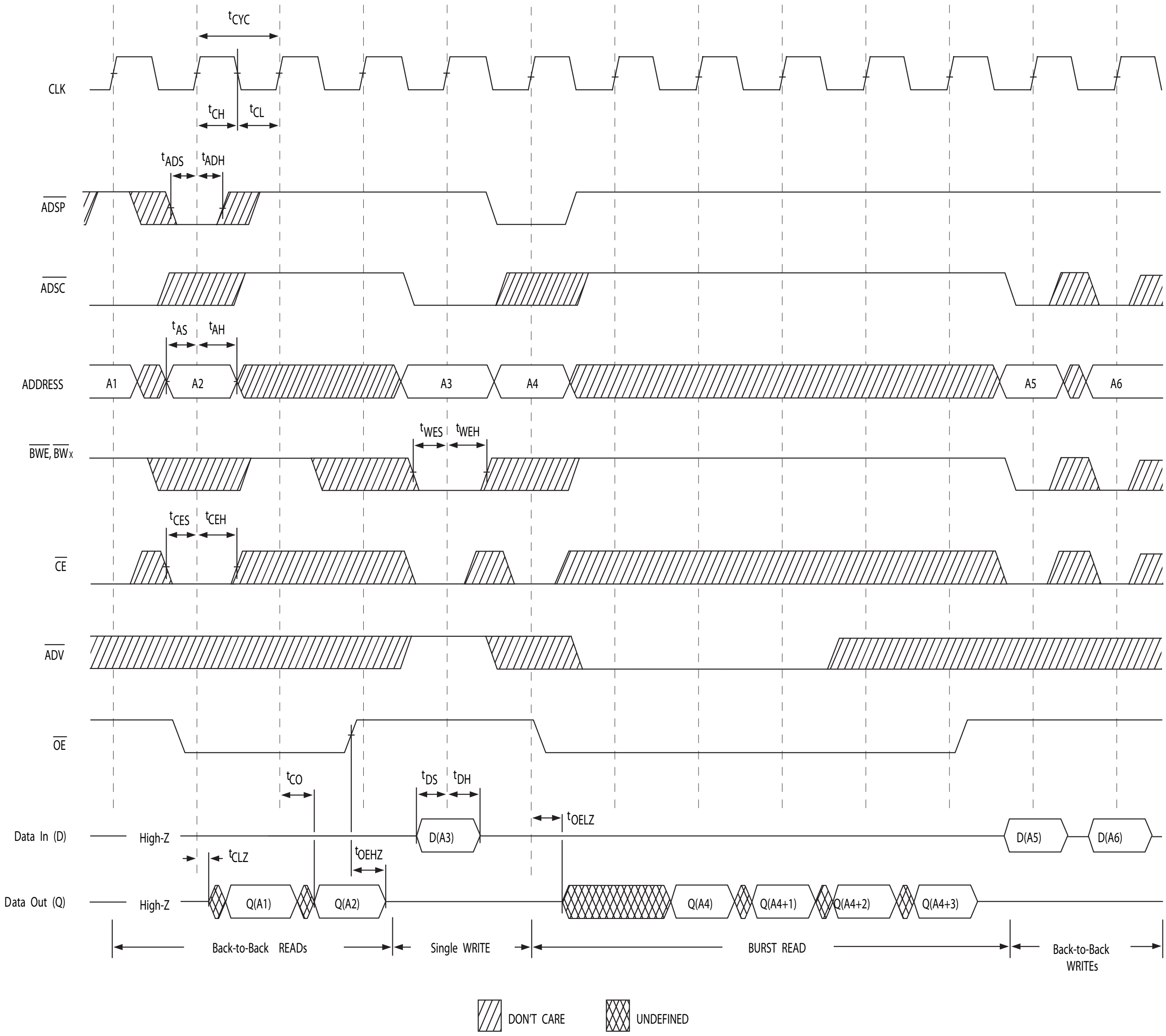


Note

22. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW_X}$ LOW.

Switching Waveforms (continued)

Read/Write Cycle Timing[21, 23, 24]

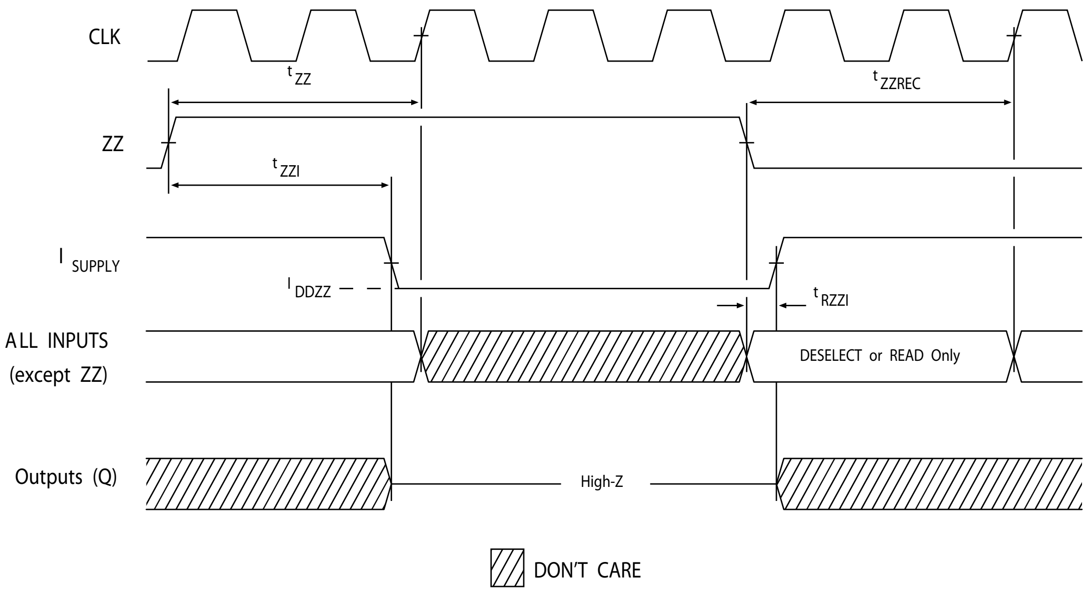


Notes

23. The data bus (Q) remains in high-Z following a write cycle, unless a new read access is initiated by $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$.
24. $\overline{\text{GW}}$ is HIGH.

Switching Waveforms (continued)

ZZ Mode Timing[25, 26]



Notes

25. Device must be deselected when entering ZZ mode. See "Truth Table" on page 10 for all possible signal conditions to deselect the device.
26. DQs are in high-Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1480V25-167AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1482V25-167AXC			
	CY7C1480V25-167BZC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1482V25-167BZC			
	CY7C1480V25-167BZXC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1482V25-167BZXC			
	CY7C1486V25-167BGC	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1486V25-167BGXC		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
	CY7C1480V25-167AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1482V25-167AXI			
	CY7C1480V25-167BZI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1482V25-167BZI			
	CY7C1480V25-167BZXI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1482V25-167BZXI			
	CY7C1486V25-167BGI	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1486V25-167BGXI		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
200	CY7C1480V25-200AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1482V25-200AXC			
	CY7C1480V25-200BZC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1482V25-200BZC			
	CY7C1480V25-200BZXC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1482V25-200BZXC			
	CY7C1486V25-200BGC	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1486V25-200BGXC		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
	CY7C1480V25-200AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1482V25-200AXI			
	CY7C1480V25-200BZI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1482V25-200BZI			
	CY7C1480V25-200BZXI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1482V25-200BZXI			
	CY7C1486V25-200BGI	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1486V25-200BGXI		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	

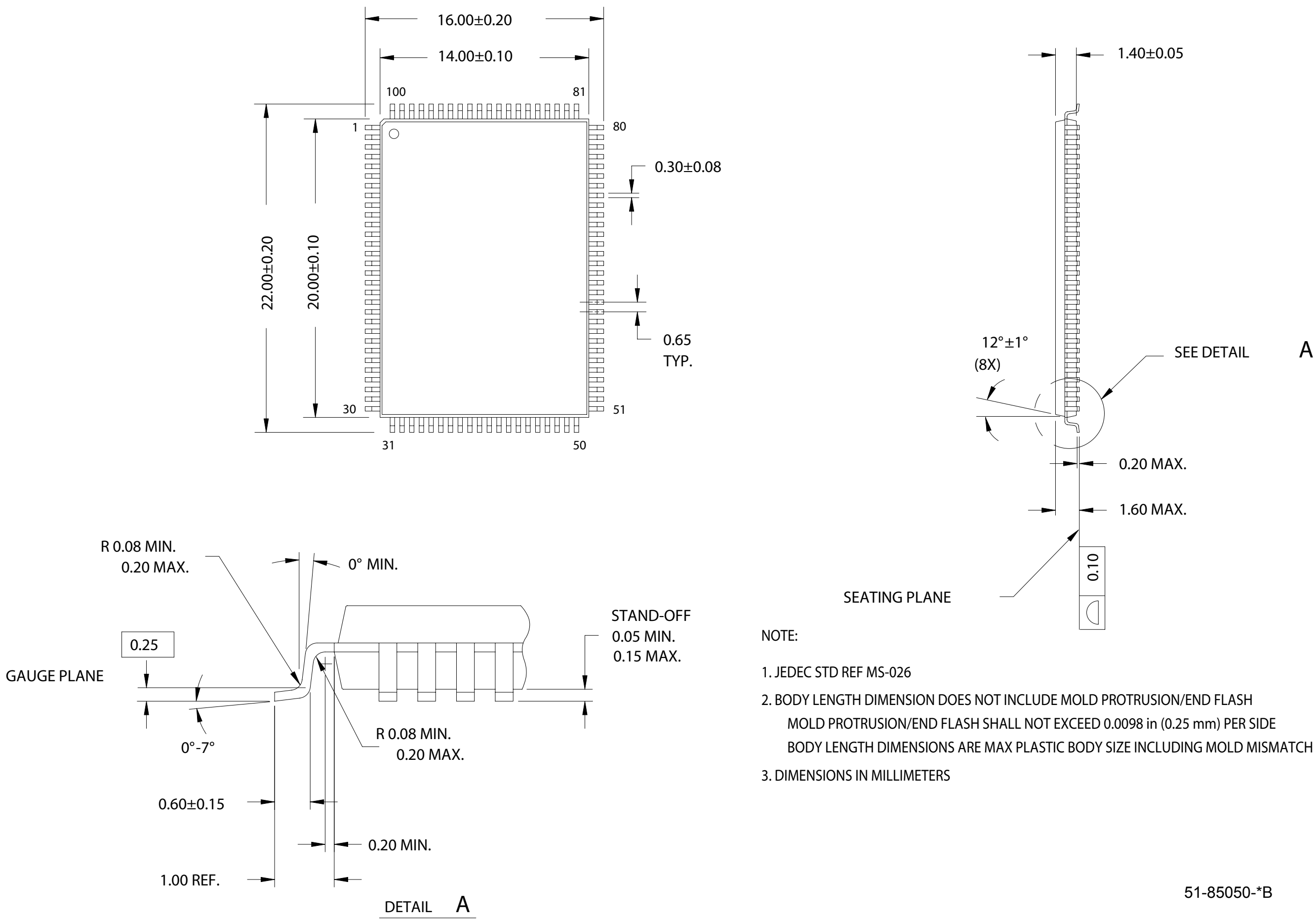
Ordering Information (continued)

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
250	CY7C1480V25-250AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Commercial
	CY7C1482V25-250AXC			
	CY7C1480V25-250BZC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1482V25-250BZC			
	CY7C1480V25-250BZXC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Lead-Free	
	CY7C1482V25-250BZXC			
	CY7C1486V25-250BGC	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1486V25-250BGXC		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Lead-Free	
	CY7C1480V25-250AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free	Industrial
	CY7C1482V25-250AXI			
	CY7C1480V25-250BZI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1482V25-250BZI			
	CY7C1480V25-250BZXI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Lead-Free	
	CY7C1482V25-250BZXI			
	CY7C1486V25-250BGI	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1486V25-250BGXI		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Lead-Free	

Package Diagrams

Figure 1. 100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm), 51-85050



NOTE:

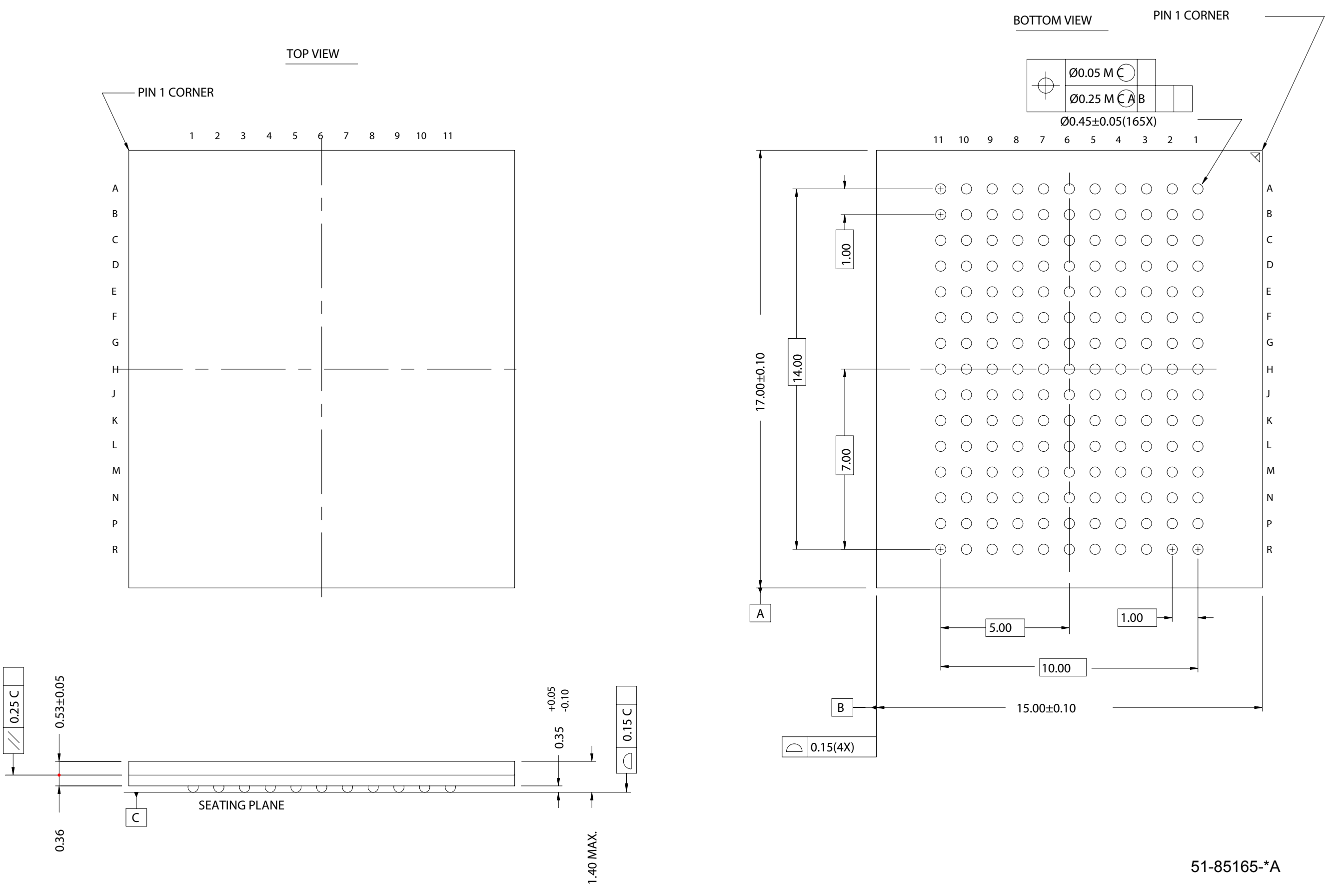
1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

[+] Feedb

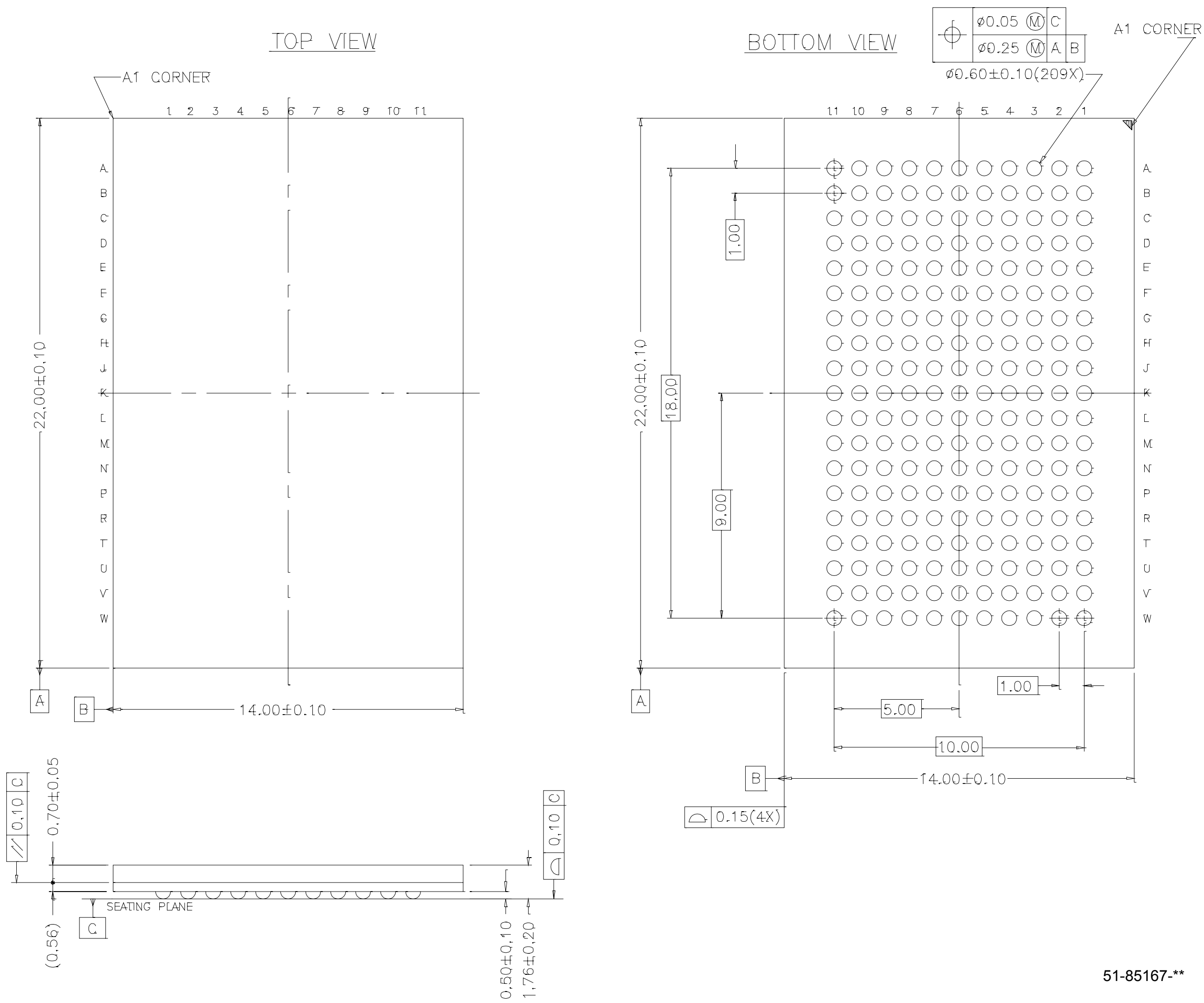
Package Diagrams (continued)

Figure 2. 165-Ball FBGA (15 x 17 x 1.4 mm), 51-85165



Package Diagrams (continued)

Figure 3. 209-Ball FBGA (14 x 22 x 1.76 mm), 51-85167



i486 is a trademark and Intel and Pentium are registered trademarks of Intel Corporation. All products and company names mentioned in this document may be the trademarks of their respective holders.

Document History Page

Document Title: CY7C1480V25/CY7C1482V25/CY7C1486V25 72-Mbit (2M x 36/4M x 18/1M x 72) Pipelined Sync SRAM Document Number: 38-05282				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114670	08/06/02	PKS	New Data Sheet
*A	118281	01/21/03	HGK	Changed t_{CO} from 2.4 to 2.6 ns for 250 MHz Updated features on page 1 for package offering Removed 300 MHz offering Updated Ordering Information Changed Advanced Information to Preliminary
*B	233368	See ECN	NJY	Changed timing diagrams Changed logic block diagrams Modified Functional Description Modified “Functional Overview” section Added boundary scan order for all packages Included thermal numbers and capacitance values for all packages Included IDD and ISB values Removed 250-MHz speed grade offering and included 225 MHz speed bin Changed package outline for 165FBGA package and 209-ball BGA package Removed 119-BGA package offering
*C	299452	See ECN	SYT	Removed 225-MHz offering and included 250-MHz speed bin Changed t_{CYC} from 4.4 ns to 4.0 ns for 250-MHz Speed Bin Changed Θ_{JA} from 16.8 to 24.63 °C/W and Θ_{JC} from 3.3 to 2.28 °C/W for 100 TQFP Package on Page # 20 Added lead-free information for 100-Pin TQFP, 165 FBGA and 209 BGA Packages Added comment of ‘Lead-free BG packages availability’ below the Ordering Information
*D	323039	See ECN	PCI	Unshaded 200 and 167 MHz speed bin in the AC/DC Table and Selection Guide Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard Added Address Expansion pins in the Pin Definitions Table Added Truth Table and Note# 7 for CY7C1486V25 on page# 11 Modified V_{OL}, V_{OH} Test Conditions Added Industrial temperature range Removed comment of ‘Lead-free BG packages availability’ below the Ordering Information Updated Ordering Information Table
*E	416193	See ECN	NXR	Converted from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Changed the description of I_X from Input Load Current to Input Leakage Current on page# 19 Changed the I_X current values of MODE on page # 19 from -5 µA and 30 µA to -30 µA and 5 µA Changed the I_X current values of ZZ on page # 19 from -30 µA and 5 µA to -5 µA and 30 µA Changed $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ on page # 19 Replaced Package Name column with Package Diagram in the Ordering Information table Updated the Ordering Information Table
*F	470723	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND Changed t_{TH}, t_{TL} from 25 ns to 20 ns and t_{TDOV} from 5 ns to 10 ns in TAP AC Switching Characteristics table Updated the Ordering Information table

Document Title: CY7C1480V25/CY7C1482V25/CY7C1486V25 72-Mbit (2M x 36/4M x 18/1M x 72) Pipelined Sync SRAM Document Number: 38-05282				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*G	486690	See ECN	VKN	Corrected the typo in the 209-Ball FBGA pinout. (Corrected the ball name H9 to V_{SS} from V_{SSQ}).
*H	1026720	See ECN	VKN/KKVTMP	Added footnote #2 related to V_{SSQ}