AOT424

N-Channel Enhancement Mode Field Effect Transistor

General Description

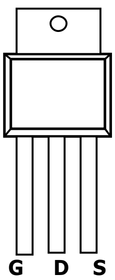
The AOT424 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. This device is ideally suited for use as a low side switch in CPU core power conversion.

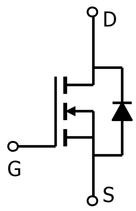
Standard Product AOT424 is Pb-free (meets ROHS & Sony 259 specifications).

Features

V_{DS} (V) = 30V
I_D = 110A (V_{GS} = 10V)
$R_{DS(ON)}$ < 4mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 5.5mΩ (V_{GS} = 4.5V)

TO-220





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B,G]	T_C=25°C [G]	I_D	110	A
	T_C=100°C [B]		88	
Pulsed Drain Current		I_{DM}	200	
Avalanche Current [C]		I_{AR}	30	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	112	mJ
Power Dissipation [B]	T_C=25°C	P_D	100	W
	T_C=100°C		50	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	14.2	20	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		39	50	°C/W
Maximum Junction-to-Case [C]	Steady-State	$R_{\theta JC}$	0.8	1.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	2	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	110			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=30A		3	4	mΩ
		T_J=125°C		4.7	6	
		V_{GS}=4.5V, I_D=30A		4.3	5.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=30A		106		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.72	1	V
I_S	Maximum Body-Diode Continuous Current				85	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		3700	4400	pF
C_{oss}	Output Capacitance			700		pF
C_{rss}	Reverse Transfer Capacitance			390		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.54	0.7	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=30A		59.6	72	nC
Q_g(4.5V)	Total Gate Charge			30.4	37	nC
Q_{gs}	Gate Source Charge			9.5		nC
Q_{gd}	Gate Drain Charge			19.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.5Ω, R_{GEN}=3Ω		12.5		ns
t_r	Turn-On Rise Time			35.5		ns
$t_{D(off)}$	Turn-Off DelayTime			40		ns
t_f	Turn-Off Fall Time			32.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=30A, dI/dt=100A/µs		35.3	42	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=30A, dI/dt=100A/µs		30.7		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on steady-state $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature fo 175°C may be used if the PCB or heatsink allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The R $_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by the package current capability.

Rev4: July 2008

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTIC[S]

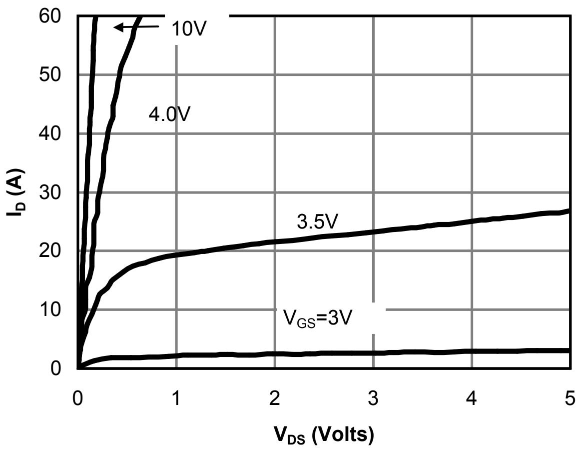


Fig 1: On-Region Characteristics

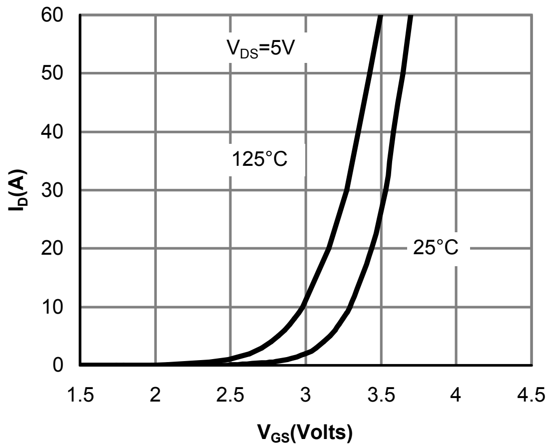


Figure 2: Transfer Characteristics

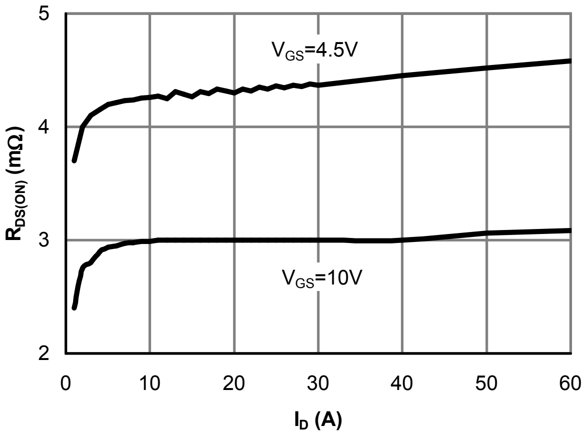


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

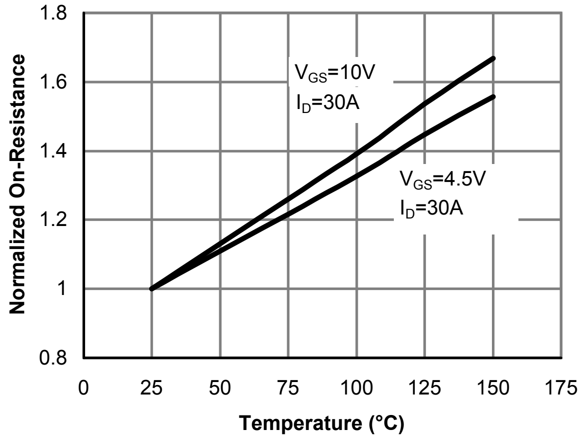


Figure 4: On-Resistance vs. Junction Temperature

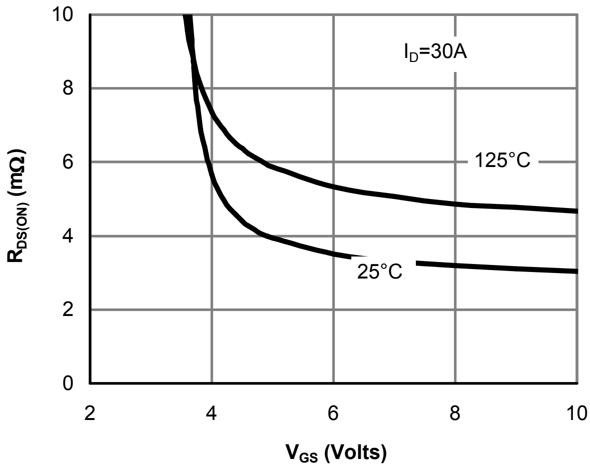


Figure 5: On-Resistance vs. Gate-Source Voltage

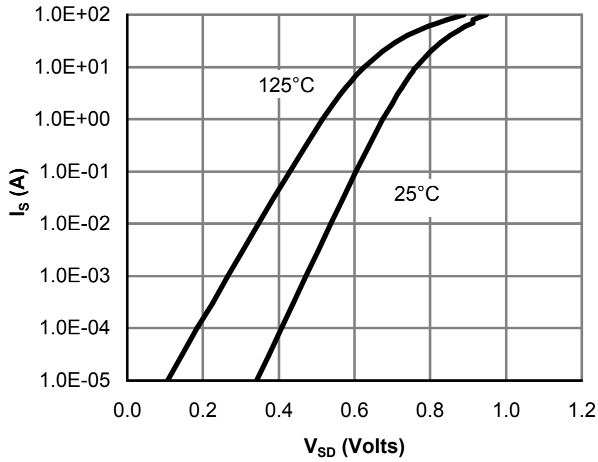


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

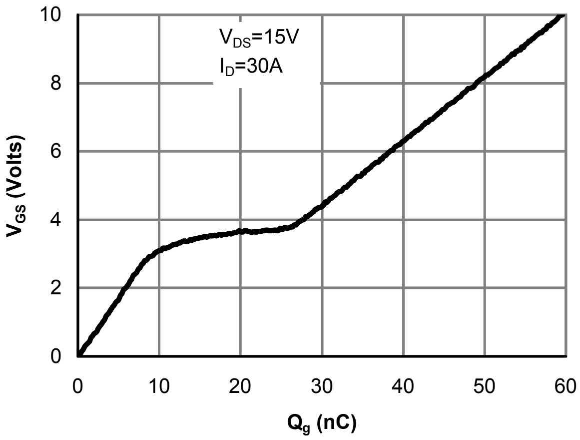


Figure 7: Gate-Charge Characteristics

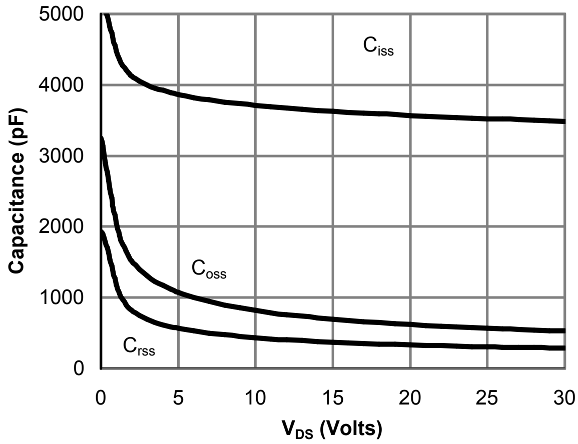


Figure 8: Capacitance Characteristics

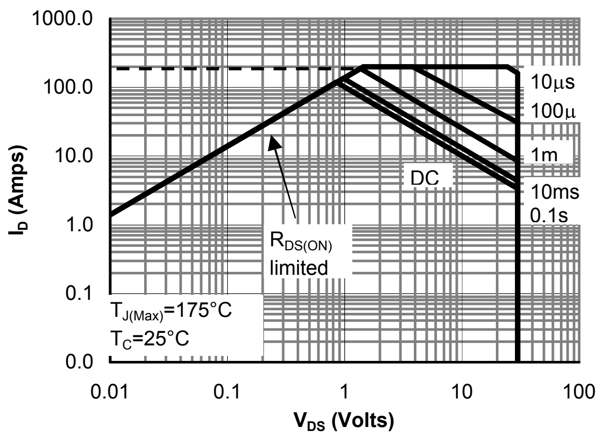


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

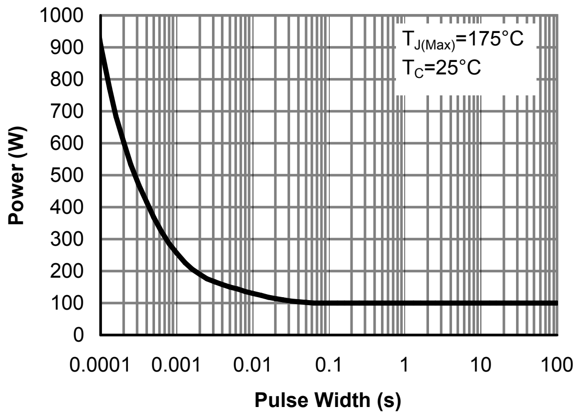


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

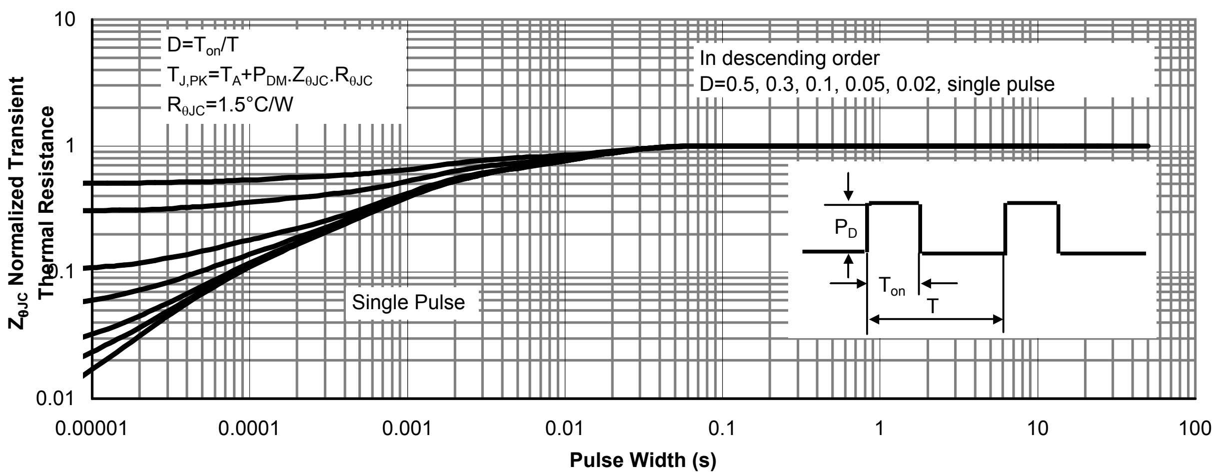


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)