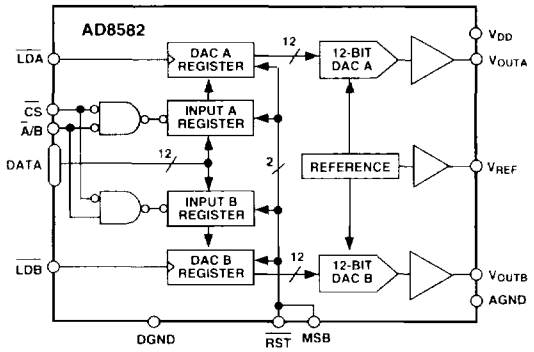
# +5 Volt, Parallel Input Complete Dual 12-Bit DAC

# AD8582

**FEATURES**
**Complete Dual 12-Bit DAC**
**No External Components**
**Single +5 Volt Operation**
**1 mV/Bit with 4.095 V Full Scale**
**True Voltage Output, ±5 mA Drive**
**Very Low Power: 5 mW**

**APPLICATIONS**
**Digitally Controlled Calibration**
**Portable Equipment**
**Servo Controls**
**Process Control Equipment**
**PC Peripherals**

**FUNCTIONAL BLOCK DIAGRAM**

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## GENERAL DESCRIPTION

The AD8582 is a complete, parallel input, dual 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DACs, are a rail-to-rail amplifier, latch and reference. The reference ($V_{REF}$) is trimmed to 2.5 volts output, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The AD8582 is coded natural binary. The op amp output swings from 0 volt to +4.095 volts for a one-millivolt-per-bit resolution, and is capable of driving ± 5 mA. Operation down to 4.3 V is possible with output load currents less than 1 mA.

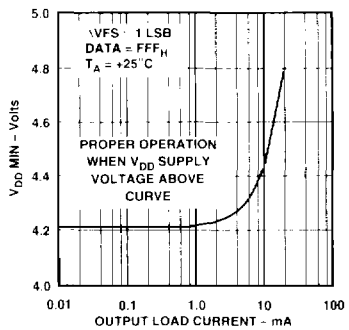


*Figure 1. Minimum Supply Voltage vs. Load*

The high speed parallel data interface connects to the fastest processors without wait states. The double-buffered input structure allows the user to load the input registers one at a time, then a single load strobe tied to both LDA + LDB inputs will update both DAC outputs simultaneously. LDA and LDB can also be activated independently to immediately update their respective DAC registers. An address input decodes DAC A or DAC B when the chip select $\overline{CS}$ input is strobed. An asynchronous reset input sets the output to zero scale. The MSB bit can be used to establish a preset to midscale when the reset input is strobed.

The AD8582 is available in the 24-pin plastic DIP and the surface mount SOIC-24. Each part is fully specified for operation over -40°C to +85°C, and the full +5 V ± 5% power supply range.

**ORDERING INFORMATION[1]**

| Model | Temperature Range | Package Description | Package Option[2] |
|---|---|---|---|
| AD8582AN | -40°C to +85°C | 24-Pin Plastic DIP | N-24 |
| AD8582AR | -40°C to +85°C | 24-Lead SOIC | SOL-24 |
| AD8582CHIPS | +25°C | Die | |

NOTES
[1]For die specifications contact your local Analog Devices sales office. The AD8582 contains 1270 transistors.
[2]For outline information see Package Information section.

# AD8582–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_{DD}$ = +5.0 V ± 5%, $R_L$ = No Load, −40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted)

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| STATIC PERFORMANCE | | | | | | |
| Resolution | N | Note 1 | 12 | | | Bits |
| Relative Accuracy | INL | | 2 | ±3/4 | +2 | LSB |
| Differential Nonlinearity | DNL | Monotonic | 1 | ±3/4 | +1 | LSB |
| Zero-Scale Error | $V_{ZSE}$ | Data = $000_H$ | | +0.2 | +3 | mV |
| Full-Scale Voltage | $V_{FS}$ | Data = $FFF_H$[2] | 4.079 | 4.095 | 4.111 | V |
| Full-Scale Tempco | $TCV_{FS}$ | Notes 2 and 3 | | ±16 | | ppm/°C |
| MATCHING PERFORMANCE | | | | | | |
| Linearity Matching Error | $\Delta V_{FS}A/B$ | | | ±1 | | LSB |
| REFERENCE OUTPUT | | | | | | |
| Output Voltage | $V_{REF}$ | | 2.484 | 2.500 | 2.516 | V |
| Output Source Current | $I_{REF}$ | Note 4 | | | −5 | mA |
| Line Rejection | $LN_{REF}$ | | | | 0.08 | %/V |
| Load Regulation | $LD_{REF}$ | $I_{REF}$ = 0 mA to 5 mA | | | 0.1 | %/mA |
| ANALOG OUTPUT | | | | | | |
| Output Current | $I_{OUT}$ | Data = $800_H$ | | | ±5 | mA |
| Load Regulation at Half Scale | $LD_{REG}$ | $R_L$ = 402 Ω to ∞, Data = $800_H$ | | 1 | 3 | LSB |
| Capacitive Load | $C_L$ | No Oscillation[5] | | 500 | | pF |
| DYNAMIC CHARACTERISTICS[6] | | | | | | |
| Crosstalk | $C_T$ | | | >64 | | dB |
| Voltage Output Settling Time[5] | $t_S$ | To ±1 LSB of Final Value | | 16 | | µs |
| Digital Feedthrough | $F_T$ | Signal Measured at DAC Output, While Changing Data ($\overline{LDA}$ = $\overline{LDB}$ = "1") | | 35 | | nV s |
| LOGIC INPUTS | | | | | | |
| Logic Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Logic Input High Voltage | $V_{IH}$ | | 2.4 | | | V |
| Input Leakage Current | $I_{IL}$ | | | | 10 | µA |
| Input Capacitance | $C_{IL}$ | Note 3 | | | 10 | pF |
| TIMING SPECIFICATIONS[3,6] | | | | | | |
| Chip Select Pulse Width | $t_{CSW}$ | | 30 | | | ns |
| DAC Select Setup | $t_{AS}$ | | 30 | | | ns |
| DAC Select Hold | $t_{AH}$ | | 0 | | | ns |
| Data Setup | $t_{DS}$ | | 30 | | | ns |
| Data Hold | $t_{DH}$ | | 10 | | | ns |
| Load Setup | $t_{LS}$ | | 20 | | | ns |
| Load Hold | $t_{LH}$ | | 10 | | | ns |
| Load Pulse Width | $t_{LDW}$ | | 20 | | | ns |
| Reset Pulse Width | $t_{RSW}$ | | 30 | | | ns |
| SUPPLY CHARACTERISTICS | | | | | | |
| Positive Supply Current | $I_{DD}$ | $V_{IH}$ = 2.4 V, $V_{IL}$ = 0.8 V | | 4 | 7 | mA |
| | | $V_{IL}$ = 0 V, $V_{DD}$ = +5 V | | 1 | 2 | mA |
| Power Dissipation[7] | $P_{DISS}$ | $V_{IH}$ = 2.4 V, $V_{IL}$ = 0.8 V | | 20 | 35 | mW |
| | | $V_{IL}$ = 0 V, $V_{DD}$ = +5 V | | 5 | 10 | mW |
| Power Supply Sensitivity | PSS | $\Delta V_{DD}$ = ±5% | | 0.002 | 0.004 | %/% |

NOTES

[1] 1 LSB = 1 mV for 0 V to +4.095 V output range.

[2] Includes internal voltage reference error.

[3] These parameters are guaranteed by design and not subject to production testing.

[4] Very little sink current is available at the $V_{REF}$ pin. Use external buffer if setting up a virtual ground.

[5] Settling time is not guaranteed for the first six codes 0 through 5.

[6] All input control signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[7] Power dissipation is a calculated value $I_{DD}$ × 5 V.

Specifications subject to change without notice.