REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27						

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-05-14

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-93006
A	67268	

SHEET 1 OF 27

DESC FORM 193
JUL 91

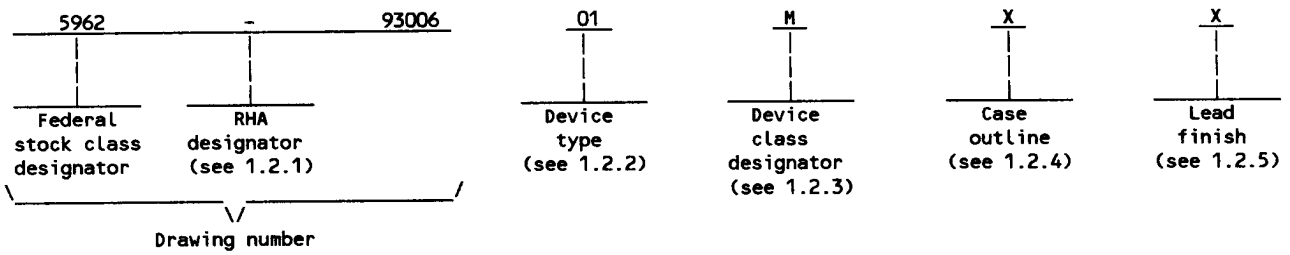
5962-E273-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320E14	Digital signal processor

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-P68	68	Pin grid array 1/
Y	CQCC2-J68	68	J-leaded chip carrier

1/ This package is inactive for new design.

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) 2/	-0.3 V dc to + 7.0 V dc
Supply voltage range (V_{PP}) 2/	-0.6 V dc to +14.0 V dc
DC input voltage range (V_{IN})	-0.3 V dc to +14.0 V dc
DC output voltage range (V_{OUT})	-0.3 V dc to + 7.0 V dc
Continuous power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-ambient (Θ_{JA})	
Case X	36°C/W
Case Y	50°C/W
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	
Operating voltage	+4.5 V dc to +5.5 V dc
Fast programming	+5.75 V dc to +6.25 V dc
Supply voltage range for fast programming 3/ (V_{PP})	+12.25 V dc to +12.75 V dc
Supply voltage (V_{SS})	+0.0 V dc
Minimum high level input voltage (V_{IH})	
CLKIN, CAP0, CAP1, CMP4/CAP2, CMP5/CAP3, $\overline{RS}$	+3.0 V dc
IOP0-IOP15	+2.4 V dc
D0-D15, INT, NMI/MC/MP, RXD, TXD, TCLK1/CLK, TCLK2/CLKX	+2.0 V dc
Maximum low level input voltage (V_{IL})	
CAP0-CAP5	+0.6 V
All other inputs	+0.8 V
Maximum high level output current (I_{OH})	-300 µA
Maximum low level output current (I_{OL})	+2 mA
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	4/ percent

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to V_{SS}.
3/ V_{PP} can be applied only to programming pins designed to accept V_{PP} as an input. During programming the total supply current is $I_{PP} + I_{CC}$.
4/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block Diagram. The block diagram shall be as specified on figure 2.

3.2.4 Waveforms. The waveforms shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 Processing EPROM's. All testing requirements and quality assurance provisions herein shall be serialized in accordance with MIL-M-38510.

3.12.1 Erasure of EPROM's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.12.2 Programmability of EPROM's. When specified, devices shall be programmed to the specifed pattern using the procedures and characteristics specified in 4.6 and table III.

3.12.3 Verification of erasure of programmability of EPROM's. When specified, devices shall be verified as either programmed to the specifed pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level output voltage	V_{OH}	$V_{CC} = 4.5\ V$, $I_{OH} = -300\ \mu A$		1,2,3	01	2.4		V
		$V_{CC} = 4.5\ V$, $I_{OH} = 20\ \mu A$ 2/ 3/				$V_{CC} - 0.4$		
Low-level output voltage	V_{OL}	$V_{CC} = 4.5\ V$, $I_{OL} = 2\ mA$		1,2,3	01		0.6	V
Off-state output current	I_{OZ}	$V_{CC} = 5.5\ V$	$V_O = 2.4\ V$	1,2,3	01		20	μA
			$V_O = 0.4\ V$				-20	
Input current	I_I	$V_I = V_{SS}$ to V_{CC}, $V_{CC} = 5.5\ V$	CLKIN	1,2,3	01		±50	μA
			All other inputs				±20	
Supply current 4/	I_{CC}	$f = 20.5\ MHz$, $V_{CC} = 5.5\ V$		1,2,3	01		90	mA
V_{PP} supply current	I_{PP1}	$V_{PP} = 5.5\ V$, $V_{CC} = 5.5\ V$		1,2,3	01		100	μA
V_{PP} supply current (during program pulse)	I_{PP2}	$V_{PP} = 13\ V$		1,2,3	01		50	mA
Input capacitance	C_{IN}	See 4.4.1c		4	01		25	pF
Output capacitance	C_{OUT}	See 4.4.1c		4	01		25	pF
Input/output capacitance	$C_{I/O}$	See 4.4.1c		4	01		35	pF
Functional test		See 4.4.1b		7, 8	01			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External clock requirements							
Input clock frequency	CLKIN	V_{CC} = 4.5 V See figure 3	9,10,11	01	6.7	20.5	MHz
Clock timing							
CLKOUT cycle time 5/	$t_{c(C)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	195	600	ns
Delay time CLKIN↑ to CLKOUT↓	$t_{d(MCC)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		60	ns
Master clock cycle time 5/	$t_{c(MC)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	48.75	150	ns
Rise time, master clock input 3/	$t_{r(MC)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		10	ns
Fall time, master clock input 3/	$t_{f(MC)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		10	ns
Pulse duration, master clock 3/	$t_{w(MCP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.45 $t_{c(MC)}$	0.55 $t_{c(MC)}$	ns
Pulse duration, master clock low 3/	$t_{w(MCL)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		82.5	ns
Pulse duration, master clock high 3/	$t_{w(MCH)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		82.5	ns
Memory read and instruction timing							
Setup time, address bus valid before REN↓	$t_{su(A)R}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.25 $t_{c(C)}$-45		ns
Setup time, address bus valid before WE↓	$t_{su(A)W}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.50 $t_{c(C)}$-45		ns
Hold time, address bus valid after REN↑ or WE↑ 3/	$t_{h(A)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable time, data starts being driven before WE↓ 3/	$t_{en(D)W}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		0.25 $t_{c(C)}$	ns
Setup time, data valid prior to WE↓	$t_{su(D)W}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.25 $t_{c(C)}$-45		ns
Hold time, data valid after WE↑	$t_{h(D)W}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.25 $t_{c(C)}$-10		ns
Disable time, data in high impedance after WE↑ 3/	$t_{dis(D)W}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		0.25 $t_{c(C)}$+25	ns
Pulse duration, $\overline{WE}$ low	$t_{w(WEL)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.50 $t_{c(C)}$-20		ns
Pulse duration, $\overline{REN}$ low	$t_{w(RENL)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.75 $t_{c(C)}$-20		ns
Write recovery time, time between WE↑ and REN↓	$t_{rec(WE)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.25 $t_{c(C)}$-5		ns
Read recovery time, time between REN↑ and WE↓	$t_{rec(REN)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.50 $t_{c(C)}$-10		ns
Delay time $\overline{WE}$↑ to CLKOUT↑	$t_{d(WE-CLK)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0.50 $t_{c(C)}$-20		ns
Setup time, data prior to REN↑	$t_{su(D)R}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	52		ns
Hold time, data after $\overline{REN}$↑	$t_{h(D)R}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	0		ns
Access time for read cycle data valid after valid address	$t_{a(A)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		$t_{c(C)}$-90	ns
Access time for read cycle from REN↓	$t_{oe(REN)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		0.75 $t_{c(C)}$-60	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Disable time, data-in high impedance after REN↑ 3/	$t_{dis(D)R}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		0.25 $t_{c(C)}$	ns
RESET ($\overline{RS}$) timing							
Delay from $\overline{RS}$↓ to $\overline{REN}$↑ and $\overline{WE}$↑ 3/	$t_{d(RS-RW)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		0.75 $t_{c(C)}$+20	ns
Delay from $\overline{RS}$↓ to $\overline{REN}$ and $\overline{WE}$ into high impedance 3/	$t_{dis(RS-RW)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		$2t_{c(C)}$	ns
Disable time, data bus after $\overline{RS}$↓ 3/	$t_{dis(RS-DB)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		1.25 $t_{c(C)}$	ns
Disable time, address bus after $\overline{RS}$↓ 3/	$t_{dis(RS-AB)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		$t_{c(C)}$	ns
Enable time, address bus after $\overline{RS}$↑ 3/	$t_{en(RS-AB)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		$t_{c(C)}$	ns
Setup time, $\overline{RS}$ before CLKOUT↓ 6/	$t_{su(RS)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	60		ns
Pulse duration, $\overline{RS}$	$t_{w(RS)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$5t_{c(C)}$		ns
Microcomputer/microprocessor mode ($\overline{NMI}$/MC/$\overline{MP}$)							
Hold time (to put device in microprocessor mode) after RS high	$t_{h(MC/MP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$t_{c(C)}$		ns
Interrupt ($\overline{INT}$)/nonmaskable interrupt ($\overline{NMI}$)							
Fall time, $\overline{INT}$ 3/	$t_{f(INT)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		15	ns
Fall time, $\overline{NMI}$ 3/	$t_{f(NMI)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse duration, $\overline{INT}$	$t_{w(INT)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$t_{c(C)}$		ns
Pulse duration, $\overline{NMI}$	$t_{w(NMI)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$t_{c(C)}$		ns
Setup time, $\overline{INT}$ before CLKOUT low 7/	$t_{su(INT)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	60		ns
Setup time, $\overline{NMI}$ before CLKOUT low 7/	$t_{su(NMI)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	60		ns
Bit I/O timing							
Rise and fall time outputs 3/	t_{rfo} (IOP)	V_{CC} = 4.5 V See figure 3	9,10,11	01		20	ns
CLKOUT low to data valid outputs	$t_{d(IOP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		0.75 $t_{c(C)}$+80	ns
Rise and fall time inputs 3/	$t_{t(IOP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		20	ns
Setup time, data before CLKOUT time	$t_{su(IOP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	40		ns
Input pulse duration	$t_{w(IOP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$t_{c(C)}$		ns
General purpose timers							
Rise time, TCLK1, TCLK2 3/	$t_{r(TIM)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		20	ns
Fall time, TCLK1, TCLK2 3/	$t_{f(TIM)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse duration, TCLK1, TCLK2 low	$t_{wl(TIM)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$t_{c(C)}+20$		ns
Pulse duration, TCLK1, TCLK2 high	$t_{wh(TIM)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$t_{c(C)}+20$		ns
Input pulse duration	$t_{clk(TIM)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$2t_{c(C)}+40$		ns
Watchdog timer timings							
Fall time, $\overline{WDT}$ 3/	$t_{f(WDT)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		20	ns
Delay time, CLKOUT to $\overline{WDT}$ valid	$t_{d(WDT)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$0.25\ t_{c(C)}+30$		ns
Pulse duration, WDT output	$t_{w(WDT)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$7t_{c(C)}$		ns
Event manager timer							
Fall time, CMP0-CMP5 3/	$t_{f(CMP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		20	ns
Rise time, CMP0-CMP5 3/	$t_{r(CMP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01		20	ns
Pulse duration, CMP0-CMP3 input	$t_{w(CAP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	$t_{c(C)}+20$		ns
Setup time, capture input before CLKOUT high	$t_{su(CAP)}$	V_{CC} = 4.5 V See figure 3	9,10,11	01	20		ns

1/ All testing to be performed using worst-case test conditions unless otherwise specified.

2/ This voltage specification is included for interface to HCMOS logic. However, note that all of the other timing parameters defined in this drawing are specified for TTL logic levels and will differ for HCMOS logic levels.

3/ Value is derived from characterization data and is guaranteed but not tested.

4/ I_{CC} characteristics are inversely proportional to temperature. Test is performed with outputs open.

5/ $t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).

6/ $\overline{RS}$ can occur anytime during the clock cycle. Time given is minimum to assure synchronous operation.

7/ $\overline{INT}$ and $\overline{NMI}$ are synchronous inputs and can occur at any time during the cycle. $\overline{NMI}$ and $\overline{INT}$ are edge triggered only.

Case X

Name	Pin	Name	Pin	Name	Pin
A11	A4	A10	B4	A9	A2
A8	C1	A7	C2	A6	D1
A5	G1	A4	G2	A3	J2
A2/PA2	K1	A1/PA1	L2	A0/PA0	K2
D15	L6	D14	K6	D13	L8
D12	K8	D11	L10	D10	J11
D9	H10	D8	G11	D7	D10
D6	C11	D5	C10	D4	B11
D3	A10	D2	B10	D1	A9
D0	B9	INT*	F1	NMI*/MC/MP*	H1
WE*	D2	REN*	E1	RS*	E2
CLKOUT	F2	V_{CC}	L5	V_{CC}	B5
V_{SS}	K5	V_{SS}	A5	CLKIN	J1
RXD	H11	TXD	J10	TCLK1	B1
TCLK2	B2	WDT*	H2	IOP15	L3
IOP14	K3	IOP13	L4	IOP12	K4
IOP11	L7	IOP10	K7	IOP9	L9
IOP8	K9	IOP7	K11	IOP6	K10
IOP5	G10	IOP4	F11	IOP3	F10
IOP2	E11	IOP1	E10	IOP0	D11
CMP0	B3	CMP1	A3	CMP2	B6
CMP3	A6	CAP0	B7	CAP1	A7
CMP4/CAP2	B8	CMP5/CAP3	A8		

* Indicates active low signals

FIGURE 1. Terminal connections.

Case Y

Name	Pin	Name	Pin	Name	Pin
A11	5	A10	6	A9	9
A8	12	A7	13	A6	14
A5	20	A4	21	A3	25
A2/PA2	26	A1/PA1	27	A0/PA0	28
D15	35	D14	36	D13	39
D12	40	D11	43	D10	46
D9	49	D8	50	D7	57
D6	58	D5	59	D4	60
D3	61	D2	62	D1	63
D0	64	INT*	18	NMI*/MC/MP*	22
WE*	15	REN*	16	RS*	17
CLKOUT	19	V_{CC}	04	V_{CC}	33
V_{SS}	03	V_{SS}	34	CLKIN	24
RXD	48	TXD	47	TCLK1	10
TCLK2	11	WDT*	23	IOP15	29
IOP14	30	IOP13	31	IOP12	32
IOP11	37	IOP10	38	IOP9	41
IOP8	42	IOP7	44	IOP6	45
IOP5	51	IOP4	52	IOP3	53
IOP2	54	IOP1	55	IOP0	56
CMP0	08	CMP1	07	CMP2	02
CMP3	01	CAP0	68	CAP1	67
CMP4/CAP2	66	CMP5/CAP3	65		

* Indicates active low signals

FIGURE 1. Terminal connections - Continued.

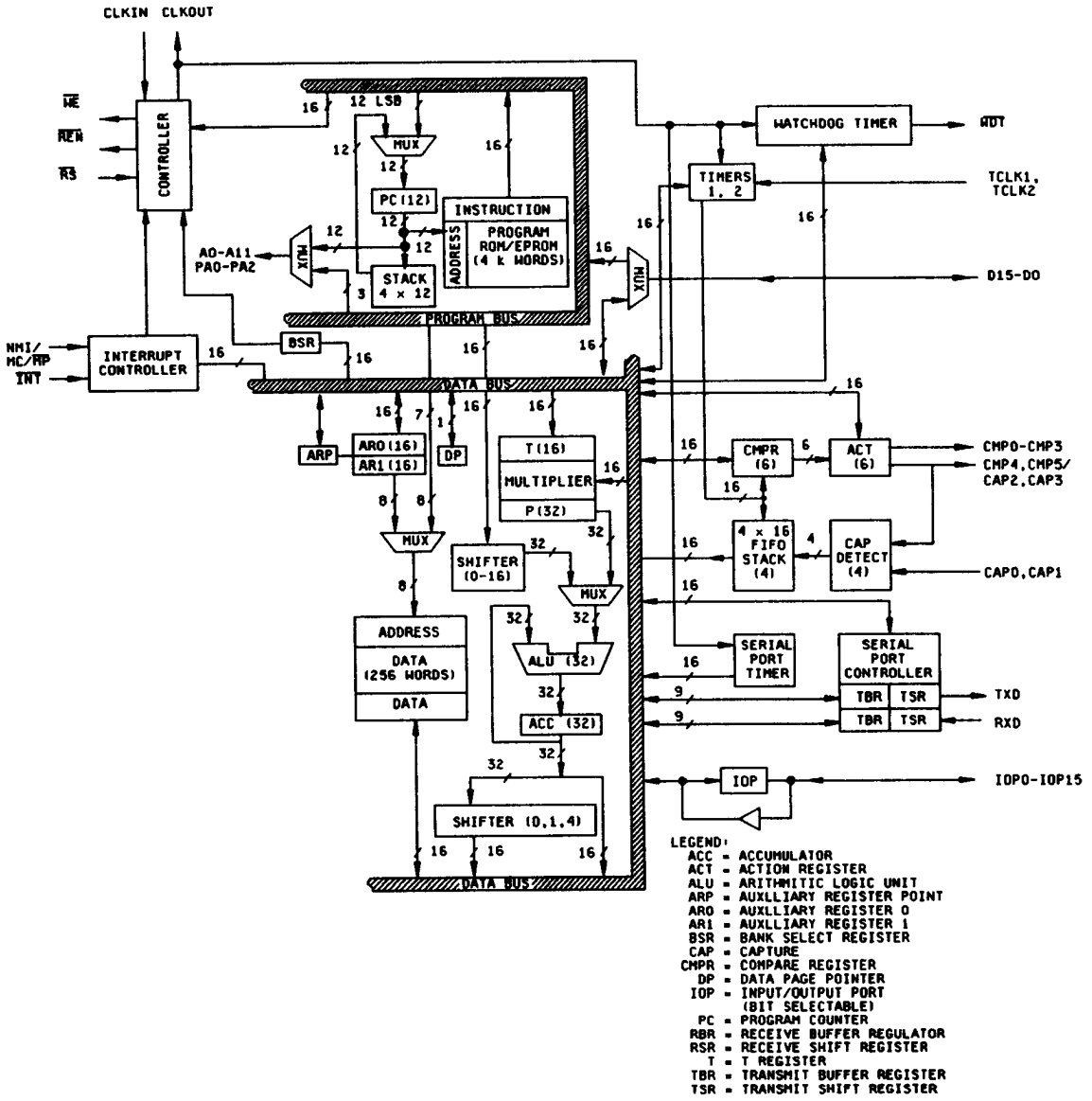
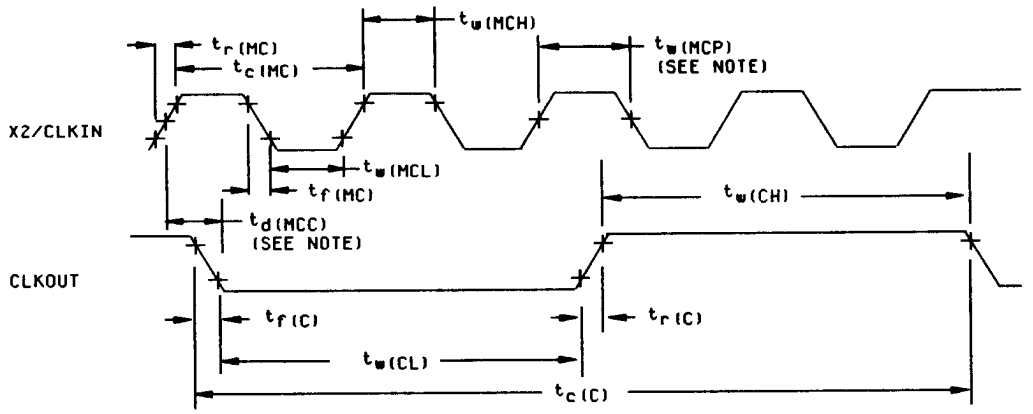


FIGURE 2. Block diagram.

Clock timing



NOTE: $t_{d(MCC)}$ AND $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 V on the CLKIN waveform.

Memory read timing

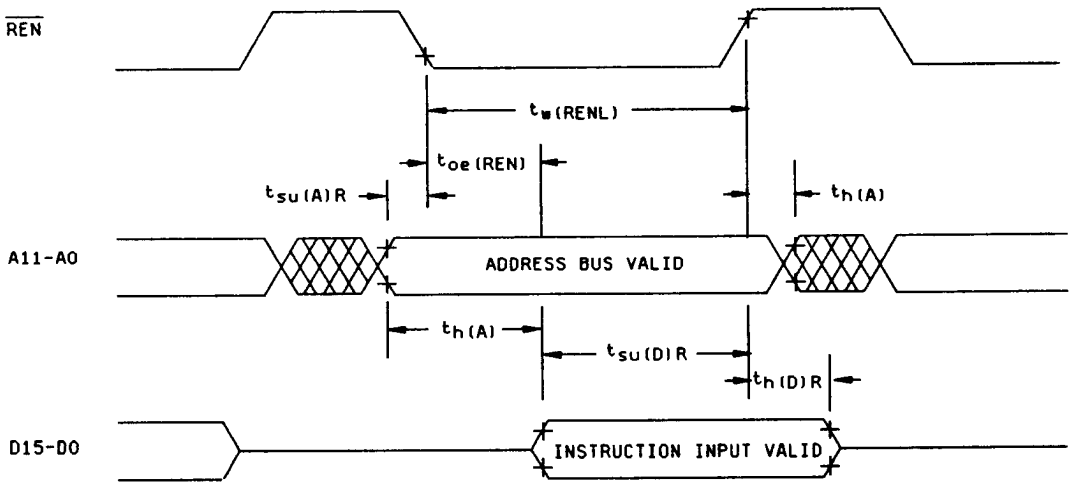
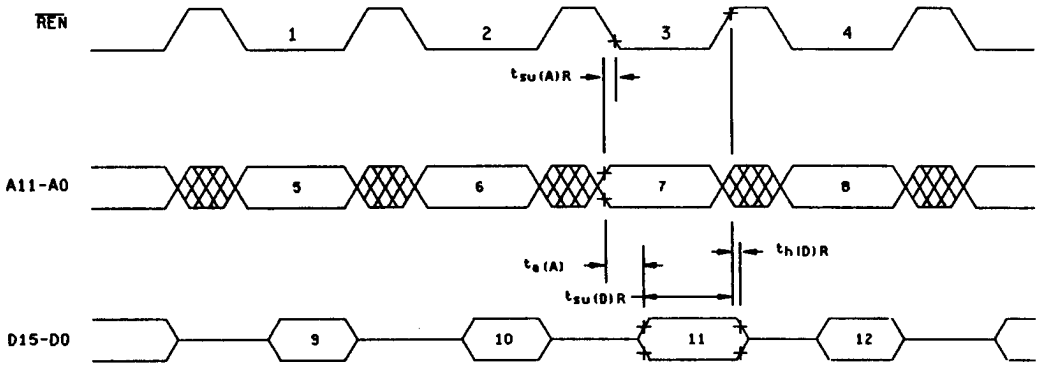


FIGURE 3. Waveforms.

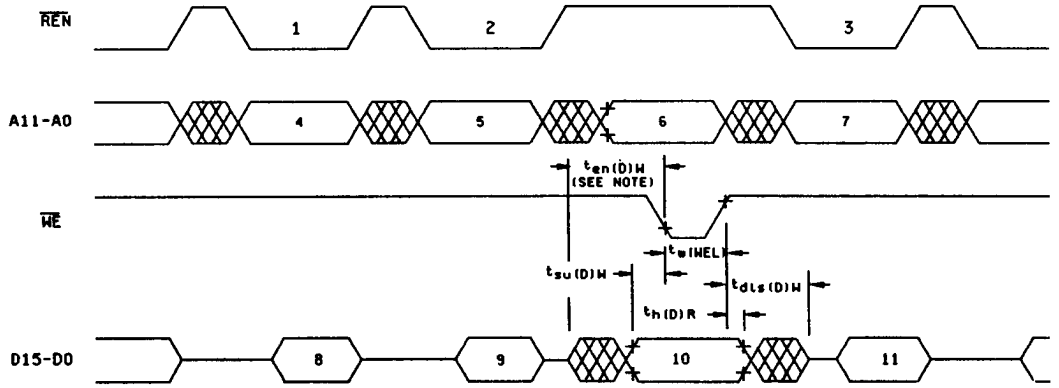
TBLR instruction timing



LEGEND:

1. TBLR instruction prefetch
2. Dummy prefetch
3. Data fetch
4. Next instruction prefetch
5. Address bus valid
6. Address bus valid
7. Address bus valid
8. Address bus valid
9. Instruction input valid
10. Instruction input valid
11. Data input valid
12. Instruction input valid

TBLR instruction timing



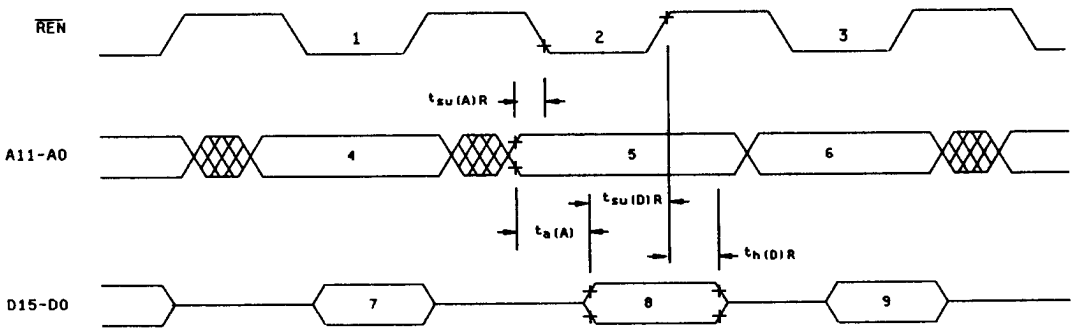
LEGEND:

1. TBLW instruction prefetch
2. Dummy prefetch
3. Next instruction prefetch
4. Address bus valid
5. Address bus valid
6. Address bus valid
7. Address bus valid
8. Instruction input valid
9. Instruction input valid
10. Data output valid
11. Instruction input valid

NOTE: Data valid prior to $\overline{WE}$↓.

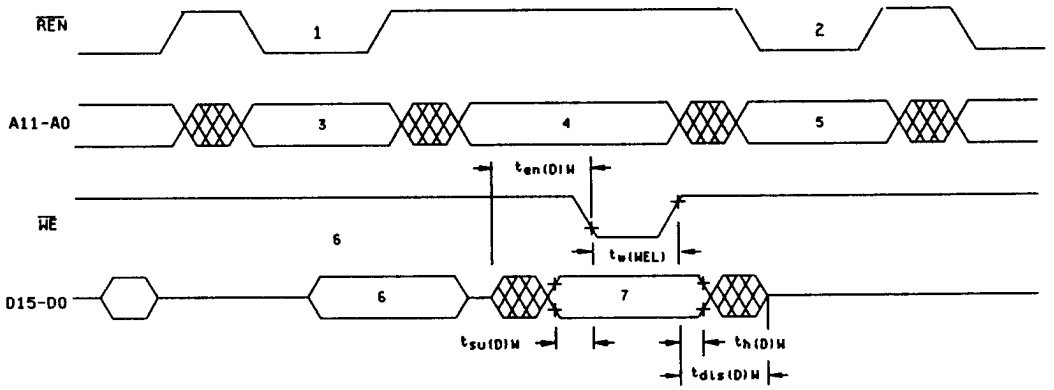
FIGURE 3. Waveforms - Continued.

IN instruction timing



LEGEND:
1. IN instruction prefetch
2. Data fetch
3. Next instruction prefetch
4. Address bus valid
5. Peripheral address valid
6. Address bus valid
7. Instruction input valid
8. Data input valid
9. Instruction input valid

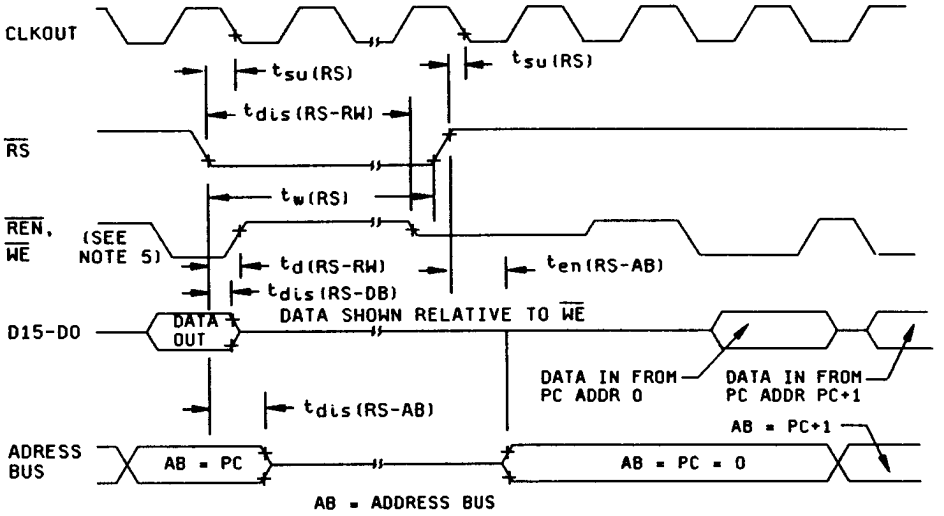
OUT instruction timing



LEGEND:
1. OUT instruction prefetch
2. Next instruction prefetch
3. Address bus valid
4. Peripheral address valid
5. Address bus valid
6. Instruction input valid
7. Data output valid

FIGURE 3. Waveforms - Continued.

Reset timing



NOTES:
1. RS forces REN and WE high and then places data bus D0-D15, REN, WE, and address bus A0-A11 in a high-impedance state. AB ouutputs and program counter are synchronously cleared to zero after the next complete clk cycle from RS↑.
2. RS must be maintained for a minimum of five clock cycles.
3. Resumption of normal program will commence after one complete CLK cycle from RS↑.
4. Due to the synchronization action on RS, time to execute the function can vary dependent upon when RS↑ or RS↓ occur in the CLK cycle.
5. Diagram shown is for definition purpose only. WE and REN are mutually exclusive.

Microcomputer/microprocessor mode timing

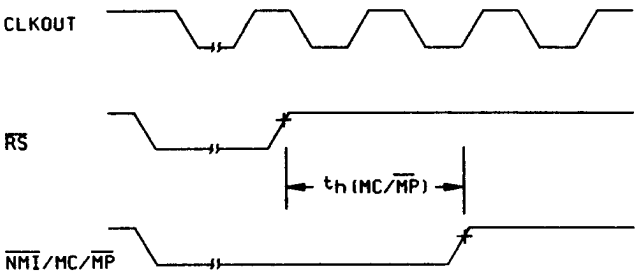


FIGURE 3. Waveforms - Continued.

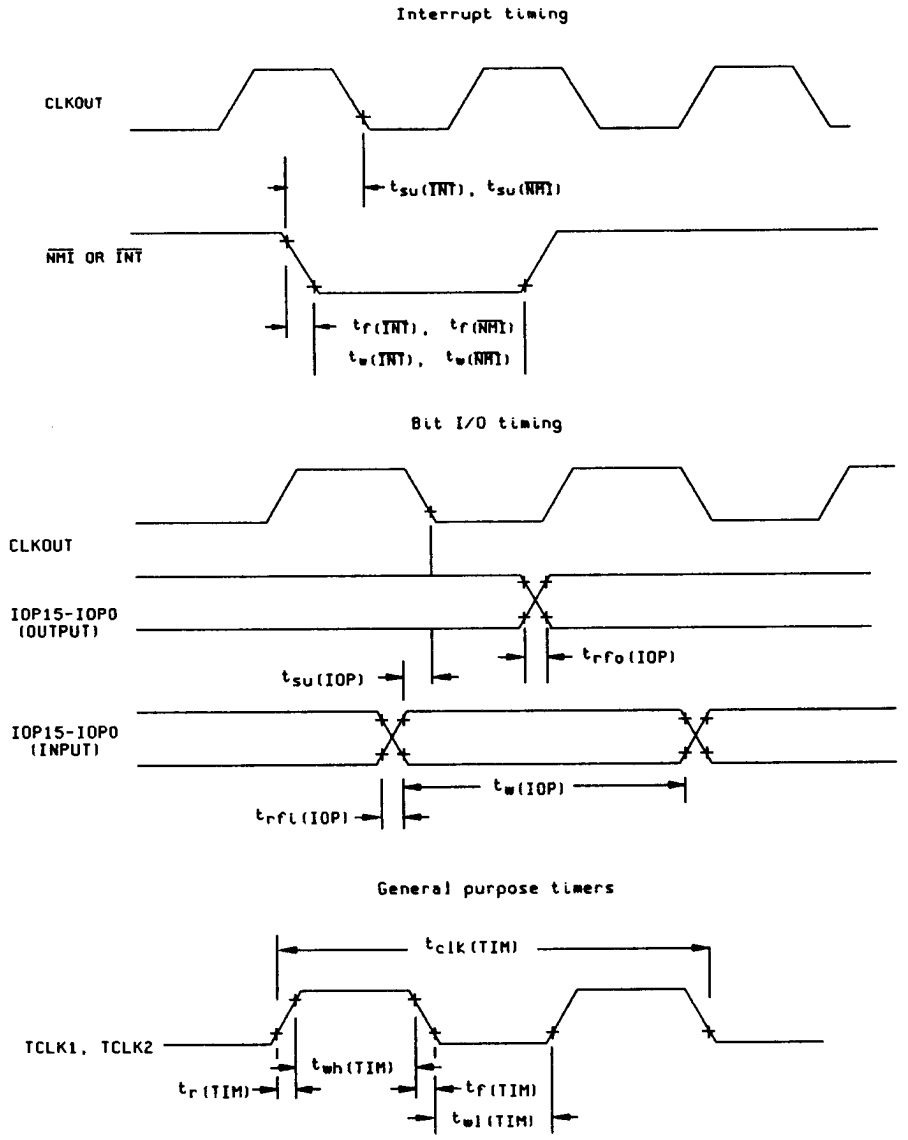
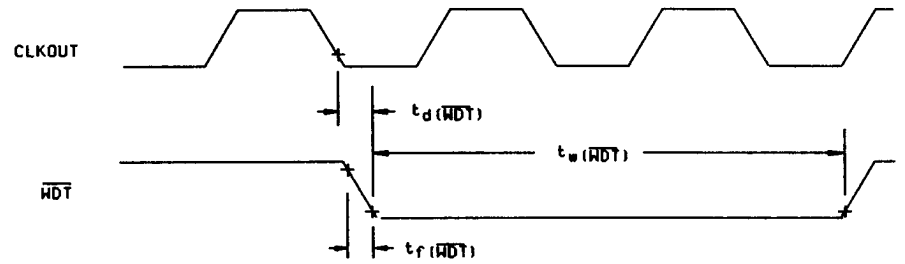
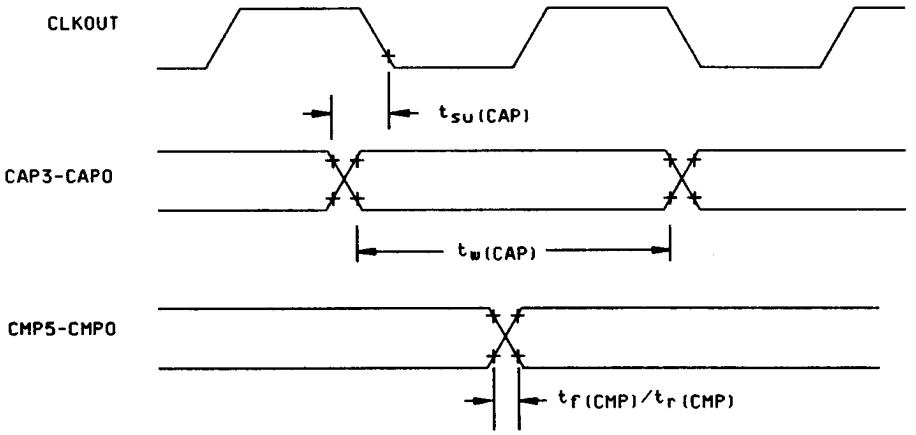


FIGURE 3. Waveforms - Continued.

Watchdog timer



Event manager



Test load circuit

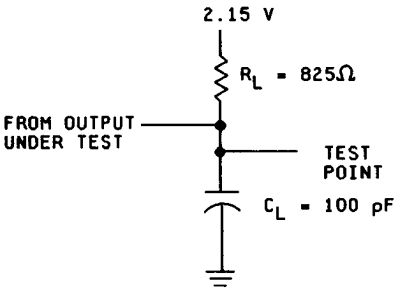


FIGURE 3. Waveforms - Continued.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except that interim electrical tests prior to burn in are optional at the discretion of the manufacturer for device class M.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

(1) Erase, (see 3.12.1).

(2) Program all 0's, (see 3.12.2).

(3) Test at +25°C. Measure V_{CC} max and store this value in the signature row.

(4) Unbiased bake for 72 hours at +165°C ±5°C.

(5) Margin test at +25°C. Measure V_{CC} max and compare with the value stored in the signature row. Any part with a delta greater than 0.66 V or with V_{CC} max less than 6.0 V consitiutes a failure. Also program and verify the r bit.

(6) Erase, (see 3.12.1).

(7) Program with random code. Verify this at max V_{CC}, (see 3.12.2).

(8) Burn-in (see 4.2.1a).

(9) Refresh EPROM data. Verify EPROM array at max V_{CC} and +25°C, (see 3.12.3).

(10) Test at +125°C and max V_{CC}. Refresh EPROM data. Verify EPROM array, (see 3.12.3).

(11) Test at -55°C and max V_{CC}. Refresh EPROM data. Verify EPROM array, (see 3.12.3).

(12) Erase, (see 3.12.1).

(13) Verify erasure at +25°C, (see 3.12.3).

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the instruction set. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT}, $C_{I/O}$ measurement) shall be measured only for the inital test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures. All input and output terminals shall be tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. Devices selected for testing shall be programmed with a random 50% pattern. After completion of all testing, the devices shall be erased and verified.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	- - -	- - -	- - -
Final electrical parameters (see 4.2)	1/ 1,2,3, 7,8 9,10,11	1/ 1,2,3, 7,8 9,10,11	2/ 1,2,3, 7,8 9,10,11	1/ 1,2,3, 7,8 9,10,11	2/ 1,2,3, 7,8 9,10,11
Group A test requirements (see 4.4)	1,2,3, 4,7,8 9,10,11	1,2,3, 4,7,8 9,10,11	1,2,3, 4,7,8 9,10,11	1,2,3, 4,7,8 9,10,11	1,2,3, 4,7,8 9,10,11
Group B end-point electrical parameters (see 4.4)	- - -	- - -	2,8A,10	- - -	- - -
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	- - -	- - -	2,8A,10	- - -	2,8A,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA environment and level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose (i.e., ultraviolet intensity times exposure time) for exposure should be a minimum of 15 ws/cm^2. The erasure time with this dosage is approximately 25 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 ws/cm^2 (one week at 12000 $\mu W/cm^2$). Exposure of EPROMS to high intensity ultraviolet light for long periods may cause permanent damage.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331 and table III.

TABLE III. Pin Descriptions.

PIN			I/O/Z	Description
Name	Package X	Package Y		Address/data buses
A11 A10 A9 A8 A7 A6 A5 A4 A3 A2/PA2 A1/PA1 A0/PA0	A4 B4 A2 C1 C2 D1 G1 G2 J2 K1 L2 KS	5 6 9 12 13 14 20 21 25 26 27 28	O/Z	Program memory address bus A11 (MSB) through A0 (LSB) and port addresses PA2 (MSB) through PA0 (LSB). Addresses A11 through A0 are always active and never go to high impedance except during reset. During execution of the IN and OUT instructions, pins 26, 27, and 28 carry the port addresses. Pins A3 though A11 are held high when port accesses are made on pins PA0 though PA2.
D15 MSB D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 LSB	L6 K6 L8 K8 L10 J11 H10 G11 D10 C11 C10 B11 A10 B10 A9 B9	35 36 39 40 43 46 49 50 57 58 59 60 61 62 63 64	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). The data bus is always in the high-impedance state except when $\overline{WE}$ is active (low). The data bus is also active when internal peripherals are written to.
Interrupt and miscellaneous signals				
$\overline{INT}$	F1	18	I	External interrupt input. The interrupt signal is generated by a high to low transition on this pin.
$\overline{NMI}/MC/\overline{MP}$	H1	22	I	Non-maskable interrupt. When this pin is brought low, the device is interrupted irrespective of the state of the INTM bit in status register ST. Microcomputer/microprocessor select. This pin is also sampled when $\overline{RS}$ is low. If high during reset, internal program memory is selected. If low during reset, external memory will be selected.
$\overline{WE}$	D2	15	O	Write enable. When active low, $\overline{WE}$ indicates that device will output data on the bus.
$\overline{REN}$	E1	16	O	Read enable. When active low, $\overline{REN}$ indicates that device will accept data from the bus.
$\overline{RS}$	E2	17	I	Reset. When this pin is low, the device is reset and PC is set to zero.

TABLE III. Pin Descriptions - Continued.

PIN			I/O/Z	Description
Name	Package X	Package Y		
				Supply/oscillator signals
CLKOUT	F2	19	O	System clock output (one fourth CLKIN frequency).
V_{CC}	L5, B5	4, 33	I	5-V supply pins.
V_{SS}	K5, A5	3, 34	I	Ground pins.
CLKIN	J1	24	I	Master clock input from external clock source.
				Address/data buses
RXD	H11	48	I	Asynchronous mode receive input.
TXD	J10	47	O/Z	Asynchronous mode transmit input.
TCLK1	B1	10	I	Timer 1 clock. If external clock is selected, it serves as clock input to Timer 1.
TCLK2	B2	11	I	Timer 2 clock. If external clock is selected, it serves as clock input to Timer 2.
$\overline{WDT}$	H2	23	O	Watchdog timer output. An active low is generated on this pin when the watchdog timer times out.
IOP15 MSB	L3	29	I/O	16 bit I/O lines that can be individually configured as inputs or outputs and also individually set or reset when configured as outputs.
IOP14	K3	30		
IOP13	L4	31		
IOP12	K4	32		
IOP11	L7	37		
IOP10	K7	38		
IOP9	L9	41		
IOP8	K9	42		
IOP7	K11	44		
IOP6	K10	45		
IOP5	G10	51		
IOP4	F11	52		
IOP3	F10	53		
IOP2	E11	54		
IOP1	E10	55		
IOP0 LSB	D11	56		
				Compare and capture signals
CMP0	B3	8	O	Compare outputs. The states of these pins are determined by the combination of compare and action registers.
CMP1	A3	7		
CMP2	B6	2		
CMP3	A6	1		
CAP0	B7	68	I	Capture inputs. A transition on these pins causes the timer register to be captured in FIFO stack.
CAP1	A7	67		
CMP4/CAP2	B8	66	I/O	This pin can be configured as compare output or capture input.
CMP5/CAP3	A8	65	I/O	This pin can be configured as compare output or capture input.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.