HB56U832 Series, HB56U432 Series

HB56U832B/SB
32 MB EDO DRAM SIMM
8-Mword × 32-bit, 2 k Refresh, 2-Bank Module
(16 pcs of 4 M × 4 Components)
HB56U432B/SB
16 MB EDO DRAM SIMM
4-Mword × 32 bit, 2 k Refresh, 1-Bank Module
(8 pcs of 4 M × 4 Components)

HITACHI

ADE-203-736B (Z)
Rev.2.0
Nov. 1997

Description

The HB56U832 is a 8M × 32 dynamic RAM module, mounted 16 pieces of 16-Mbit DRAM (HM5117405) sealed in SOJ package. The HB56U432 is a 4M × 32 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM5117405) sealed in SOJ package. The HB56U832, HB56U432 offer Extended Data Out (EDO) Page Mode as a high speed access time. An outline of the HB56U832, HB56U432 is 72-pin single in-line package. Therefore, the HB56U832, HB56U432 make high density mounting possible without surface mount technology. The HB56U832, HB56U432 provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 72-pin single in-line package
  - — Outline: 107.95 mm (Length) × 25.40 mm (Height) × 9.14/5.28 mm (Thickness)
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: t_{RAC} = 50/60/70 ns (max)
- Low power dissipation
  - — Active mode : 4.41/3.99/3.57W (max) (HB56U832 Series)
    : 4.20/3.78/3.36 W (max) (HB56U432 Series)

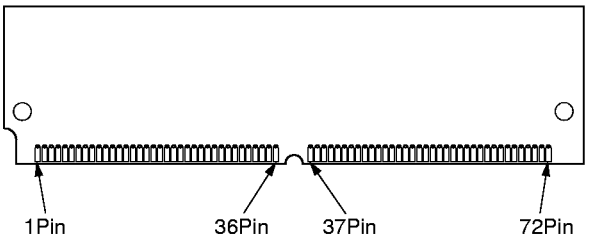
— Standby mode (TTL): 168 mW (max) (HB56U832 Series)
(TTL): 84 mW (max) (HB56U432 Series)
(CMOS): 12.6 mW (max) (L-version) (HB56U832 Series)
(CMOS): 6.3 mW (max) (L-version) (HB56U432 Series)

- EDO page mode capability
- Refresh period
  — 2048 refresh cycles: 32 ms
  :128 ms (L-version)
- 3 variations of refresh
  — $\overline{\text{RAS}}$-only refresh
  — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  — Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56U832B-5N	50 ns	72-pin SIP socket type	Gold
HB56U832B-6N	60 ns		
HB56U832B-7N	70 ns		
HB56U832B-5NL	50 ns		
HB56U832B-6NL	60 ns		
HB56U832B-7NL	70 ns		
HB56U432B-5N	50 ns		
HB56U432B-6N	60 ns		
HB56U432B-7N	70 ns		
HB56U432B-5NL	50 ns		
HB56U432B-6NL	60 ns		
HB56U432B-7NL	70 ns		
HB56U832SB-5N	50 ns	72-pin SIP socket type	Solder
HB56U832SB-6N	60 ns		
HB56U832SB-7N	70 ns		
HB56U832SB-5NL	50 ns		
HB56U832SB-6NL	60 ns		
HB56U832SB-7NL	70 ns		
HB56U432SB-5N	50 ns		
HB56U432SB-6N	60 ns		
HB56U432SB-7N	70 ns		
HB56U432SB-5NL	50 ns		
HB56U432SB-6NL	60 ns		
HB56U432SB-7NL	70 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V_{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{CAS1}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ30
9	DQ19	27	DQ23	45	$\overline{RAS1}$ (NC)*2	63	DQ14
10	V_{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{WE}$	65	DQ15
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	$\overline{RAS3}$ (NC)*1	51	DQ9	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V_{SS}

Notes: 1. $\overline{RAS3}$: HB56U832, NC: HB56U432
2. $\overline{RAS1}$: HB56U832, NC: HB56U432

Pin Description

Pin name	Function
A0 to A10	Address inputs: Row address: A0 to A10 Column address: A0 to A10 Refresh address: A0 to A10
DQ0 to DQ31	Data-in/Data-out
$\overline{CAS0}$ to $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$ to $\overline{RAS3}$	Row address strobe
$\overline{WE}$	Read/Write enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD4	Presence detect pin
NC	No connection

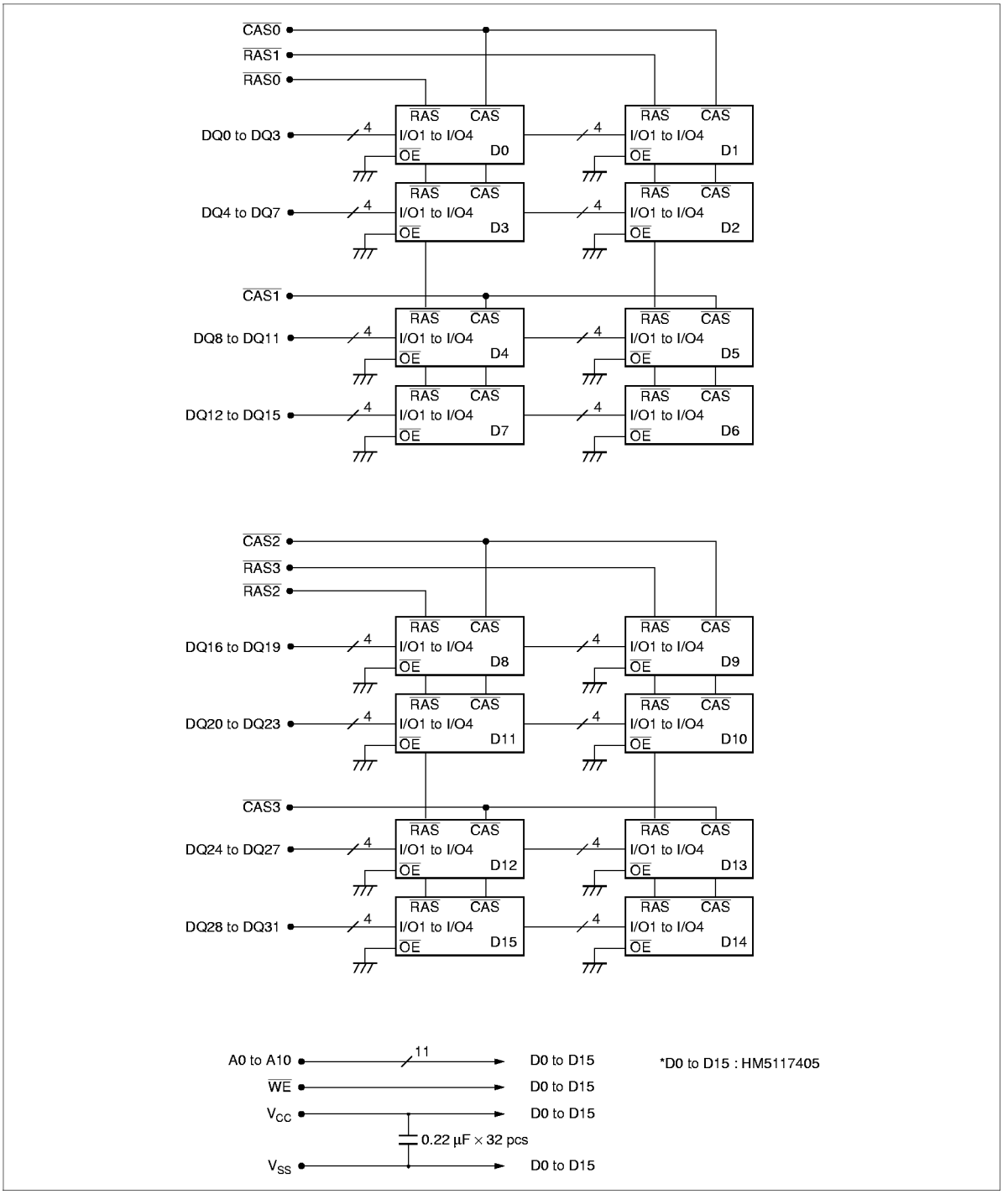
Presence Detect Pin Arrangement (HB56U832)

		Function		
Pin No.	Pin name	50 ns	60 ns	70 ns
67	PD1	NC	NC	NC
68	PD2	V_{SS}	V_{SS}	V_{SS}
69	PD3	V_{SS}	NC	V_{SS}
70	PD4	V_{SS}	NC	NC

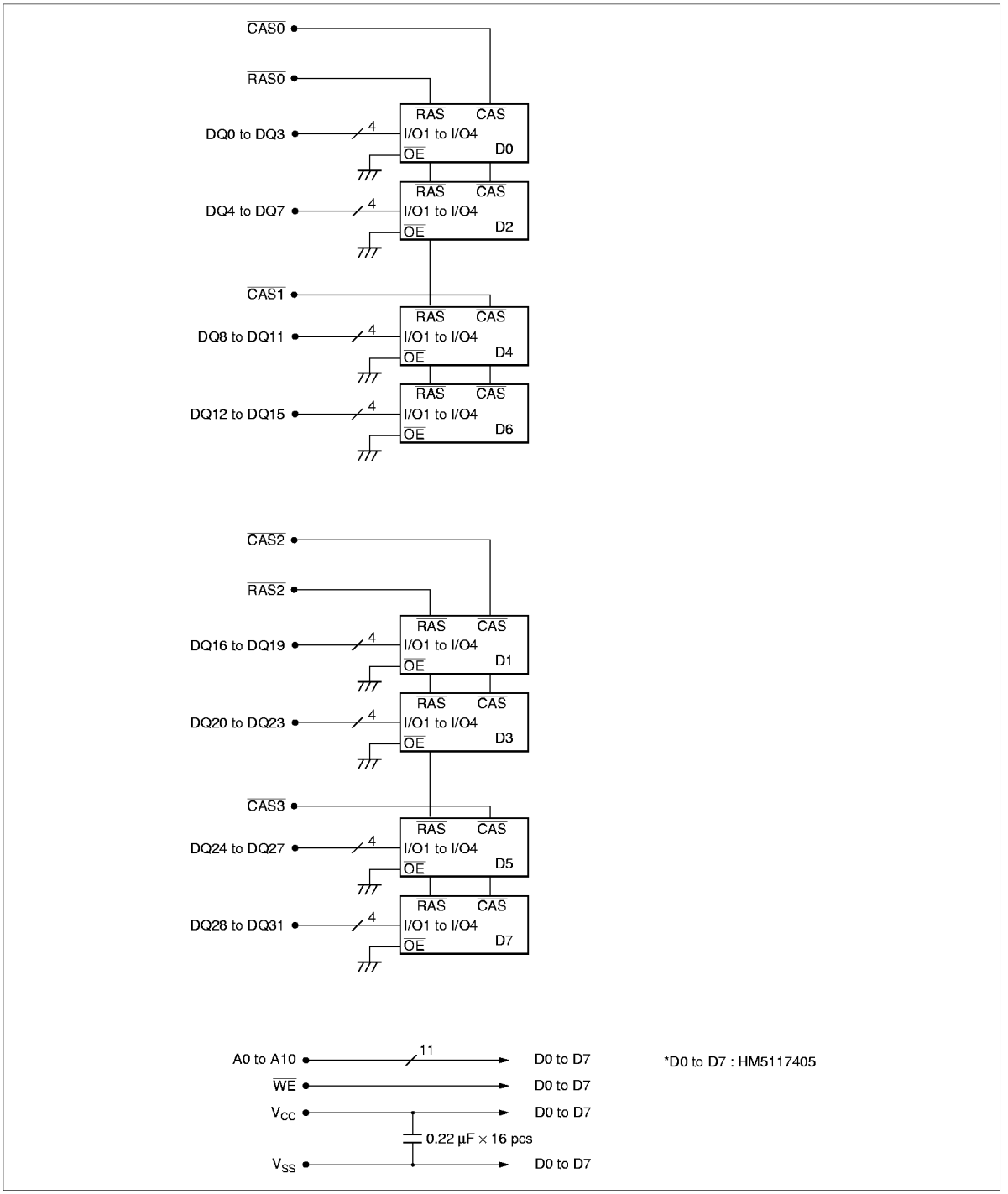
Presence Detect Pin Arrangement (HB56U432)

		Function		
Pin No.	Pin name	50 ns	60 ns	70 ns
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	NC	NC	NC
69	PD3	V_{SS}	NC	V_{SS}
70	PD4	V_{SS}	NC	NC

Block Diagram (HB56U832)



Block Diagram (HB56U432)



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	8	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56U832)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	840	—	760	—	680	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	32	—	32	—	32	mA	TTL interface, $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, Dout = High-Z	
		—	16	—	16	—	16	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	2.4	—	2.4	—	2.4	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	840	—	760	—	680	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	80	—	80	—	80	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	840	—	760	—	680	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	760	—	680	—	640	mA	t_{HPC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	5.6	—	5.6	—	5.6	mA	CMOS interface, Dout = High-Z, CBR refresh: t_{RC} = 62.5 µs, t_{RAS} ≤ 0.3 µs	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V, Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56U432)

		50 ns		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	800	—	720	—	640	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface, $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	1.2	—	1.2	—	1.2	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	800	—	720	—	640	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	800	—	720	—	640	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	720	—	640	—	600	mA	t_{HPC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	2.8	—	2.8	—	2.8	mA	CMOS interface, Dout = High-Z, CBR refresh: t_{RC} = 62.5 µs, t_{RAS} ≤ 0.3 µs	
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V, Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56U832)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	95	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	127	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	43	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	43	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	29	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56U432)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	60	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	71	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	43	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	29	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ±5%, V_{SS} = 0 V) *1, *2, *18

Test Conditions

- Input rise and fall times: 2 ns
- Input level: 0 V, 3.0V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, and Refresh Cycles (Common parameters)

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	7	10000	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	7	—	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	11	37	14	45	14	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	9	25	12	30	12	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	10	—	13	—	13	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	35	—	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	5
Refresh period (2,048 cycles)	t_{REF}	—	32	—	32	—	32	ms	
Refresh period (2,048 cycles) (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	7, 8, 15
Access time from address	t_{AA}	—	25	—	30	—	35	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time from $\overline{RAS}$	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	15	—	18	—	23	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	19
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	11, 19
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	3	—	ns	19
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	13	—	15	—	15	ns	19
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	13	—	15	—	15	ns	
$\overline{WE}$ to Din delay time	t_{WED}	13	—	15	—	18	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	
$\overline{RAS}$ to next $\overline{CAS}$ delay time	t_{RNCD}	50	—	60	—	70	—	ns	

Write Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	12
Write command hold time	t_{WCH}	7	—	10	—	13	—	ns	
Write command pulse width	t_{WP}	7	—	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	13
Data-in hold time	t_{DH}	7	—	10	—	13	—	ns	13

Refresh Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	7	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	7	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns	

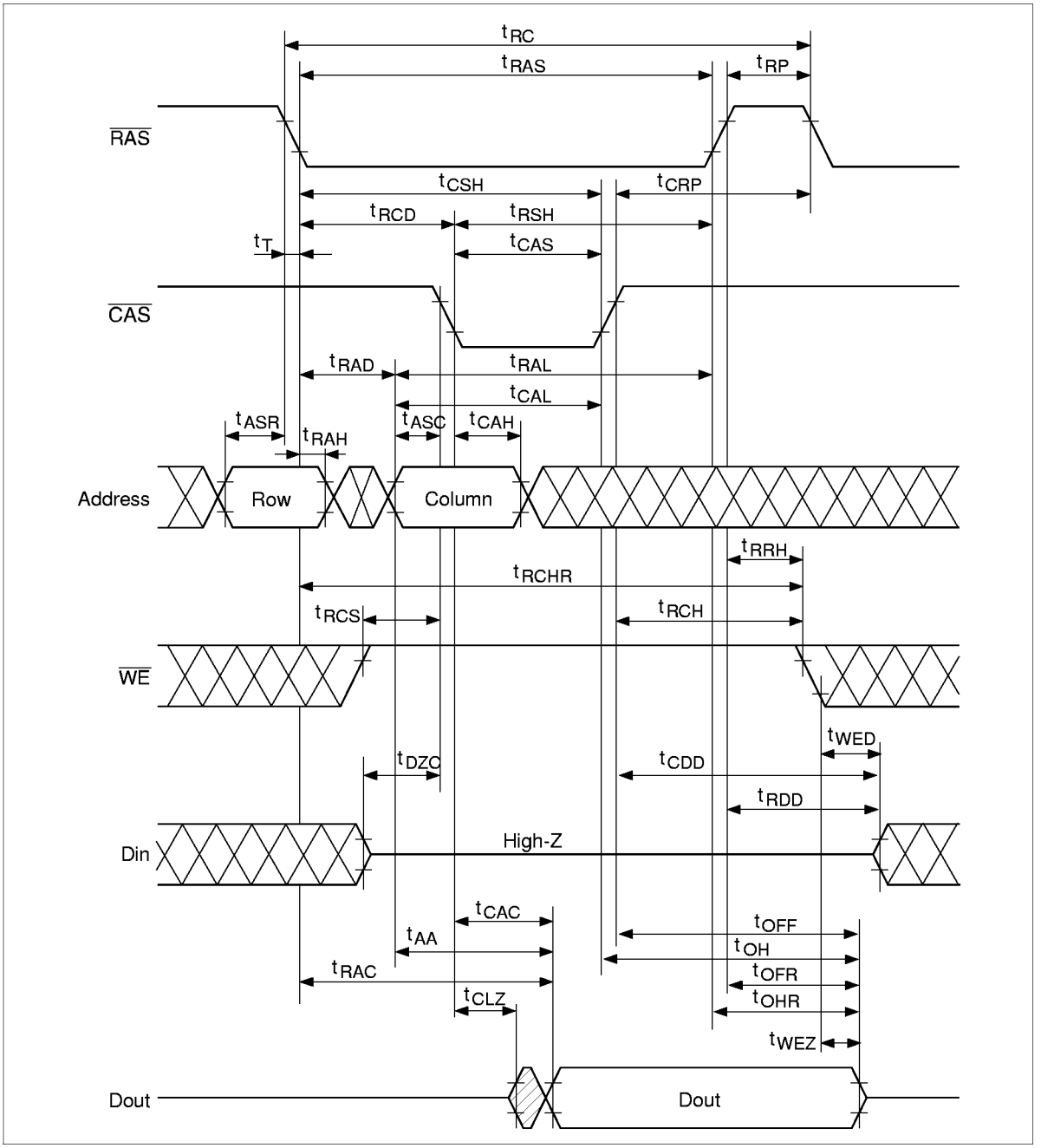
EDO Page Mode Cycle

		50 ns		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	20	—	25	—	30	—	ns	16
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	28	—	35	—	40	ns	7, 15
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	28	—	35	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	7, 15
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	28	—	35	—	40	—	ns	

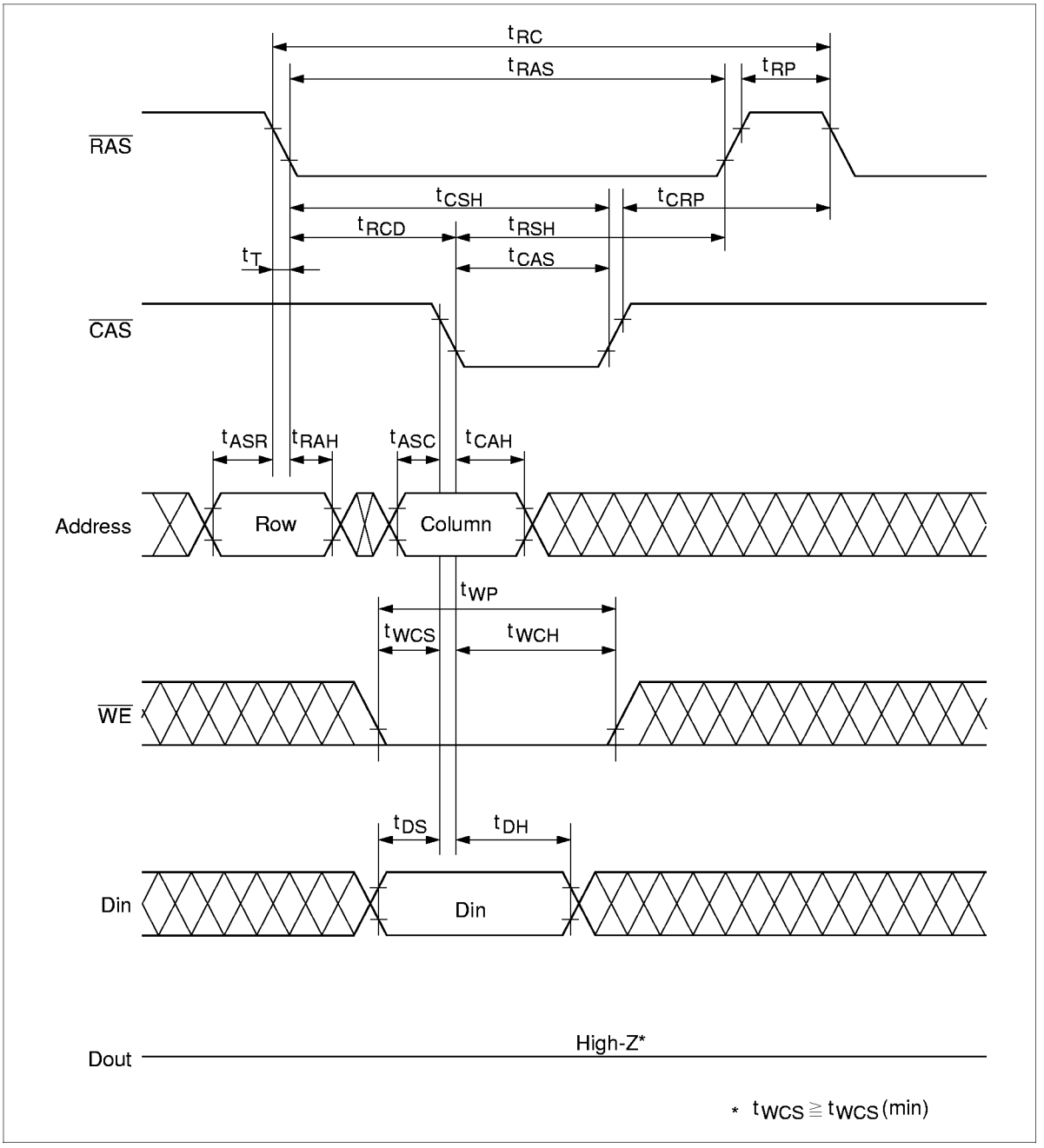
Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RCD}$ (max) + t_{AA} (max) - t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and t_{RCD} + t_{CAC} (max) $\geq t_{RAD}$ + t_{AA} (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and t_{RCD} + t_{CAC} (max) $\leq t_{RAD}$ + t_{AA} (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
12. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
13. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
15. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
16. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles.
17. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
19. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.
20. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))
    ///////: Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[20]

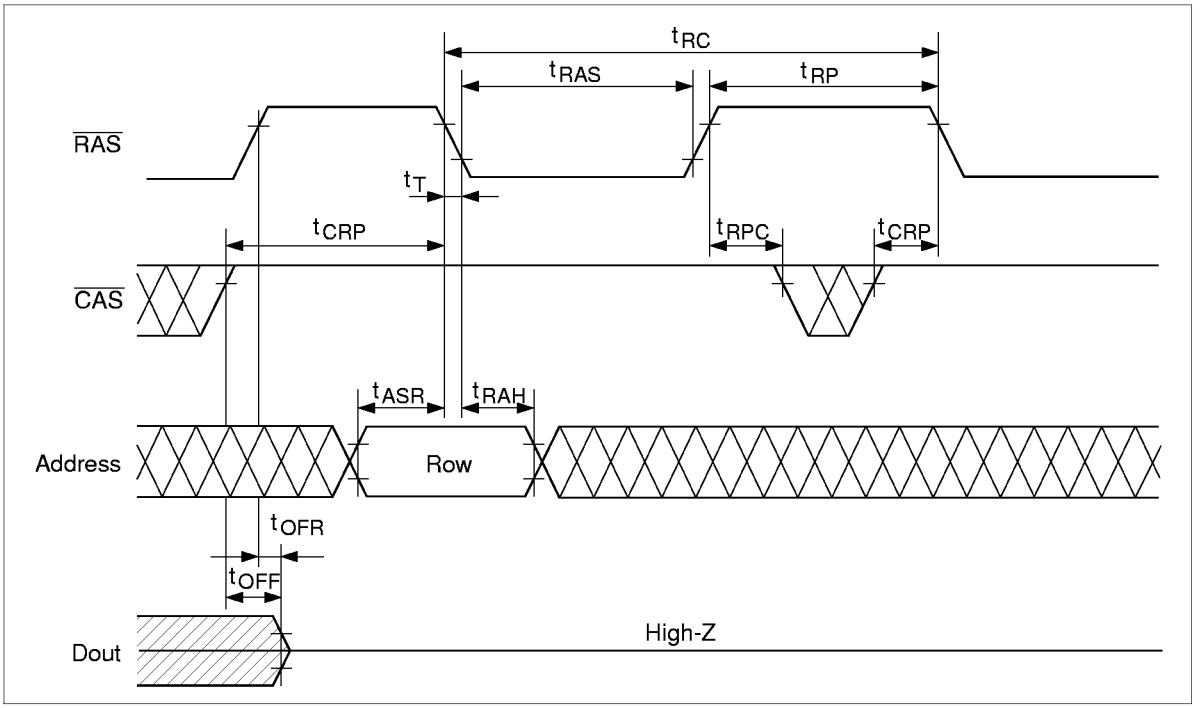
Read Cycle



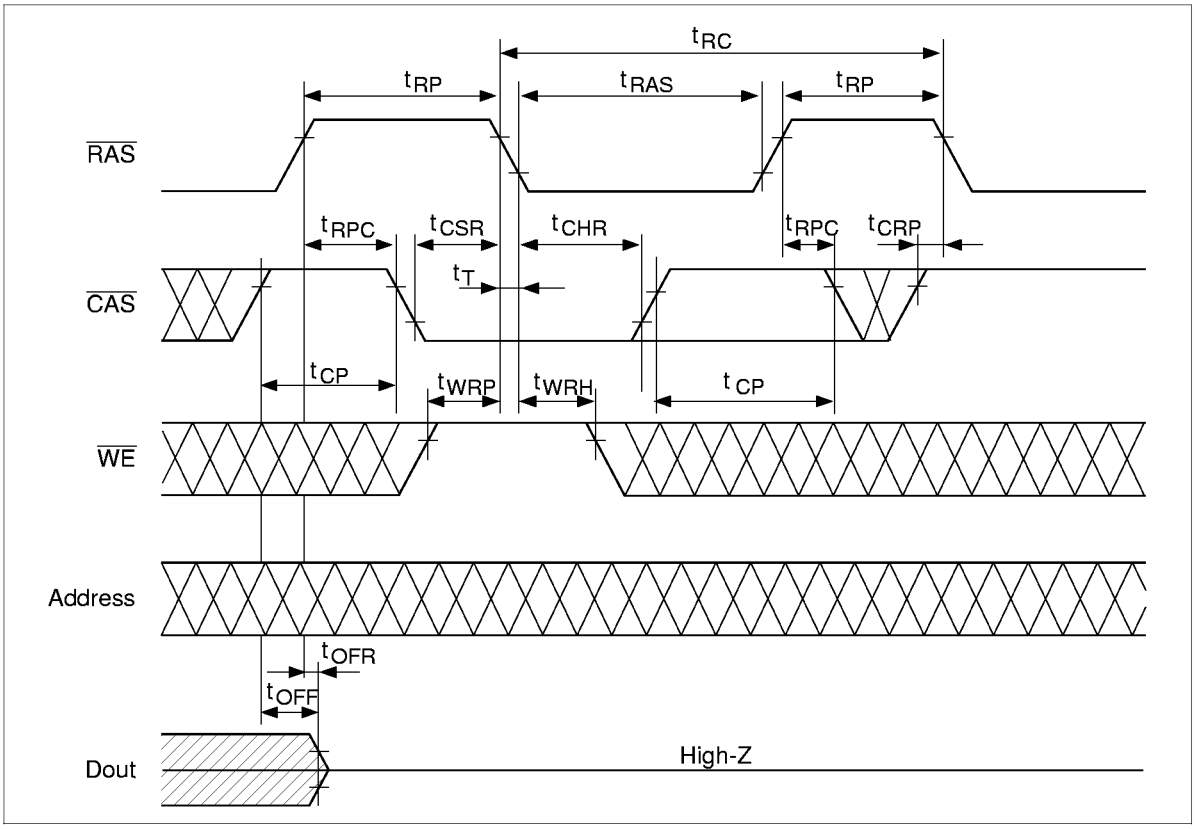
Early Write Cycle



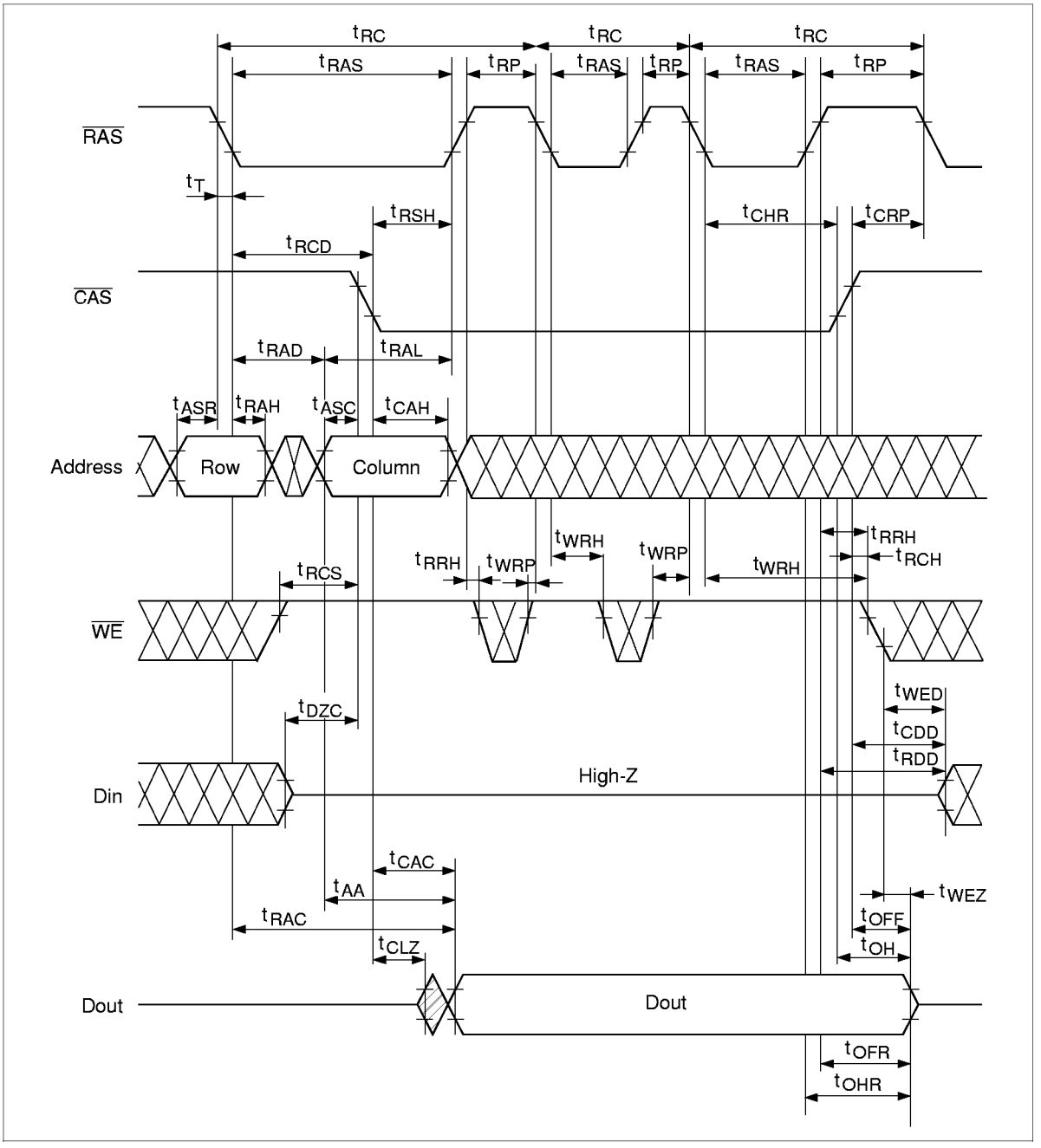
$\overline{\text{RAS}}$-Only Refresh Cycle



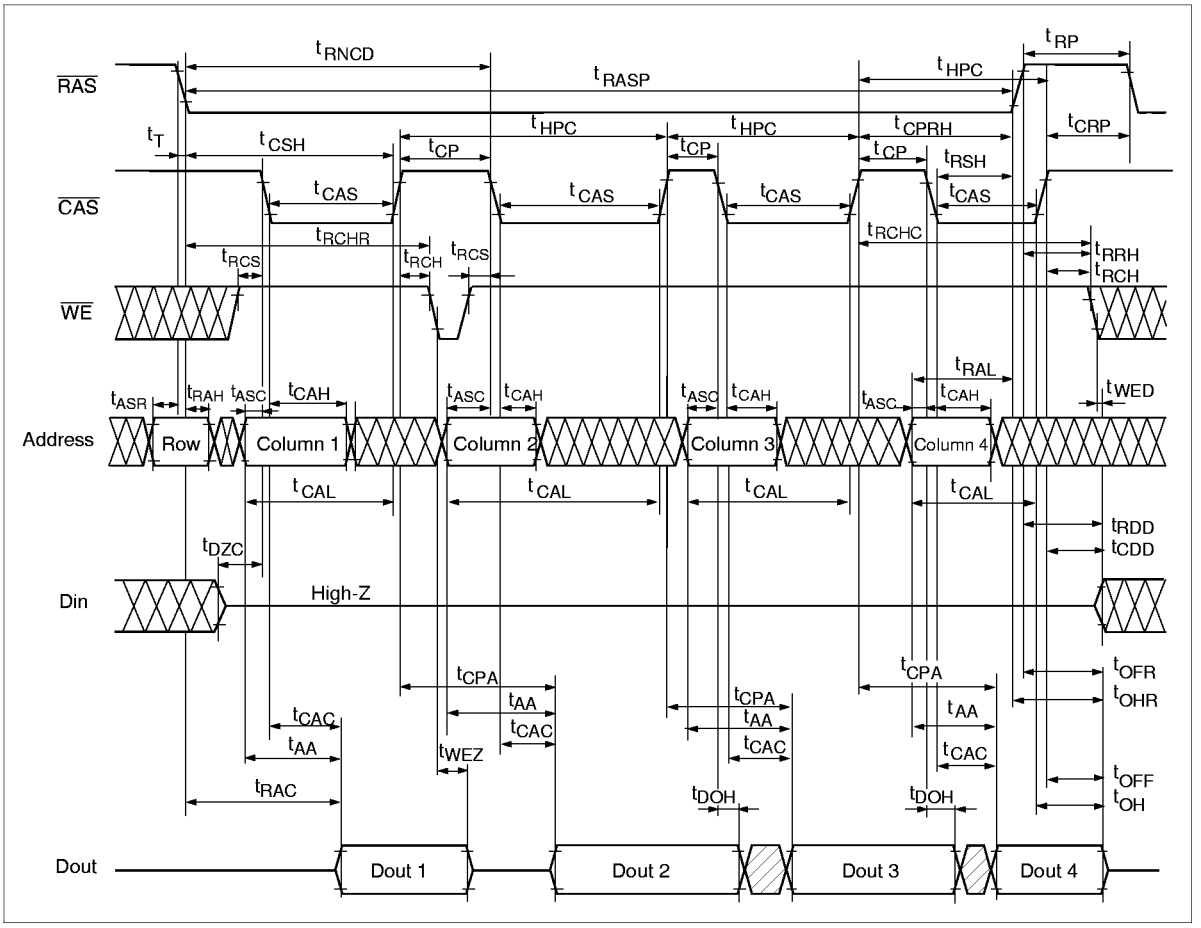
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



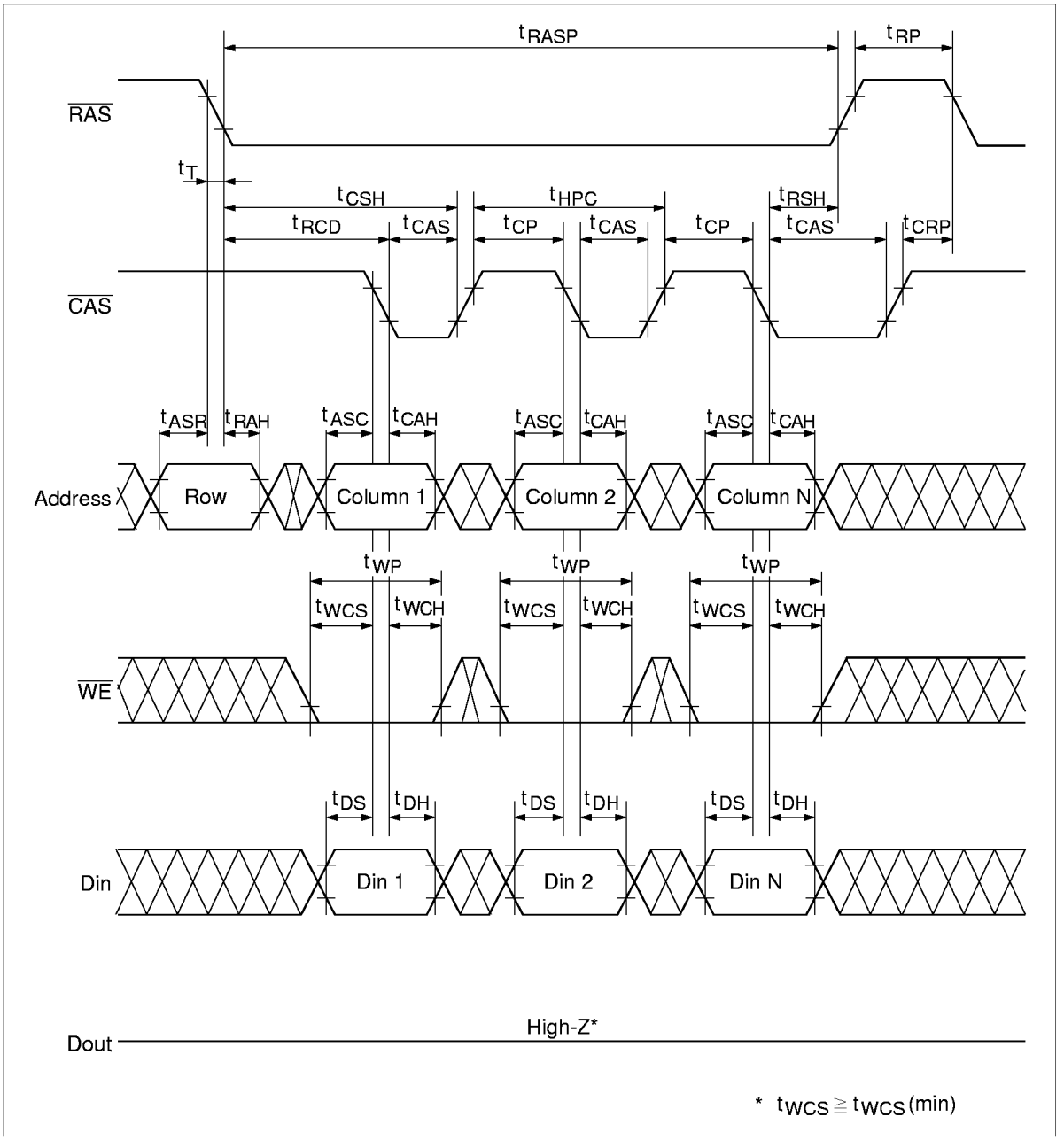
Hidden Refresh Cycle



EDO Page Mode Read Cycle

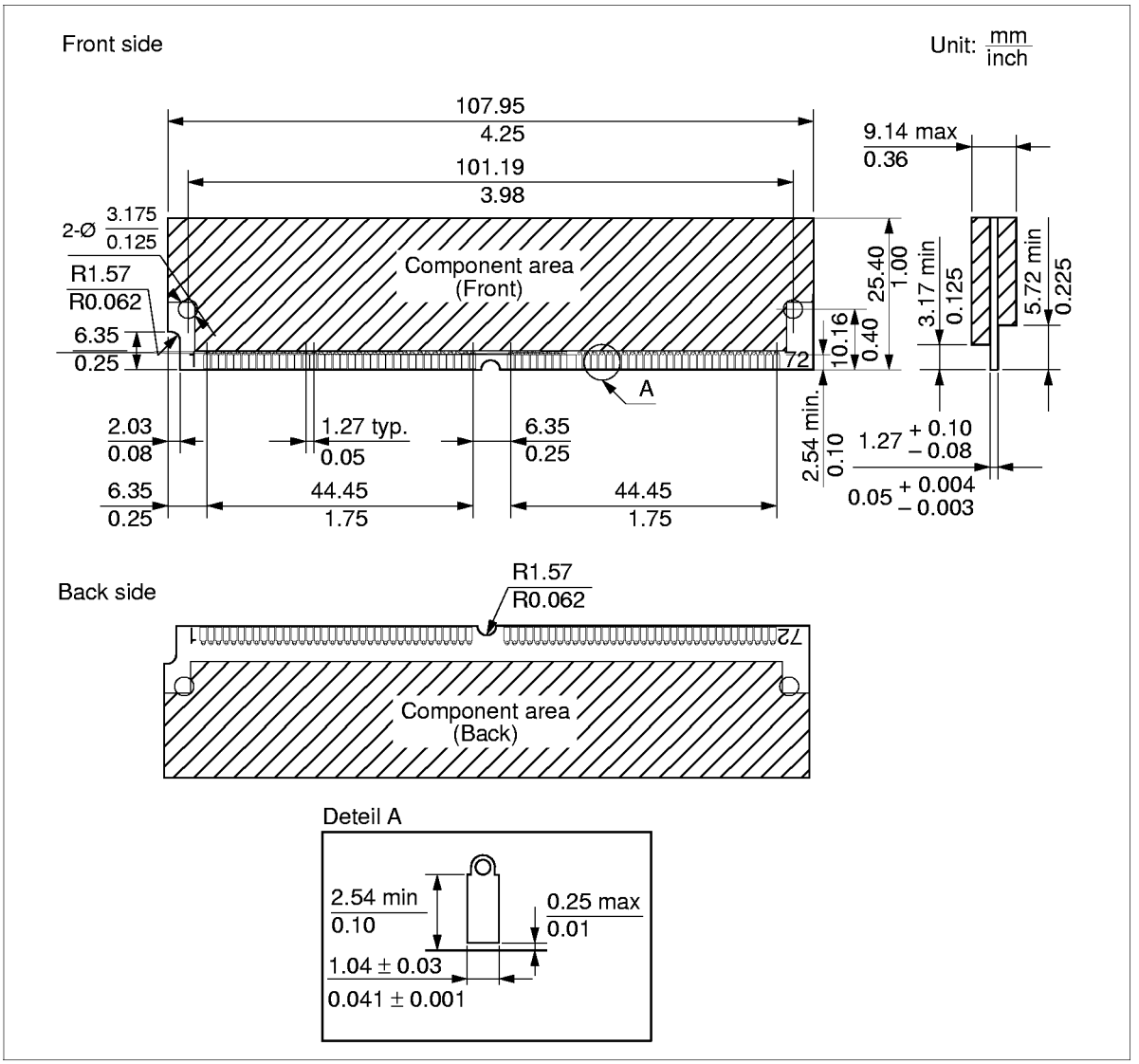


EDO Page Mode Early Write Cycle

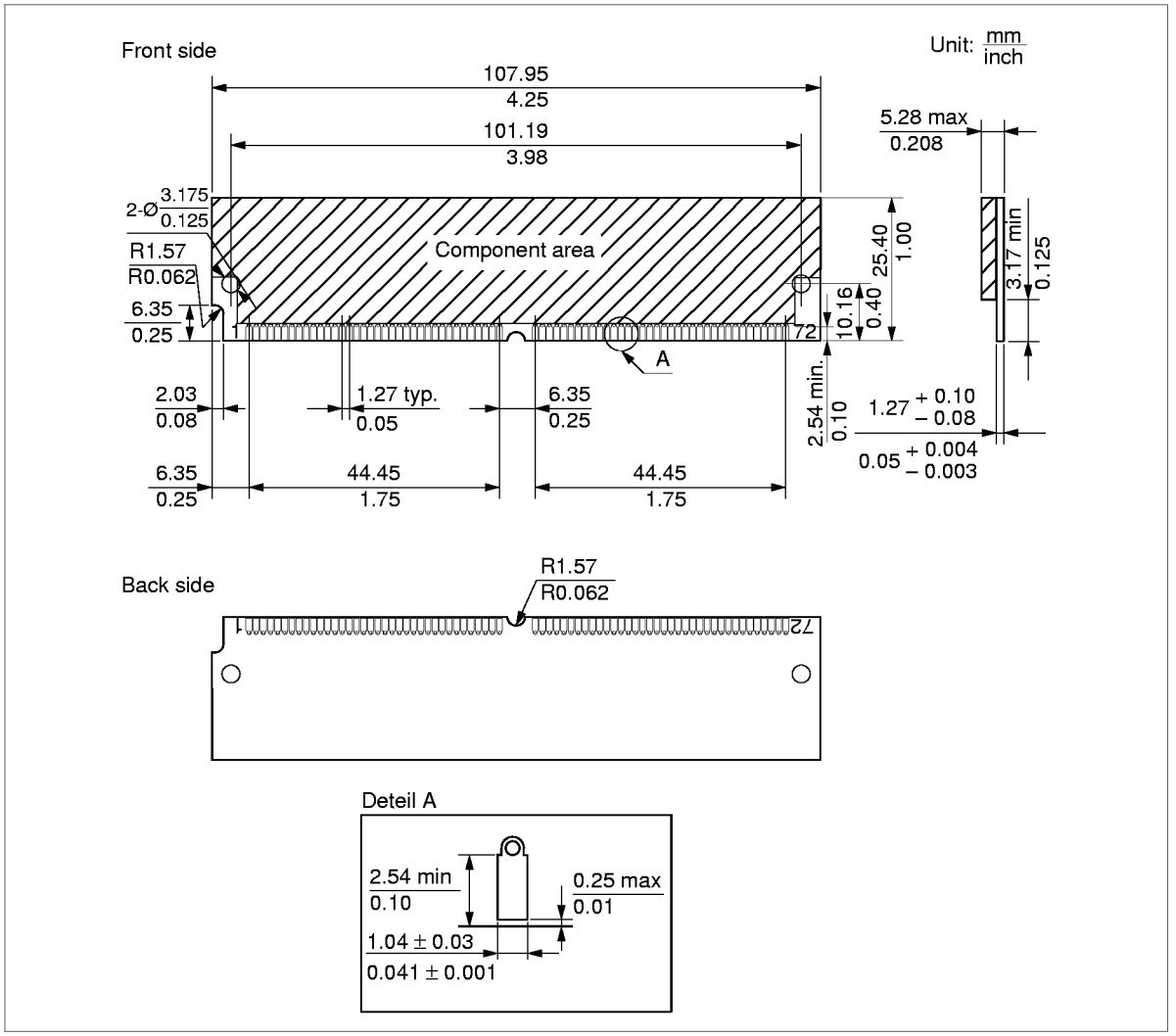


Physical Outline

HB56U832B/SB Series



HB56U432B/SB Series



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Feb. 7, 1997	Initial issue	S. Tsukui	K. Tsuneda
2.0	Nov. 1997	Change of Subtitle		