

2SJ550(L), 2SJ550(S)

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

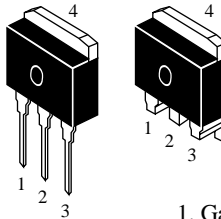
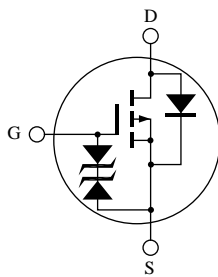
ADE-208-633A (Z)
2nd. Edition
Jul. 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.075\Omega$ typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

Outline

LDBPAK



1. Gate
2. Drain
3. Source
4. Drain

2SJ550(L),2SJ550(S)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-15	A
Drain peak current	$I_{D(pulse)}^{Note1}$	-60	A
Body-drain diode reverse drain current	I_{DR}	-15	A
Avalanche current	I_{AP}^{Note3}	-15	A
Avalanche energy	E_{AR}^{Note3}	19	mJ
Channel dissipation	P_{ch}^{Note2}	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

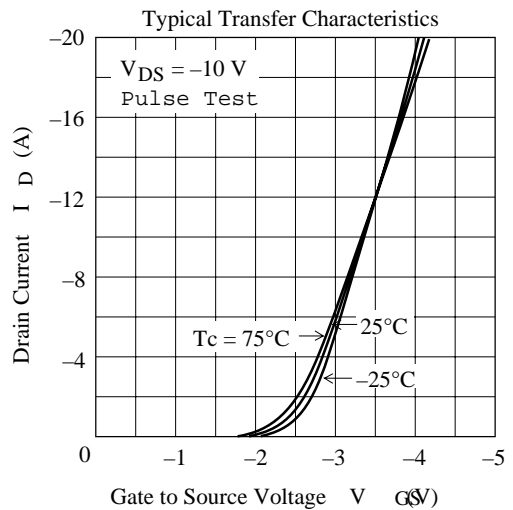
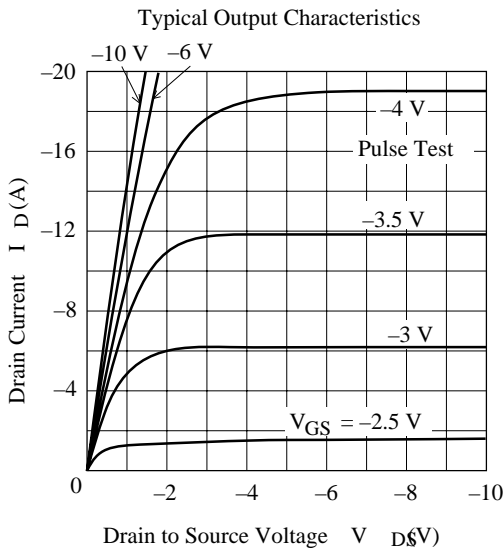
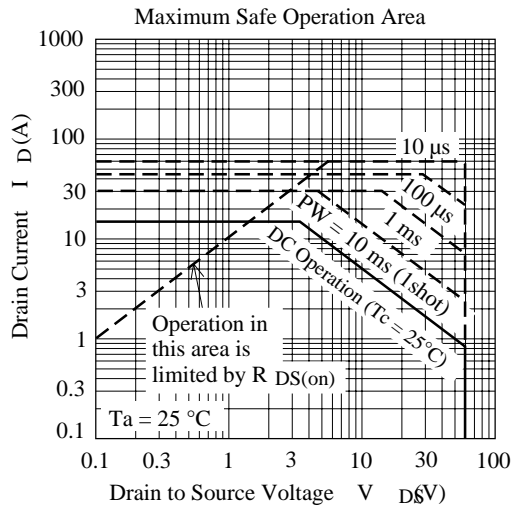
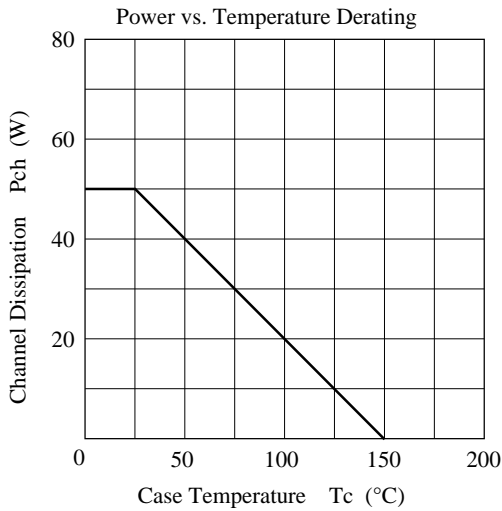
- Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ C$
3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50\ \Omega$

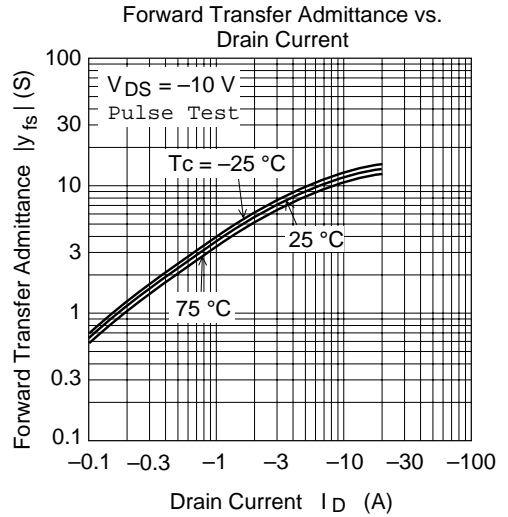
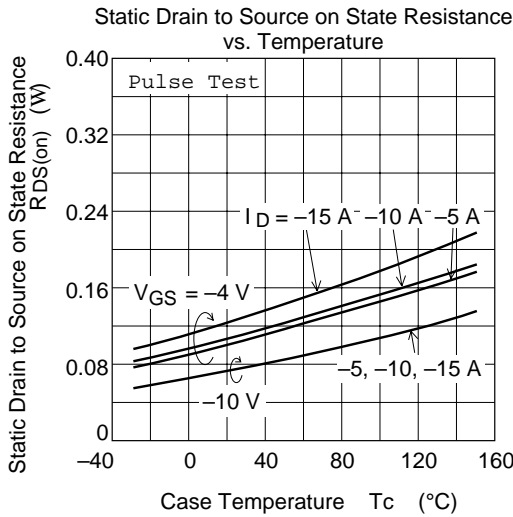
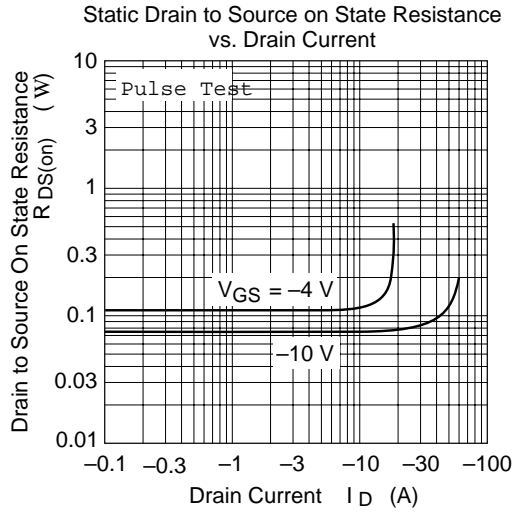
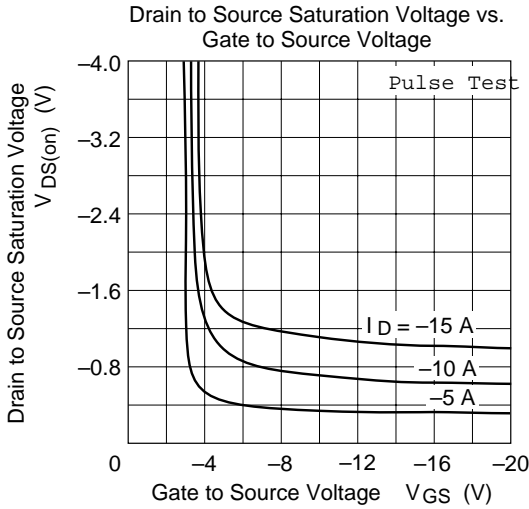
Electrical Characteristics (Ta = 25°C)

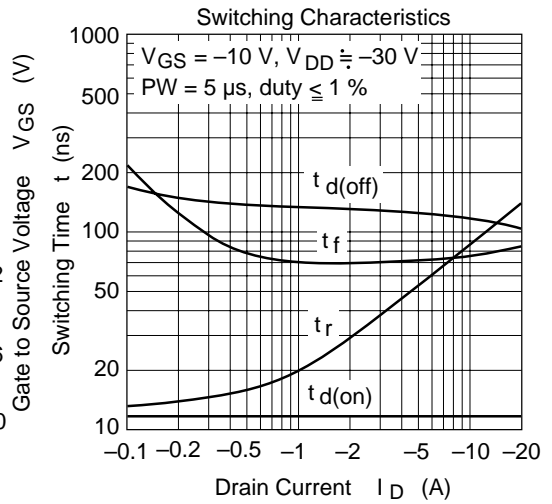
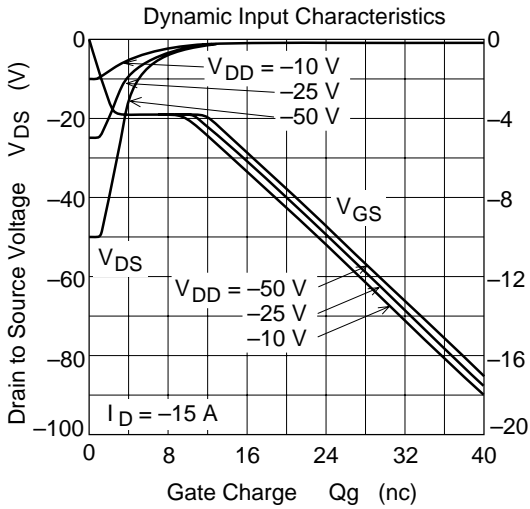
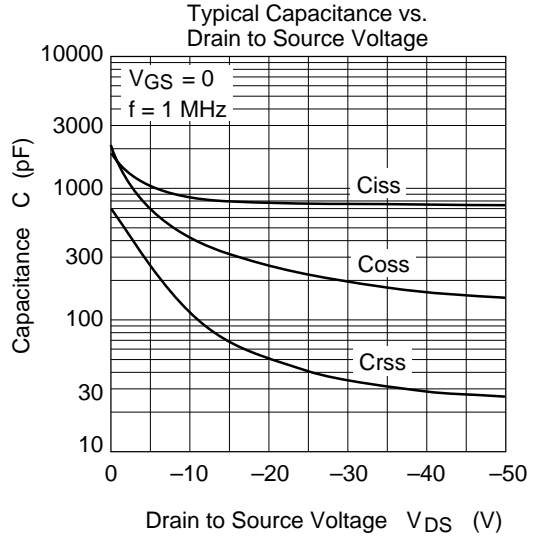
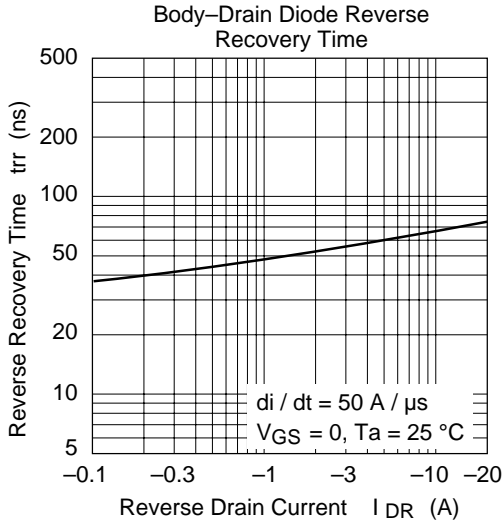
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$, $V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.075	0.095	Ω	$I_D = -8\text{A}$, $V_{GS} = -10\text{V}$ ^{Note4}
	$R_{DS(on)}$	—	0.105	0.155	Ω	$I_D = -8\text{A}$, $V_{GS} = -4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	6.5	11	—	S	$I_D = -8\text{A}$, $V_{DS} = -10\text{V}$ ^{Note4}
Input capacitance	C_{iss}	—	850	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	C_{oss}	—	420	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	110	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	$V_{GS} = -10\text{V}$, $I_D = -8\text{A}$
Rise time	t_r	—	75	—	ns	$R_L = 3.75\Omega$
Turn-off delay time	$t_{d(off)}$	—	125	—	ns	
Fall time	t_f	—	75	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-1.1	—	V	$I_F = -15\text{A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	70	—	ns	$I_F = -15\text{A}$, $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

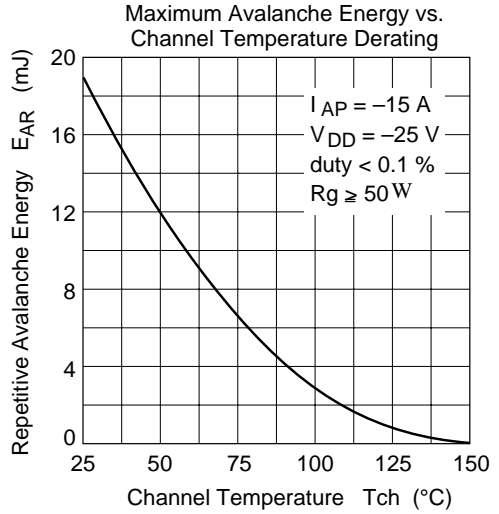
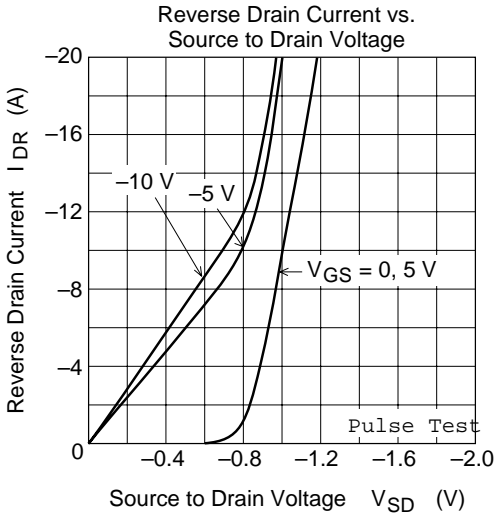
Note: 4. Pulse test

Main Characteristics

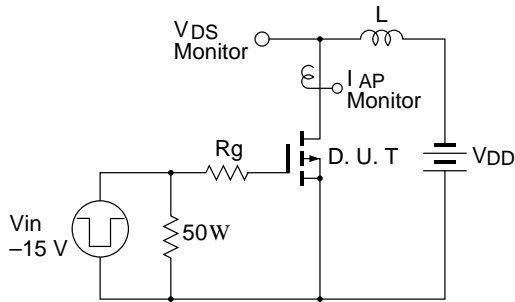






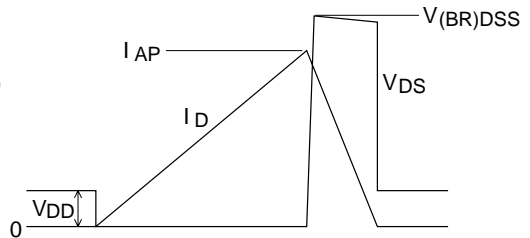


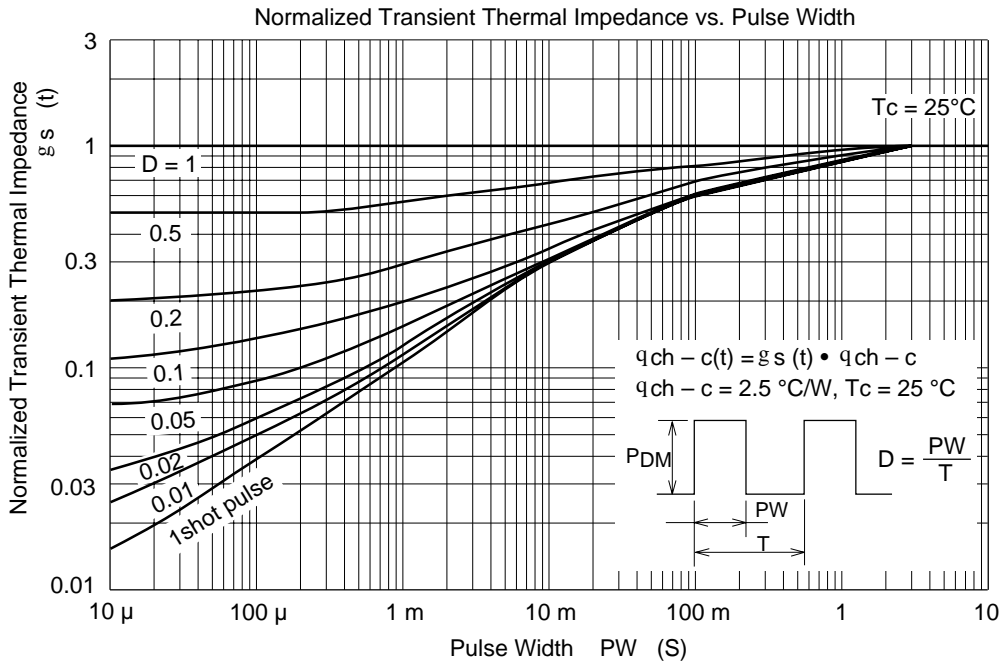
Avalanche Test Circuit



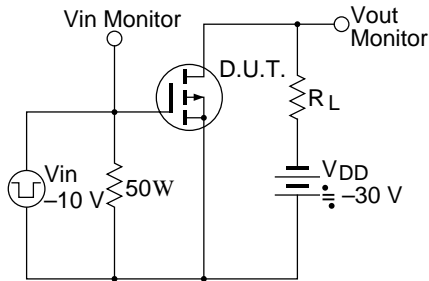
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

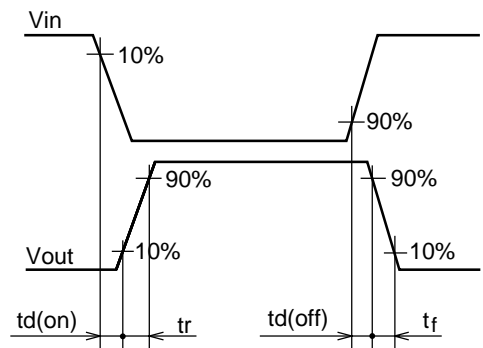




Switching Time Test Circuit

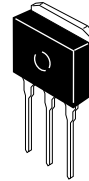
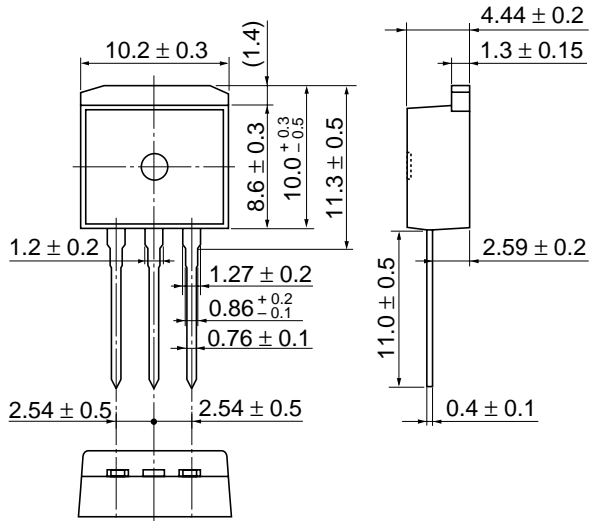


Waveform



Package Dimensions

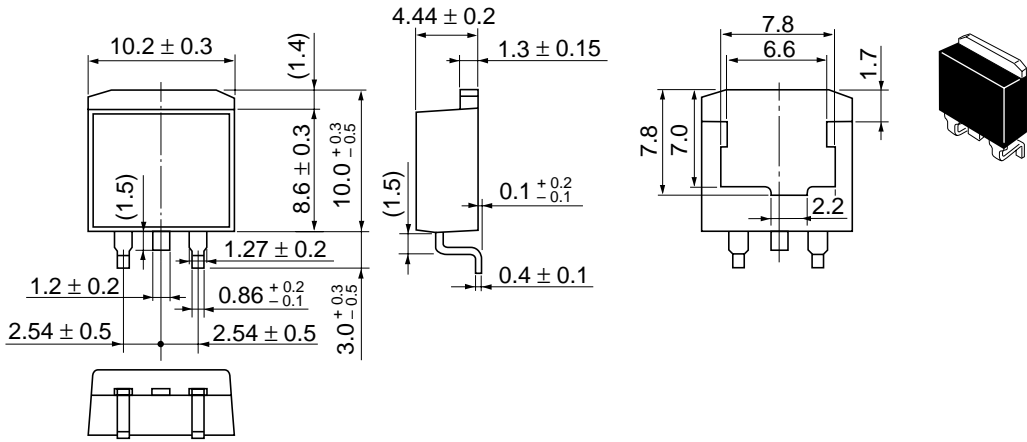
As of January, 2001
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

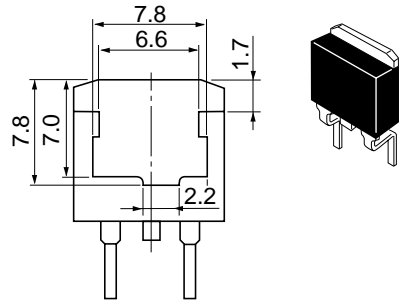
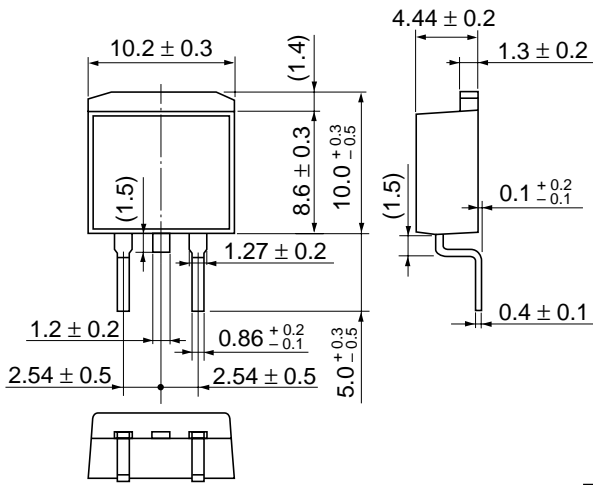
2SJ550(L),2SJ550(S)

As of January, 2001
Unit: mm



Hitachi Code	LDBAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

As of January, 2001
Unit: mm



Hitachi Code	LDBAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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