FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20890-1E

PAGE MODE FLASH MEMORY

CMOS

32 M (2 M × 16/1 M × 32) BIT

MBM29PL3200TE/BE 70/90

■ DESCRIPTION

The MBM29PL3200TE/BE is 32 M-bit, 3.0 V-only Page mode Flash memory organized as 2 M words of 16 bits each or 1 M words of 32 bits each. The device is offered in 90-pin SSOP and 84-ball FBGA packages. This device is designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

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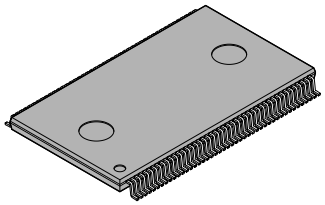
■ PRODUCT LINE-UP

Part No.		MBM29PL3200TE/BE	
Ordering Part No.	V_{CC} = 3.3 V $^{+0.3\ V}_{-0.3\ V}$	70	—
	V_{CC} = 3.0 V $^{+0.6\ V}_{-0.3\ V}$	—	90
Max. Random Address Access Time (ns)		70	90
Max. Page Address Access Time (ns)		25	35
Max. $\overline{CE}$ Access Time (ns)		70	90
Max. $\overline{OE}$ Access Time (ns)		25	35

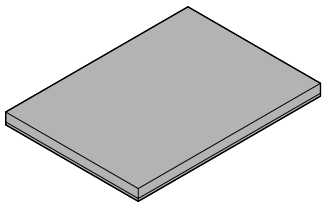
■ PACKAGES

90-pin plastic SSOP



(FPT-90P-M01)

84-ball plastic FBGA



(BGA-84P-M01)

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The device provides truly high performance non-volatile Flash memory solution. The device offers fast page access times of 25 ns and 35 ns with random access times of 70 ns and 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls. The page size is 8 words or 4 double words.

The device is command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The device is programmed by executing the program command sequence. This will invoke the Embedded Program™ * Algorithm, which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margins. Typically, each sector can be programmed and verified in about 2.2 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase™ * Algorithm, which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margins.

Any individual sector is typically erased and verified in 4.8 second. (If already preprogrammed.)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The device is erased when shipped from the factory.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, output pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device memory electrically erases all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The words/double words are programmed one word/double word at a time using the EPROM programming mechanism of hot electron injection.

*: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

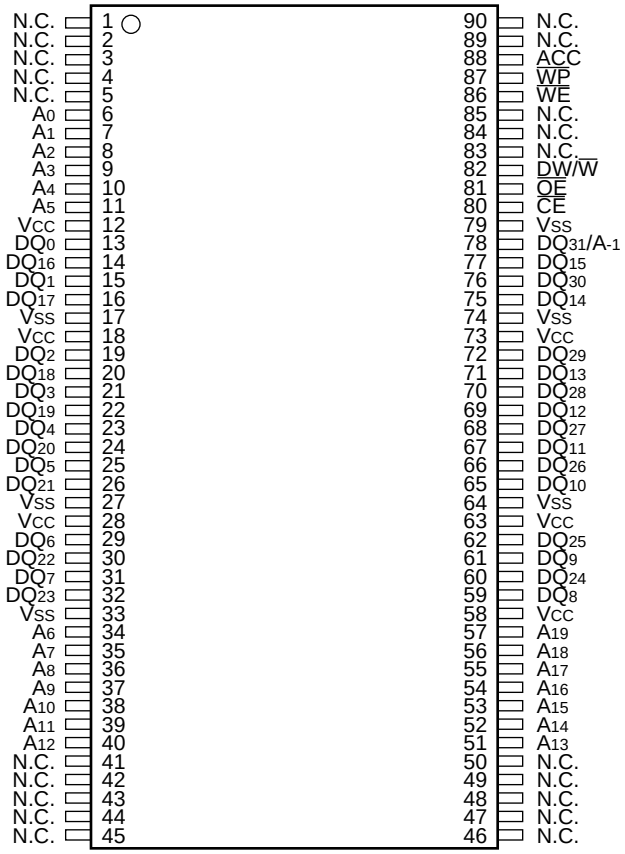
■ FEATURES

- **0.23 µm Process Technology**
- **Single 3.0 V read, program and erase**
  Minimized system level power requirements
- **High Performance Page Mode**
  25 ns maximum page access time (70 ns random access time)
- **8 words Page (× 16) /4 double words (× 32) size**
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
  90-pin SSOP (Package suffix : PFV)
  84-ball FBGA (Package suffix : PBT)
- **Minimum 100,000 program/erase cycles**
- **Sector erase architecture**
  One 16 K word, two 8 K words, one 96 K word, and fifteen 128 K words sectors in word mode (× 16)
  One 8 K double word, two 4 K double words, one 48 K double word, and fifteen 64 K double words sectors in double word mode (× 32)
  Any combination of sectors can be concurrently erased. Also supports full chip erase

- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Automatic sleep mode**
  When addresses remain stable, automatically switches themselves to low power mode
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector protection**
  Hardware method disables any combination of sectors from program or erase operations
- **Fast Programming Function by Extended command**
- **Temporary sector unprotection**
  Temporary sector unprotection with the software command
- **In accordance with CFI (Common Flash Memory Interface)**

■ PIN ASSIGNMENTS

SSOP
(TOP VIEW)



FPT-90P-M01

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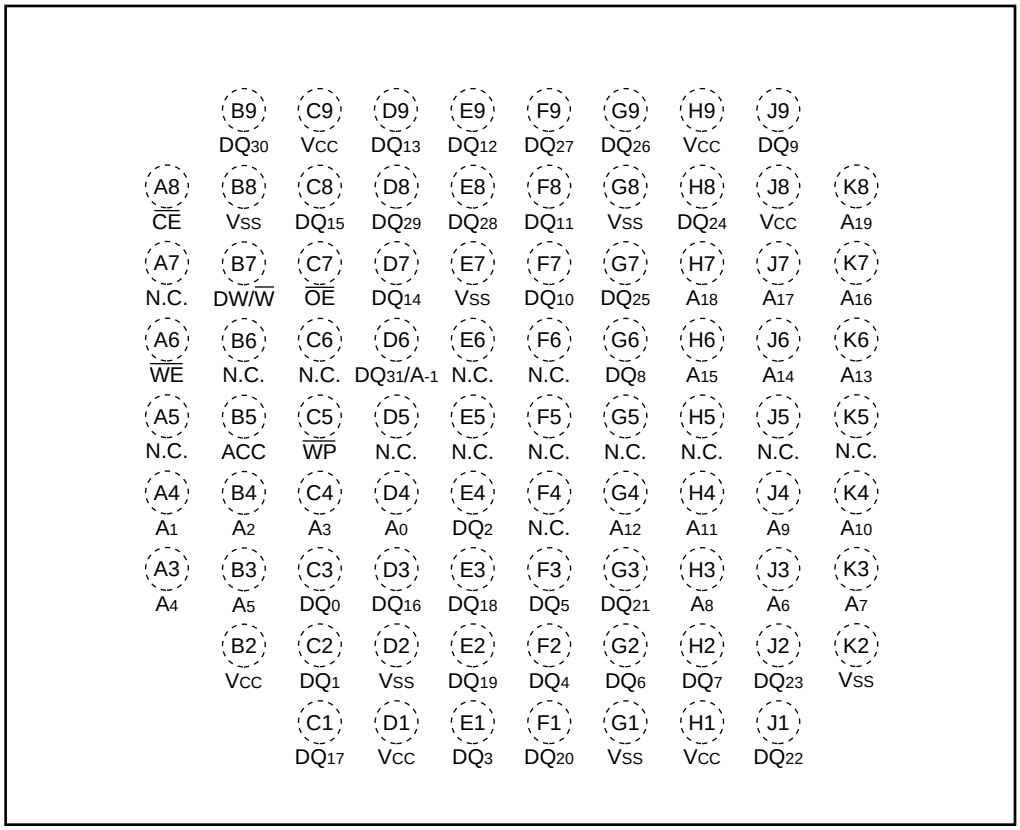
FBGA
(TOP VIEW)
Marking Side



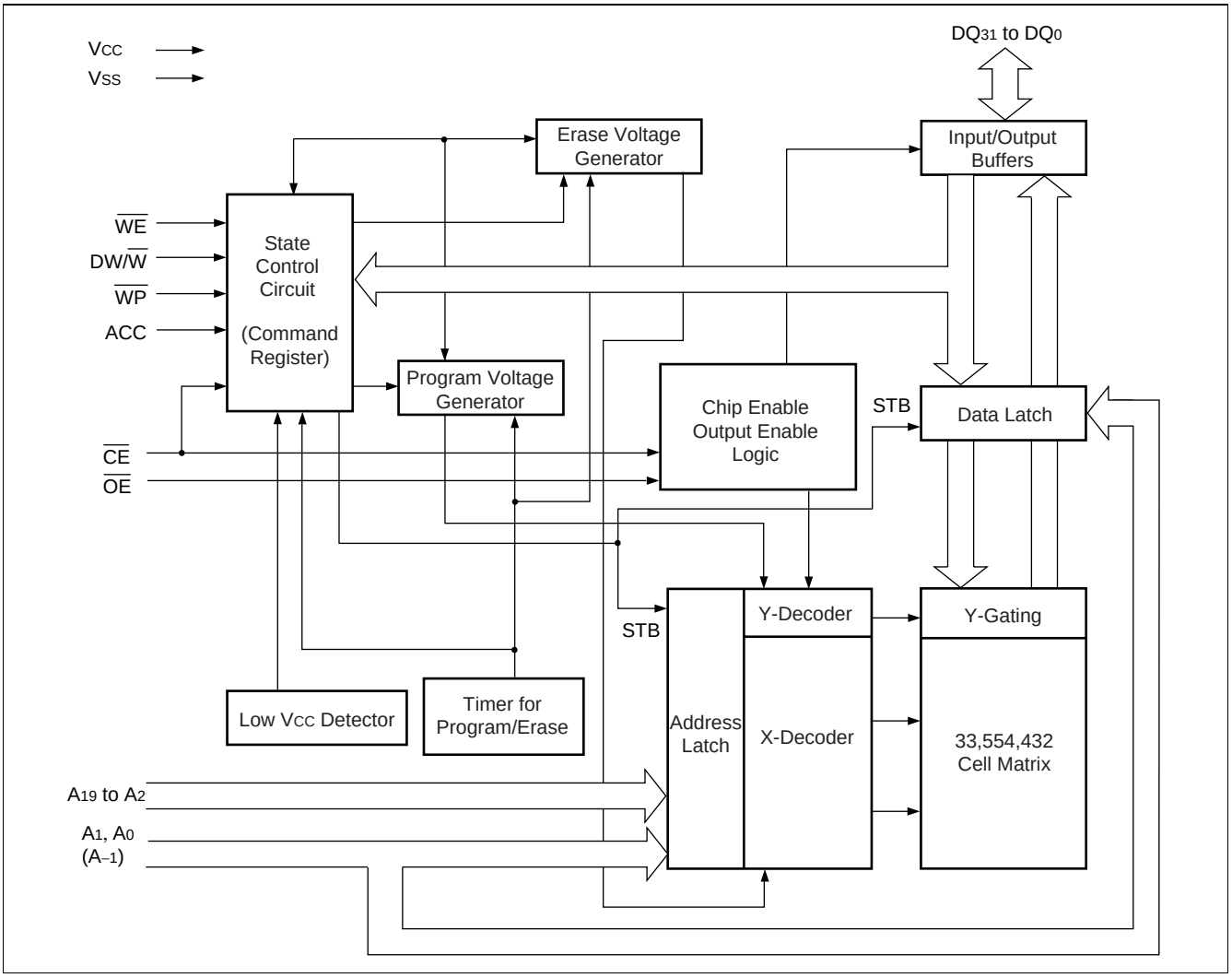
BGA-84P-M01

■ PIN DESCRIPTIONS

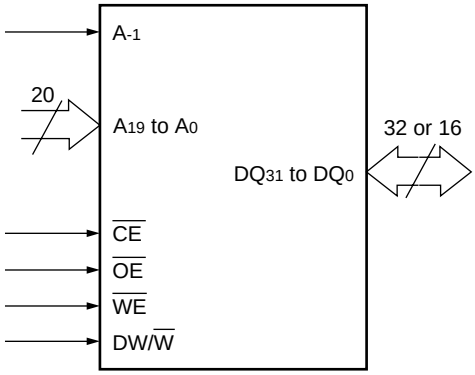
Table 1 MBM29PL3200TE/BE Pin Configuration

Pin Name	Function
A_{19} to A_0, A_{-1}	Address Input
DQ_{31} to DQ_0	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
DW/$\overline{W}$	Selects 32-bit or 16-bit mode
$\overline{WP}$	Hardware Write Protection
ACC	Program Acceleration
N.C.	Pin Not Connected Internally
V_{SS}	Device Ground
V_{CC}	Device Power Supply

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

Table 2 MBM29PL3200TE/BE User Bus Operations (DW/$\overline{W}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_2	A_3	A_6	A_9	DQ_{31} to DQ_0	$\overline{WP}$
Auto-Select Manufacturer Code *1	L	L	H	L	L	L	L	L	V_{ID}	Code	X
Auto-Select Device Code *1	L	L	H	H	L	L	L	L	V_{ID}	Code	X
Extended Auto-Select Device Code *1	L	L	H	H	H	H	H	L	V_{ID}	Code	X
Read *3	L	L	H	A_0	A_1	A_2	A_3	A_6	A_9	D_{OUT}	X
Standby	H	X	X	X	X	X	X	X	X	HIGH-Z	X
Output Disable	L	H	H	X	X	X	X	X	X	HIGH-Z	X
Write (Program/Erase)	L	H	L	A_0	A_1	A_2	A_3	A_6	A_9	D_{IN}	X
Enable Sector Protection *2, *4	L	V_{ID}	⎍	L	H	L	L	L	V_{ID}	X	X
Verify Sector Protection *2, *4	L	L	H	L	H	L	L	L	V_{ID}	Code	X
Boot Block Sector Write Protection *5	X	X	X	X	X	X	X	X	X	X	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ⎍ = Pulse input. See DC Characteristics for voltage levels.

*1: Manufacturer and device codes may also be accessed via a command register write sequence. See Table 4.

*2: Refer to section on Sector Protection.

*3: $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4: V_{CC} = 3.3 V ± 10%

*5: Protect “outermost” 16 K words (8 K double words) of the boot block sectors.

Table 3 MBM29PL3200TE/BE User Bus Operations (DW/$\overline{W}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{31}/A_{-1}	A_0	A_1	A_2	A_3	A_6	A_9	DQ_{15} to DQ_0	$\overline{WP}$
Auto-Select Manufacturer Code *1	L	L	H	L	L	L	L	L	L	V_{ID}	Code	X
Auto-Select Device Code *1	L	L	H	L	H	L	L	L	L	V_{ID}	Code	X
Extended Auto-Select Device Code *1	L	L	H	L	H	H	H	H	L	V_{ID}	Code	X
Read *3	L	L	H	A_{-1}	A_0	A_1	A_2	A_3	A_6	A_9	D_{OUT}	X
Standby	H	X	X	X	X	X	X	X	X	X	HIGH-Z	X
Output Disable	L	H	H	X	X	X	X	X	X	X	HIGH-Z	X
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_2	A_3	A_6	A_9	D_{IN}	X
Enable Sector Protection *2, *4	L	V_{ID}	⎍	L	L	H	L	L	L	V_{ID}	X	X
Verify Sector Protection *2, *4	L	L	H	L	L	H	L	L	L	V_{ID}	Code	X
Boot Block Sector Write Protection *5	X	X	X	X	X	X	X	X	X	X	X	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ⎍ = Pulse input. See DC Characteristics for voltage levels.

*1: Manufacturer and device codes may also be accessed via a command register write sequence. See Table 4.

*2: Refer to section on Sector Protection.

*3: $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4: V_{CC} = 3.3 V ± 10%

*5: Protect “outermost” 16 K words (8 K double words) of the boot block sectors.

Table 4 MBM29PL3200TE/BE Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	DW	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
	W													
Read/Reset	DW	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
	W		AAAh		555h		AAAh							
Autoselect	DW	3	555h	AAh	2AAh	55h	555h	90h	—	—	—	—	—	—
	W		AAAh		555h		AAAh							
Program	DW	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	W		AAAh		555h		AAAh							
Chip Erase	DW	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	W		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	DW	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	W		AAAh		555h		AAAh		AAAh		555h			
Erase Suspend		1	XXXh	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	XXXh	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	DW	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	W		AAAh		555h		AAAh							
Fast Program *1	DW	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	W		XXXh											
Reset from Fast Mode *1	DW	2	XXXh	90h	XXXh	*4 F0h	—	—	—	—	—	—	—	—
	W		XXXh		XXXh									
Temporary Unprotection Enable	DW	4	555h	AAh	2AAh	55h	555h	E0h	XXXh	01h	—	—	—	—
	W		AAAh		555h		AAAh							
Temporary Unprotection Disable	DW	4	555h	AAh	2AAh	55h	555h	E0h	XXXh	00h	—	—	—	—
	W		AAAh		555h		AAAh							
Query *2	DW	1	55h	98h	—	—	—	—	—	—	—	—	—	—
	W		AAh											
Hi-ROM Entry	DW	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
	W		AAAh		555h		AAAh							
Hi-ROM Program *3	DW	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—
	W		AAAh		555h		AAAh							
Hi-ROM Exit *3	DW	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h	—	—	—	—
	W		AAAh		555h		AAAh							

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DW : Double Word
W : Word

*1: This command is valid while Fast Mode.

*2: The valid addresses are A_6 to A_0.

*3: This command is valid while Hi-ROM mode.

*4: The data “00h” is also acceptable.

Notes : 1.Address bits A_{19} to A_{11} = X = “H” or “L” for all address commands except or Program Address (PA), and Sector Address (SA).
2.Bus operations are defined in Tables 2 and 3.
3.RA = Address of the memory location to be read
PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased. The combination of A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12} will uniquely select any sector.
4.RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the falling edge of write pulse.
5.HRA = Address of the Hi-ROM area Word Mode : 000000h to 000100h
Double Word Mode : 000000h to 000080h
6.The system should generate the following address patterns :
DW (Double Word) Mode : 555h or 2AAh to addresses A_{10} to A_0
W (Word) Mode : AAAh or 555h to addresses A_{10} to A_0, and A_{-1}
7.Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

Table 5.1 MBM29PL3200TE Sector Protection Verify Autoselect Codes

Type		A_{19} to A_{12}	A_6	A_3	A_2	A_1	A_0	A_{-1} *1	Code (HEX)
Manufacture's Code		X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	Word	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	227Eh
	Double Word							X	2222227Eh
Extended Device Code	Word	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	2203h
	Double Word							X	22222203h
	Word	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	2201h
	Double Word							X	22222201h
Sector Protection		Sector Addresses	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h *2
Temporary Sector Unprotection		X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	01h *3

*1 : A_{-1} is for Word mode. In double word mode, DQ_{15} to DQ_{30} become "High-Z" and DQ_{31} becomes the lower address "A_{-1}".

*2 : Outputs 01h at protected sector addresses and outputs 00h at unprotected sector addresses.

*3 : Outputs 01h at Temporary Sector Unprotection and outputs 00h at Non Temporary Sector Unprotection.

Table 5.2 Expanded Autoselect Code

Type		Code	DQ_{31}	DQ_{30}	DQ_{29}	DQ_{28}	DQ_{27}	DQ_{26}	DQ_{25}	DQ_{24}	DQ_{23}	DQ_{22}	DQ_{21}	DQ_{20}	DQ_{19}	DQ_{18}	DQ_{17}	DQ_{16}
Manufacturer's Code		04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Device Code	(W)	227Eh	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
	(DW)	2222 227Eh	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
Extended Device Code	(W)	2203h	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
	(DW)	2222 2203h	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
	(W)	2201h	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
	(DW)	2222 2201h	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
Sector Protection		01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Temporary Sector Unprotection		01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Type		DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_{9}	DQ_{8}	DQ_{7}	DQ_{6}	DQ_{5}	DQ_{4}	DQ_{3}	DQ_{2}	DQ_{1}	DQ_{0}
Manufacturer's Code		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	(W)	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
	(DW)	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
Extended Device Code	(W)	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1
	(DW)	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1
	(W)	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1
	(DW)	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1
Sector Protection		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Temporary Sector Unprotection		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(W) : Word mode
(DW) : Double Word mode

Table 5.3 MBM29PL3200BE Sector Protection Verify Autoselect Codes

Type		A_{19} to A_{12}	A_6	A_3	A_2	A_1	A_0	A_{-1} *1	Code (HEX)
Manufacture's Code		X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	Word	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	227Eh
	Double Word							X	2222227Eh
Extended Device Code	Word	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	2203h
	Double Word							X	22222203h
	Word	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	2200h
	Double Word							X	22222200h
Sector Protection		Sector Addresses	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h *2
Temporary Sector Unprotection		X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	01h *3

*1 : A_{-1} is for Word mode. In double word mode, DQ_{15} to DQ_{30} become "High-Z" and DQ_{31} becomes the lower address "A_{-1}".

*2 : Outputs 01h at protected sector addresses and outputs 00h at unprotected sector addresses.

*3 : Outputs 01h at Temporary Sector Unprotection and outputs 00h at Non Temporary Sector Unprotection.

Table 5.4 Expanded Autoselect Code

Type		Code	DQ_{31}	DQ_{30}	DQ_{29}	DQ_{28}	DQ_{27}	DQ_{26}	DQ_{25}	DQ_{24}	DQ_{23}	DQ_{22}	DQ_{21}	DQ_{20}	DQ_{19}	DQ_{18}	DQ_{17}	DQ_{16}
Manufacturer's Code		04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Device Code	(W)	227Eh	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
	(DW)	2222 227Eh	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
Extended Device Code	(W)	2203h	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
	(DW)	2222 2203h	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
	(W)	2200h	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
	(DW)	2222 2200h	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
Sector Protection		01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Temporary Sector Unprotection		01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Type		DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_{9}	DQ_{8}	DQ_{7}	DQ_{6}	DQ_{5}	DQ_{4}	DQ_{3}	DQ_{2}	DQ_{1}	DQ_{0}
Manufacturer's Code		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	(W)	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
	(DW)	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
Extended Device Code	(W)	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1
	(DW)	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1
	(W)	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
	(DW)	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
Sector Protection		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Temporary Sector Unprotection		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(W) : Word mode
(DW) : Double Word mode

Table 7 Sector Address (MBM29PL3200TE)

Sector	Sector Address								Sector Size (Kwords/ Double kwords)	(×16) Address Range	(×32) Address Range
	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
SA0	0	0	0	0	X	X	X	X	128/64	000000h to 01FFFFh	00000h to 0FFFFh
SA1	0	0	0	1	X	X	X	X	128/64	020000h to 03FFFFh	10000h to 1FFFFh
SA2	0	0	1	0	X	X	X	X	128/64	040000h to 05FFFFh	20000h to 2FFFFh
SA3	0	0	1	1	X	X	X	X	128/64	060000h to 07FFFFh	30000h to 3FFFFh
SA4	0	1	0	0	X	X	X	X	128/64	080000h to 09FFFFh	40000h to 4FFFFh
SA5	0	1	0	1	X	X	X	X	128/64	0A0000h to 0BFFFFh	50000h to 5FFFFh
SA6	0	1	1	0	X	X	X	X	128/64	0C0000h to 0DFFFFh	60000h to 6FFFFh
SA7	0	1	1	1	X	X	X	X	128/64	0E0000h to 0FFFFFh	70000h to 7FFFFh
SA8	1	0	0	0	X	X	X	X	128/64	100000h to 11FFFFh	80000h to 8FFFFh
SA9	1	0	0	1	X	X	X	X	128/64	120000h to 13FFFFh	90000h to 9FFFFh
SA10	1	0	1	0	X	X	X	X	128/64	140000h to 15FFFFh	A0000h to AFFFFh
SA11	1	0	1	1	X	X	X	X	128/64	160000h to 17FFFFh	B0000h to BFFFFh
SA12	1	1	0	0	X	X	X	X	128/64	180000h to 19FFFFh	C0000h to CFFFFh
SA13	1	1	0	1	X	X	X	X	128/64	1A0000h to 1BFFFFh	D0000h to DFFFFh
SA14	1	1	1	0	X	X	X	X	128/64	1C0000h to 1DFFFFh	E0000h to EFFFFh
SA15	1	1	1	1	0000 to 1011				96/48	1E0000h to 1F7FFFh	F0000h to FBFFFh
SA16	1	1	1	1	1	1	0	0	8/4	1F8000h to 1F9FFFh	FC000h to FEFFFh
SA17	1	1	1	1	1	1	0	1	8/4	1FA000h to 1FBFFFh	FD000h to FDFFFh
SA18	1	1	1	1	1	1	1	X	16/8	1FC000h to 1FFFFFh	FE000h to FFFFFh

Note : The address range is A_{19} to A_{-1} if in word mode (DW/$\overline{W}$ = V_{IL}).
The address range is A_{19} to A_0 if in double word mode (DW/$\overline{W}$ = V_{IH}).

Table 8 Sector Address (MBM29PL3200BE)

Sector	Sector Address								Sector Size (Kwords/ Double kwords)	(× 16) Address Range	(× 32) Address Range
	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
SA0	0	0	0	0	0	0	0	X	16/8	000000h to 003FFFh	00000h to 01FFFh
SA1	0	0	0	0	0	0	1	0	8/4	004000h to 005FFFh	02000h to 02FFFh
SA2	0	0	0	0	0	0	1	1	8/4	006000h to 007FFFh	03000h to 03FFFh
SA3	0	0	0	0	0100 to 1111				96/48	008000h to 01FFFFh	04000h to 0FFFFh
SA4	0	0	0	1	X	X	X	X	128/64	020000h to 03FFFFh	10000h to 1FFFFh
SA5	0	0	1	0	X	X	X	X	128/64	040000h to 05FFFFh	20000h to 2FFFFh
SA6	0	0	1	1	X	X	X	X	128/64	060000h to 07FFFFh	30000h to 3FFFFh
SA7	0	1	0	0	X	X	X	X	128/64	080000h to 09FFFFh	40000h to 4FFFFh
SA8	0	1	0	1	X	X	X	X	128/64	0A0000h to 0BFFFFh	50000h to 5FFFFh
SA9	0	1	1	0	X	X	X	X	128/64	0C0000h to 0DFFFFh	60000h to 6FFFFh
SA10	0	1	1	1	X	X	X	X	128/64	0E0000h to 0FFFFFh	70000h to 7FFFFh
SA11	1	0	0	0	X	X	X	X	128/64	100000h to 11FFFFh	80000h to 8FFFFh
SA12	1	0	0	1	X	X	X	X	128/64	120000h to 13FFFFh	90000h to 9FFFFh
SA13	1	0	1	0	X	X	X	X	128/64	140000h to 15FFFFh	A0000h to AFFFFh
SA14	1	0	1	1	X	X	X	X	128/64	160000h to 17FFFFh	B0000h to BFFFFh
SA15	1	1	0	0	X	X	X	X	128/64	180000h to 19FFFFh	C0000h to CFFFFh
SA16	1	1	0	1	X	X	X	X	128/64	1A0000h to 1BFFFFh	D0000h to DFFFFh
SA17	1	1	1	0	X	X	X	X	128/64	1C0000h to 1DFFFFh	E0000h to EFFFFh
SA18	1	1	1	1	X	X	X	X	128/64	1E0000h to 1FFFFFh	F0000h to FFFFFh

Note : The address range is A_{19} to A_{-1} if in word mode (DW/$\overline{W}$ = V_{IL}).
The address range is A_{19} to A_0 if in double word mode (DW/$\overline{W}$ = V_{IH}).

Table 9 Common Flash Memory Interface Code

A_6 to A_0	DQ_{15} to DQ_0	Description
10h 11h 12h	0051h 0052h 0059h	Query-unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set 2h : AMD/FJ standard type
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = not applicable)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table
1Bh	0027h	V_{CC} Min. (write/erase) D7-4 : 1 V, D3-0 : 100 mV
1Ch	0036h	V_{CC} Max. (write/erase) D7-4 : 1 V, D3-0 : 100 mV
1Dh	0000h	V_{PP} Min. voltage
1Eh	0000h	V_{PP} Max. voltage
1Fh	0004h	Typical timeout per single byte/word write (2^N µs)
20h	0000h	Typical timeout for Min. size buffer write (2^N µs)
21h	000Ah	Typical timeout per individual block erase (2^N ms)
22h	0000h	Typical timeout for full chip erase (2^N ms)
23h	0005h	Max. timeout for byte/word write ($2^N \times$ typical time)
24h	0000h	Max. timeout for buffer write ($2^N \times$ typical time)
25h	0006h	Max. timeout per individual block erase ($2^N \times$ typical time)
26h	0000h	Max. timeout for full chip erase ($2^N \times$ typical time)
27h	0016h	Device Size = 2^N byte
28h 29h	0005h 0000h	Flash Device Interface description
2Ah 2Bh	0000h 0000h	Max. number of bytes in multi-byte write = 2^N
2Ch	0004h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0000h 0000h 0080h 0000h	Erase Block Region 1 Information Bit0 to 15: y = Number of sectors Bit16 to 31: z = Size (Z × 256 Byte)
31h 32h 33h 34h	0001h 0000h 0040h 0000h	Erase Block Region 2 Information Bit0 to 15: y = Number of sectors Bit16 to 31: z = Size (Z × 256 Byte)
35h 36h 37h 38h	0000h 0000h 0000h 0003h	Erase Block Region 3 Information Bit0 to 15: y = Number of sectors Bit16 to 31: z = Size (Z × 256 Byte)
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0000h	Address Sensitive Unlock 0h = Required 1h = Not Required
46h	0002h	Erase Suspend 0h = Not Supported 1h = To Read Only 2h = To Read & Write
47h	0001h	Sector Protection 0h = Not Supported X = Number of sectors per group
48h	0001h	Sector Temporary Unprotection 00h = Not Supported 01h = Supported
49h	0003h	Sector Protection Algorithm
4Ah	0000h	00h = Not Supported, X = Total number of sectors in all Banks except Bank 1
4Bh	0000h	Burst Mode Type 00h = Not Supported
4Ch	0002h	Page Mode Type 00h = Not Supported

(Continued)

(Continued)

A_6 to A_0	DQ_{15} to DQ_0	Description
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-4 : 1 V, D3-0 : 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-4 : 1 V, D3-0 : 100 mV
4Fh	00XXh	Boot Type 02h = MBM29PL3200BE 03h = MBM29PL3200TE

Note : DQ_{31} to DQ_{16} = “0000h”

■ FUNCTIONAL DESCRIPTION

Read Mode

The device has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins when a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable prior to $t_{ACC} - t_{OE}$ time). When reading out data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from “H” to “L”.

Page Mode Read

The device is capable of fast Page mode read and is compatible with the Page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The Page size of the device is 8 words, or 4 double words, within the appropriate Page being selected by the higher address bits A_{19} to A_2 and the LSB bits A_1 to A_0 (in double word mode) and A_1 to A_{-1} (in word mode) determining the specific double word/word within that page. This is an asynchronous operation with the microprocessor supplying the specific double word or word location.

The random or initial page access is equal to t_{ACC} and subsequent Page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to t_{PACC}. Here again, $\overline{CE}$ selects the device and $\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected. Fast Page mode accesses are obtained by keeping A_{19} to A_2 constant and changing A_1 and A_0 to select the specific double word, or changing A_1 to A_{-1} to select the specific word within that page. See Figure 5.2 for timing specifications.

Standby Mode

The device has CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.3$ V.), when the current consumed is less than 50 μA. In the standby mode, the output pins are in a high impedance state, independent of $\overline{OE}$ input.

During Embedded Algorithm operation, V_{CC} Active current (I_{CC2}) is required even if $\overline{CE}$ = “H”. The device can be read with standard access time (t_{CE}) from either of these standby modes.

In the standby mode, the output pins are in the high impedance state, independent of $\overline{OE}$ input.

Automatic Sleep Mode

Automatic sleep mode lower consumption during read-out of the device data. This mode can be useful for applications such as a handy terminal that requires low power consumption.

To activate this mode, the device automatically switches itself to low power mode when addresses remain stable during access time of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ in this mode. In this mode, the current consumed is typically 50 μA (CMOS Level).

Since the data are latched during this mode, they are read out continuously. If the addresses are changed, this mode is canceled automatically, and the device reads the data for changed addresses.

Output Disable

With the $\overline{OE}$ input is at a logic high level (V_{IH}), output from the device is disabled. This will put the output pins in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9. Three identifier words may then be sequenced from the device outputs by toggling address A_0 and A_1 from V_{IL} to V_{IH}. All addresses are DON'T CAREs except A_6, A_3, A_2, A_1, and A_0 (A_{-1}). (See Tables 2 and 3.)

The manufacturer and device codes may also be read via the command register, for instance when the device is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 11. (Refer to Autoselect Command section.)

A read cycle from address 00h returns the manufacturer's code (Fujitsu = 04h). A read cycle from address 01h, 0Eh to 0Fh returns the device code. (See Tables 5.1 to 5.4.)

In order to determine which sectors are write protected, A_1 must be at V_{IH} while running through the sector addresses; if the selected sector is protected, a logical '1' will be output on DQ_0 (DQ_0 = 1).

Write

The device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later, while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The device features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 18). The sector protection feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, $\overline{CE}$ = V_{IL}, $A_6 = A_3 = A_2 = A_0 = V_{IL}$, $A_1 = V_{IH}$. The sector address pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. Tables 7 and 8 define the sector address for each of the nineteen (19) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See Figures 15 and 21 for sector protection waveforms and algorithms.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector. Otherwise the device will read 00h for an unprotected sector. In this mode, the lower order address, except for A_0, A_1 and A_6 are DON'T CAREs. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes. A_{-1} requires to V_{IL} in word mode.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order address pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) represents the sector address will produce a logical "1" at DQ_0 for a protected sector. See Tables 5.1 to 5.4 for Autoselect codes.

Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the device in order to change data. The Sector Unprotection mode is activated by the command register. In this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the mode is taken away using the command register, all previously protected sectors will be protected again. (See Figure 22.)

Boot Block Sector Protection

The Write Protection function provides a hardware method of protecting certain “outermost” 16 K word (× 16 mode) sector without using V_{ID}.

If the system asserts V_{IL} on the $\overline{WP}$ pin, the device disables program and erase functions in the “outermost” 16 K word sector independently of whether this sector was protected or unprotected using the method described in “Sector Protection/Unprotection”. The outermost 16 K word sector is the highest addresses in MBM29PL3200TE, or the lowest addresses in MBM29PL3200BE.

(MBM29PL3200TE : SA18, MBM29PL3200BE : SA0)

If the system asserts V_{IL} on the $\overline{WP}$ pin, the device reverts to whether the outermost 16 K word sector was last set to be protected or unprotected. That is, sector protection or unprotection for this sector depends on whether this was last protected or unprotected using the method described in “Sector protection/unprotection”.

Accelerated Program Operation

The device offers accelerated program operation which enables high-speed programming. If the system asserts V_{ACC} to the ACC pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 60%. This function is primarily intended to allow high-speed programming, so caution is needed as the sector group will temporarily be unprotected.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device is automatically set to fast mode. Therefore, the present sequence could be used for programming and detection of completion in acceleration mode.

Removing V_{ACC} from the ACC pin returns the device to normal operation. Do not remove V_{ACC} from the ACC pin while programming. See Figure 16.

■ COMMAND DEFINITIONS

The device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in an improper sequence will reset the device to the read mode. Table 4 defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_{15} to DQ_0 and DQ_{31} to DQ_{16} bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits ($DQ_5 = 1$) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, both manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register. Following the last command write, a read cycle from address XX00h retrieves the manufacture code of 04h. A read cycle at address XX01h (XX02h for ×8) returns 7Eh indicating that this device uses an extended device code. The successive read cycle from XX0Eh to XX0Fh returns this extended device code for this device. (See Tables 5.1 to 5.4.)

The sector state (protection or unprotection) will be indicated by address XX02h for × 32 (XX04h for × 16). Scanning the sector addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) while (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector. The programming verification should perform margin mode verification on the protected sector. (See Tables 2 and 3.)

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register and to write the Autoselect command during the operation by executing it after writing the Read/Reset command sequence.

Word/Double Word Programming

The device is programmed on a word-by-word (or double word-by-double word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later, and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of the last $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. (See Figures 6 and 7.)

The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling), or DQ_6 (Toggle Bit). The $\overline{Data}$ Polling and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit. Then, the device return to the read mode and addresses are no longer latched. (See Table 10, Hardware Sequence Flags.) Therefore, the device requires that a valid address be supplied by the system at this time. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Figure 17 illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six-bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence, the device will automatically program and verify the entire memory for an all-zero data pattern prior to electrical erase (Preprogram Function). The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling), or DQ_6 (Toggle Bit). The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section), at which time the device returns to the read mode.

Chip Erase Time = Sector Erase Time × All sectors + Chip Program Time (Preprogramming)

Figure 18 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later, while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, which happens first. After time-out of “t_{TOW}” from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on Table 4. This sequence is followed with writes of the Sector Erase command (30h) to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “t_{TOW}”, or that command will not be accepted and erasure will not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of “t_{TOW}” from the rising edge of last $\overline{CE}$ or $\overline{WE}$, whichever happens first, will initiate the execution of the Sector Erase command (s). If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first, occurs within the “t_{TOW}” time-out window, the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open; see section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. In that case, restart the erase on those sectors and allow them to complete. (Refer to Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 19).

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector (s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors, the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling) or DQ_6 (Toggle Bit).

The sector erase begins after the “t_{TOW}” time out from the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first ,for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (See Write Operation Status section), at which time the device returns to the read mode. $\overline{\text{Data}}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time = [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase.

Erase Suspend/Resume

The Erase Suspend/Resume command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. Erase suspend command is applicable ONLY during the Sector Erase operation, which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The addresses are “DON’T CAREs” when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “t_{SPD}” to suspend the erase operation. When the device has entered the erase-suspended mode, the DQ_7 bit will be at logic “1” and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode will become the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the $\overline{\text{Data}}$ polling of DQ_7 or by the Toggle Bit I (DQ_6), which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

The device has a Fast Mode function. This mode dispenses with the initial two unlock cycles required in the standard program command sequence by writing a Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write a Fast Mode Reset command into the command register. (Refer to Figure 23.) The V_{CC} active current is required even if $\overline{CE} = V_{IH}$ during Fast Mode.

(2) Fast Programming

In Fast Mode, the programming can be executed with two bus cycle operation. The Embedded Program Algorithm is executed by writing a program set-up command (A0h) and data write cycles (PA/PD). (Refer to Figure 23.)

(3) CFI (Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines the device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of the device. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrieves device information. Please note that output data of upper byte (DQ_{15} to DQ_8) is “0” in word mode (16 bit) read. Refer to the CFI code table. To terminate operation, it is necessary to write the Read/Reset command sequence into the register.

Hidden ROM (Hi-ROM) Region

The Hi-ROM feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the Hi-ROM region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.

The Hi-ROM region is 512 words in length. After the system has written the Enter Hi-ROM command sequence, it may read the Hidden ROM region by using device addresses A_7 to A_0 (A_{11} to A_8 are "00", A_{19} to A_{12} are don't care). That is, the device sends only program command that would normally be sent to the address to the Hi-ROM region. This mode of operation continues until the system issues the Exit Hi-ROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the address.

Hidden ROM (Hi-ROM) Entry Command

The device has a Hidden ROM area with One Time Protect function. This area is to enter the security code and to unable the change of the code once set. Program/erase is possible in this area until it is protected. However, once it is protected, it is impossible to unprotect, so please use this with caution.

Hidden ROM area is 512 words. This area is normally the "outermost" 16 K word boot block area. Therefore, write the Hidden ROM entry command sequence to enter the Hidden ROM area. It is called Hidden ROM mode when the Hidden ROM area appears.

Hidden ROM (Hi-ROM) Program Command

To program the data to the Hidden ROM area, write the Hidden ROM program command sequence during Hidden ROM mode. This command is the same as the program command in usual except to write the command during Hidden ROM mode. Therefore the detection of completion method is the same as in the past, using the DQ_7 data polling, and DQ_6 toggle bit. Need to pay attention to the address to be programmed. If the address other than the Hidden ROM area is selected to program, data of the address will be changed.

Hidden ROM (Hi-ROM) Protect Command

The method to protect the Hidden ROM is to apply high voltage (V_{ID}) to A_9 and $\overline{OE}$, set the sector address in the Hidden ROM area and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0), and apply the write pulse during the Hidden ROM mode. To verify the protect circuit, apply high voltage (V_{ID}) to A_9, specify (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) and the sector address in the Hidden ROM area, and read. When "1" appears on DQ_0, the protect setting is completed. "0" will appear on DQ_0 if it is not protected. Please apply write pulse agian. The same command sequence could be used for the above method because other than the Hidden ROM mode, it is the same as the sector protect in the past. Please refer to "Function Explanation Secor Protection" for details of the sector protect setting.

Other sector will be effected if the address other than those for Hidden ROM area is selected for the sector address, so please be carefull. Once it is protected, protection can not be cancelled, so please pay the closest attention.

Write Operation Status

Detailed in Table 10 are all the status flags that can be used to check the status of the device for current mode operation. During sector erase, the part provides the status flags automatically to the I/O ports. The information on DQ_2 is address sensitive. This means that if an address from an erasing sector is consecutively read, then the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows users to determine which sectors are in erase and which are not.

Once erase suspend is entered, address sensitivity still applies. If the address of a non-erasing sector (that is, one available for read) is provided, then stored data can be read from the device. If the address of an erasing sector (that is, one unavailable for read) is applied, the device will output its status bits.

Table 10 Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle *
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1 *
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspend Program (Non-Erase Suspended Sector)		$\overline{DQ_7}$	Toggle	1	0	N/A

*: Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

Notes : 1.DQ_0 and DQ_1 are reserve pins for future use.
2.DQ_4 is Fujitsu internal use only.

DQ_7
$\overline{\text{Data}}$ Polling

The device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce a complement of data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" on DQ_7. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in Figure 19.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at the sector address of sectors being erased, not protected sectors. Otherwise, the status may be invalid.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ_7 at one instant and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ_7 has valid data, data outputs on DQ_6 to DQ_0 may be still invalid. The valid data on DQ_7 to DQ_0 will be read on successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See Table 10.)

See Figure 9 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ_6
Toggle Bit I

The device also features the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written is protected, the toggle bit will toggle for about 1 µs and then stop toggling with data unchanged. In erase, device will erase all selected sectors except for ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 µs and then drop back into read mode, having data unchanged.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ_6 to toggle.

See Figure 10 and Figure 20 for the Toggle Bit I timing specifications and diagrams.

DQ_5
Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is only operating function of device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Tables 2 and 3.

The DQ_5 failure condition may also appear if a user tries to program a non-blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads valid data on DQ_7 bit and DQ_6 never stops toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a “1.” Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device with the command sequence.

DQ_3
Sector Erase Timer

After completion of the initial sector erase command sequence, sector erase time-out will begin. DQ_3 will remain low until the time-out is completed. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates that the device has been written with a valid erase command, DQ_3 may be used to determine whether the sector erase timer window is still open. If DQ_3 is high (“1”), the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit I. If DQ_3 is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 is high on the second status check, the command may not have been accepted.

See Table 10 : Hardware Sequence Flags.

DQ_2
Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic “1” at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows :

For example, DQ_2 and DQ_6 can be used together to determine whether the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also Table 11 and Figure 11.

Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Reading Toggle Bits DQ_6/DQ_2

Whenever the system initially begins reading toggle bit status, it must read DQ_7 to DQ_0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ_7 to DQ_0 on the following read cycle.

However, if, after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ_5 is high (see the section on DQ_5). If it is the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ_5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ_5 has not gone high. The system may continue to monitor the toggle bit and DQ_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to Figure 20.)

Table 11 Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle (Note)
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1 (Note)

Note : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

Double Word/Word Configuration

DW/$\overline{W}$ pin selects double word (32-bit) mode or word (16-bit) mode for the device. When this pin is driven high, the device operates in the double word (32-bit) mode. Data is read and programmed at DQ_{31} to DQ_0. When this pin is driven low, the device operates in word (16-bit) mode. In this mode, the DQ_{31}/A_{-1} pin becomes the lowest address bit, and DQ_{30} to DQ_{16} bits are tri-stated. However, the command bus cycle is always an 16-bit operation and hence commands are written at DQ_{31} to DQ_{16} and DQ_{15} to DQ_0 bits are ignored. Refer to Figures 12, 13 and 14 for the timing diagram.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power-up, the device automatically resets the internal state machine to Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of the specific multi-bus cycle command sequence.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} (Min.). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO} (Min.).

If the Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector (s) can not be used.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be "L" while $\overline{OE}$ is a logical one.

Power-up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	Ta	–40	+85	°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, and ACC *1	V_{IN}, V_{OUT}	–0.5	V_{CC} + 0.5	V
Power Supply Voltage *1	V_{CC}	–0.5	+4.0	V
A_9, $\overline{OE}$, and ACC *2	V_{IN}	–0.5	+13.0	V

*1: Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

*2: Minimum DC input voltage on A_9, $\overline{OE}$ and ACC pins is –0.5 V. During voltage transitions, A_9, $\overline{OE}$ and ACC pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage ($V_{IN} – V_{CC}$) does not exceed 9.0 V. Maximum DC input voltage on A_9, $\overline{OE}$ and ACC pins is +13.0 V which may overshoot to 14.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Part No.	Value		Unit
			Min.	Max.	
Ambient Temperature	Ta	MBM29PL3200TE/BE 70	–20	+70	°C
		MBM29PL3200TE/BE 90	–40	+85	
Power Supply Voltage	V_{CC}	MBM29PL3200TE/BE 70	+3.0	+3.6	V
		MBM29PL3200TE/BE 90	+2.7	+3.6	

Operating ranges define those limits between which the functionality of the device is quaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT/UNDERSHOOT

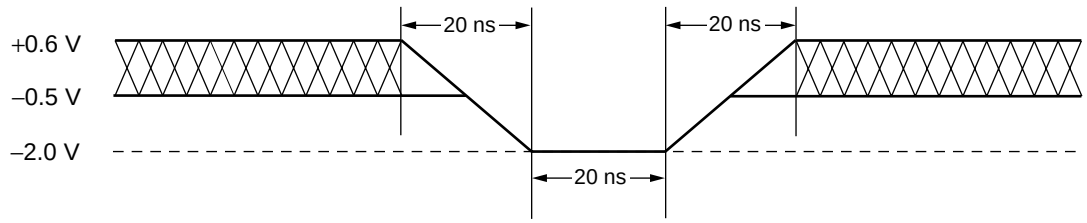


Figure 1 Maximum Undershoot Waveform

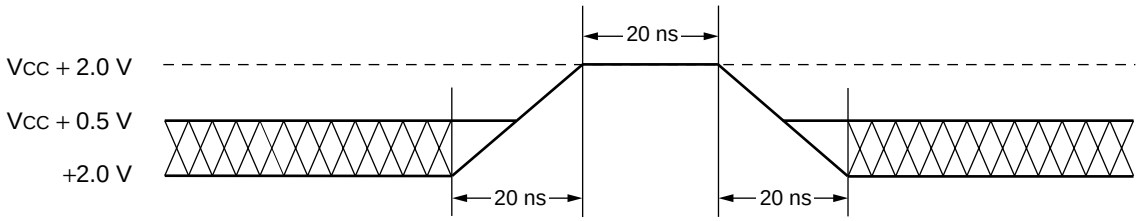
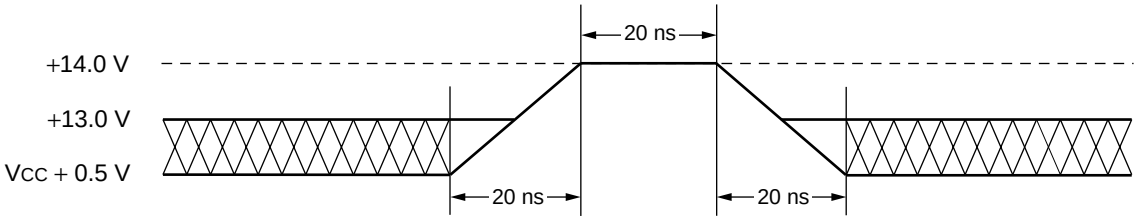


Figure 2 Maximum Overshoot Waveform 1



Note : This waveform is applied for A_9, $\overline{OE}$ and ACC.

Figure 3 Maximum Overshoot Waveform 2

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Conditions		Value Min.	Value Max.	Unit
Input Leakage Current (except $\overline{WP}$, ACC)	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		–1.0	+1.0	µA
Output Leakage Current (except $\overline{WP}$, ACC)	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		–1.0	+1.0	µA
Input Leakage Current ($\overline{WP}$, ACC)	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		–2.0	+2.0	µA
Output Leakage Current ($\overline{WP}$, ACC)	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		–2.0	+2.0	µA
A_9, $\overline{OE}$, ACC Inputs Leakage Current	I_{LIT}	V_{CC} = V_{CC} Max., A_9, $\overline{OE}$, ACC = 12.5 V		—	35	µA
V_{CC} Active Current (Read) *1	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} f = 10 MHz	Word	—	80	mA
			Double Word		80	
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} f = 5 MHz	Word	—	50	mA
			Double Word		50	
V_{CC} Active Current (Program/Erase) *2	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	80	mA
V_{CC} Current (Standby)	I_{CC3}	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ± 0.3 V		—	5	µA
V_{CC} Current (Automatic Sleep Mode) *3	I_{CC4}	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{SS} ± 0.3 V, V_{IN} = V_{CC} ± 0.3 V or V_{SS} ± 0.3 V		—	5	µA
V_{CC} Active Current (Page Read Mode)	I_{CC5}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	30 MHz	—	12	mA
			40 MHz	—	15	
ACC Accelerated Program Current	I_{ACC}	V_{CC} = V_{CC} Max., ACC = V_{ACC} Max.		—	20	mA
Input Low Level	V_{IL}	—		–0.5	0.8	V
Input High Level	V_{IH}	—		2.0	V_{CC} + 0.3	V
Voltage for Program Acceleration *4	V_{ACC}	—		11.5	12.5	V
Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$) *4	V_{ID}	—		11.5	12.5	V
Output Low Voltage Level	V_{OL}	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min.		—	0.45	V
Output High Voltage Level	V_{OH1}	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min.		2.4	—	V
	V_{OH2}	I_{OH} = –100 µA		V_{CC} – 0.4	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—		2.3	2.5	V

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Erase or Embedded Program is in progress.

*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

*4: (V_{ID} – V_{CC}) do not exceed 9 V.

2. AC Characteristics

(1) Read Only Operations Characteristics

Parameter	Symbol		Condition	Value				Unit
				70 *1		90 *2		
	JEDEC	Standard		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	90	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	—	90	ns
Page Read Cycle Time	—	t_{PRC}	—	25		35		ns
Page Address to Output Delay	—	t_{PACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	25	—	35	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	70	—	90	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	25	—	35	ns
Chip Enable to Output HIGH-Z	t_{EHQZ}	t_{DF}	—	—	25	—	30	ns
Output Enable to Output HIGH-Z	t_{GHQZ}	t_{DF}	—	—	25	—	30	ns
Output Hold Time From Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	4	—	5	—	ns
$\overline{CE}$ or DW/$\overline{W}$ Switching Low or High	—	t_{ELFL} t_{ELFH}	—	—	5	—	5	ns

*1: Test Conditions :
Output Load : 1 TTL gate and 50 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V to 3.0 V
Timing measurement reference level
Input : 1.5 V
Output : 1.5 V

*2 Test Conditions :
Output Load : 1 TTL gate and 100 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V to 3.0 V
Timing measurement reference level
Input : 1.5 V
Output : 1.5 V

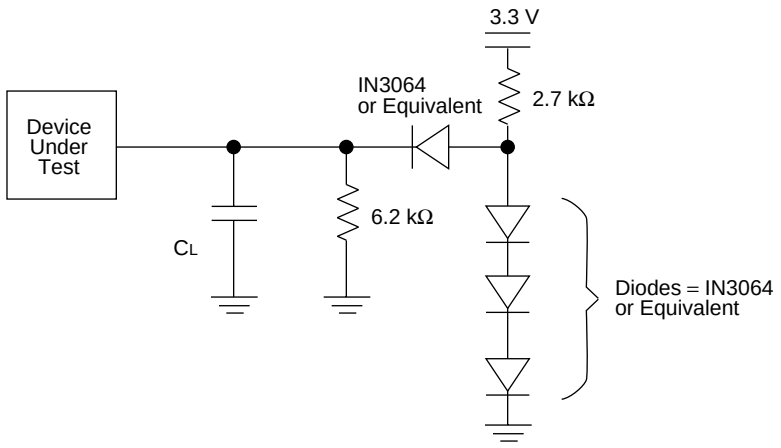


Figure 4 Test Conditions

(2) Write (Erase/Program) Operations

Symbol		Parameter		Value						Unit
				70 *1			90 *2			
JEDEC	Standard			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time		70	—	—	90	—	—	ns
t_{AVWL}	t_{AS}	Address Setup Time		0	—	—	0	—	—	ns
t_{WLAX}	t_{AH}	Address Hold Time		45	—	—	45	—	—	ns
t_{DVWH}	t_{DS}	Data Setup Time		35	—	—	45	—	—	ns
t_{WHDX}	t_{DH}	Data Hold Time		0	—	—	0	—	—	ns
—	t_{OES}	Output Enable Setup Time		0	—	—	0	—	—	ns
—	t_{OEH}	Output Enable Hold Time	Read	0	—	—	0	—	—	ns
			Toggle and $\overline{\text{Data}}$ Polling	10	—	—	10	—	—	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		0	—	—	0	—	—	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		0	—	—	0	—	—	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		0	—	—	0	—	—	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		0	—	—	0	—	—	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		0	—	—	0	—	—	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		0	—	—	0	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width		35	—	—	35	—	—	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		35	—	—	35	—	—	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High Level		30	—	—	30	—	—	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High Level		30	—	—	30	—	—	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Double Word	—	18.3	—	—	18.3	—	µs
			Word	—	14.3	—	—	14.3	—	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation *3		—	4	—	—	4	—	s
—	t_{VCS}	V_{CC} Setup Time		50	—	—	50	—	—	µs
—	t_{VIDR}	Rise Time to V_{ID} *4		500	—	—	500	—	—	ns
—	t_{VACCR}	Rise Time to V_{ACC} *5		500	—	—	500	—	—	ns
—	t_{VLHT}	Voltage Transition Time *4		4	—	—	4	—	—	µs
—	t_{WPP}	Write Pulse Width *4		100	—	—	100	—	—	µs
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active *4		4	—	—	4	—	—	µs
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active *4		4	—	—	4	—	—	µs
—	t_{EOE}	Delay Time from Embedded Output Enable		—	—	70	—	—	90	ns
—	t_{FLQZ}	DW/$\overline{W}$ Switching Low to Output HIGH-Z		—	—	30	—	—	30	ns
—	t_{FHQV}	DW/$\overline{W}$ Switching High to Output Active		35	—	—	30	—	—	ns
—	t_{TOW}	Erase Time-out Time		50	—	—	50	—	—	µs
—	t_{SPD}	Erase Suspend Transition Time		—	—	20	—	—	20	µs

*1: Test Conditions :
Output Load : 1 TTL gate and 50 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V to 3.0 V
Timing measurement reference level
Input : 1.5 V
Output : 1.5 V

*2 Test Conditions :
Output Load : 1 TTL gate and 100 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V to 3.0 V
Timing measurement reference level
Input : 1.5 V
Output : 1.5 V

*3: This does not include the preprogramming time.

*4: This timing is for Sector Protection operation.

*5: This timing is for Accelerated Program operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Value			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	4	40	s	Excludes programming time prior to erasure
Word Programming Time	—	14.3	360	µs	Excludes system-level overhead
Double Word Programming Time	—	18.3	480		
Chip Programming Time	—	20	280	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

■ PIN CAPACITANCE

Parameter	Symbol	Condition	Value		Unit
			Typ.	Max.	
Input Capacitance	C_{IN}	V_{IN} = 0	6	7.5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8	10.0	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8	10.0	pF

Note : Test conditions Ta = 25 °C, f = 1.0 MHz

■ FBGA PIN CAPACITANCE

Parameter	Symbol	Condition	Value		Unit
			Typ.	Max.	
Input Capacitance	C_{IN}	V_{IN} = 0	TBD	TBD	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	TBD	TBD	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	TBD	TBD	pF

Note : Test conditions Ta = 25 °C, f = 1.0 MHz

■ SWITCHING WAVEFORMS

- **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Change from H to L
	May Change from L to H	Will Be Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

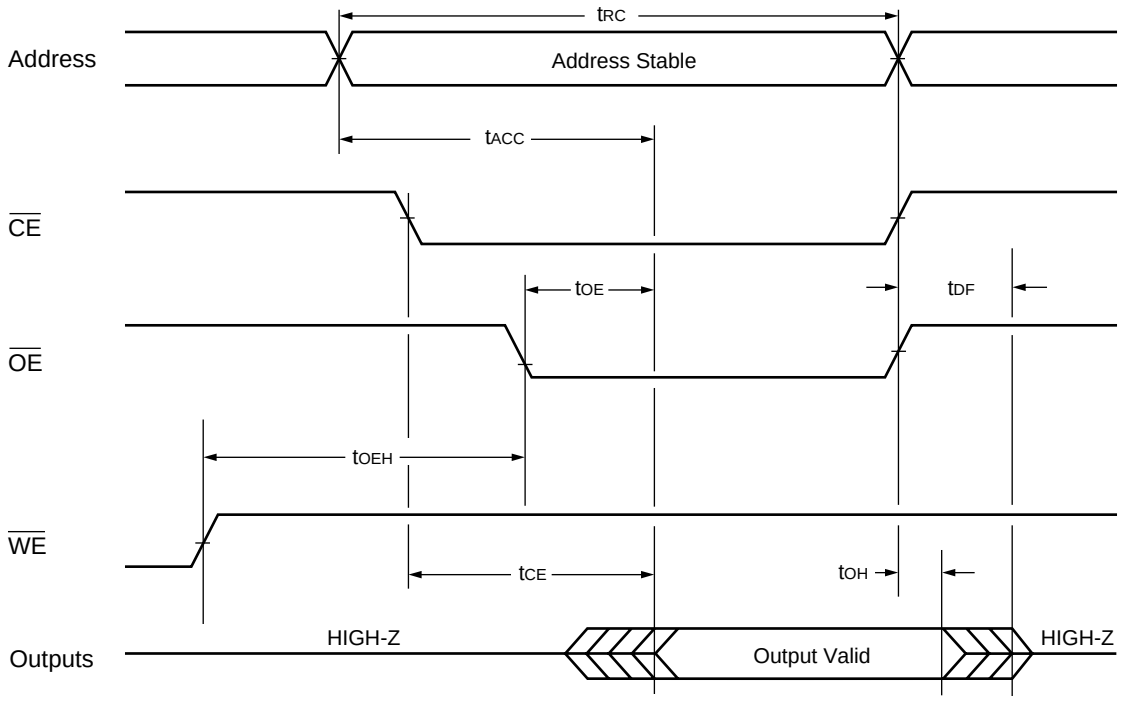


Figure 5.1 Read Operation Timing Diagram

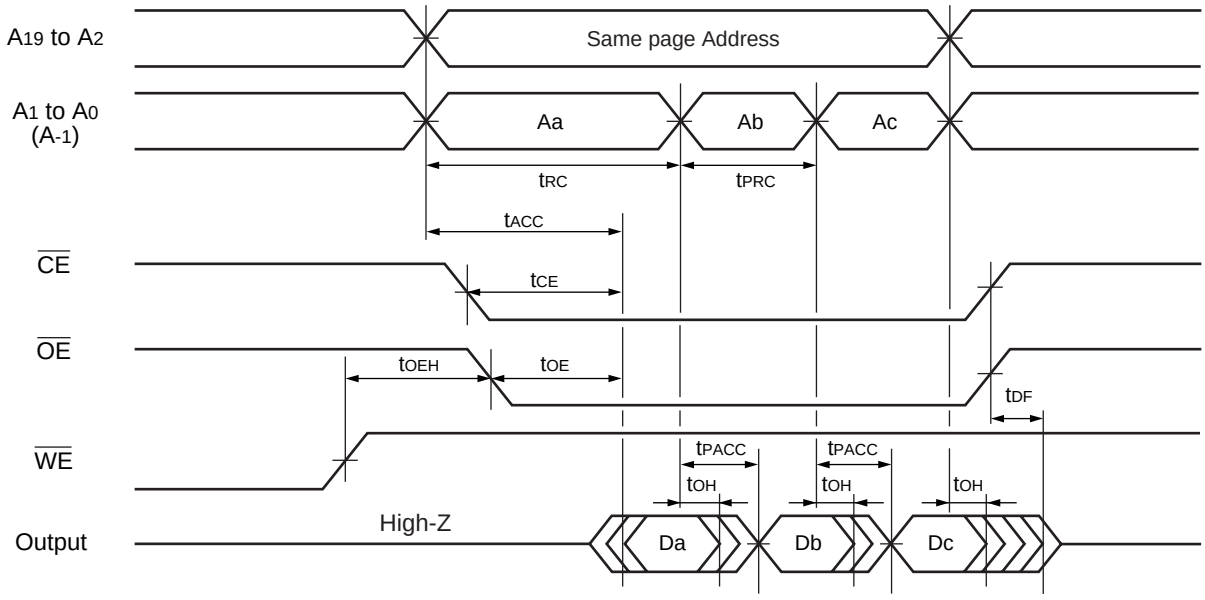
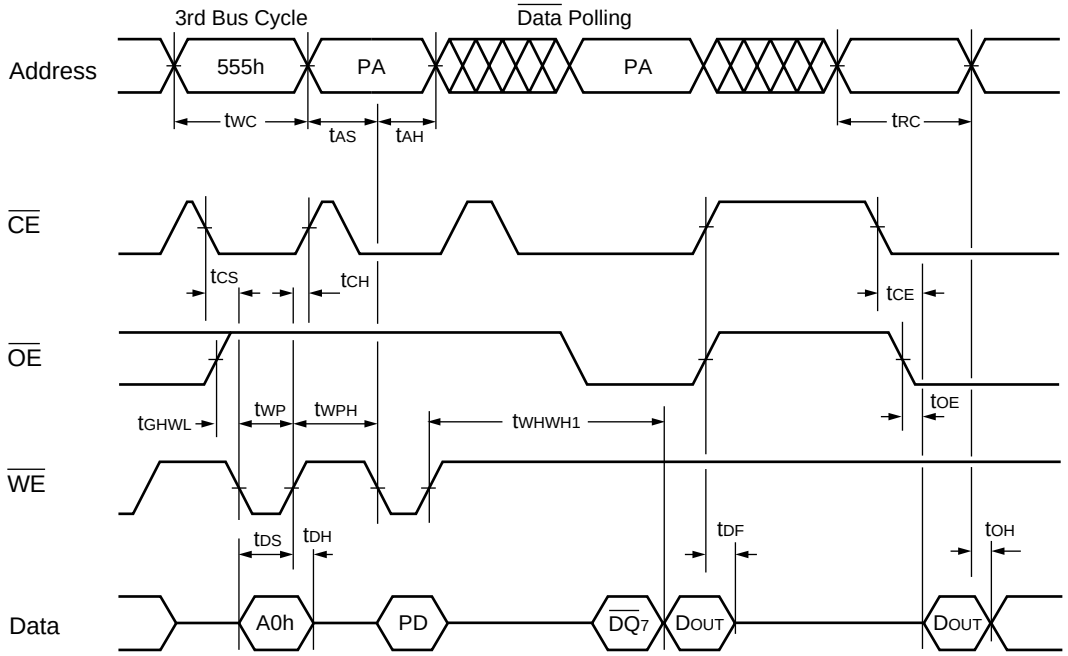
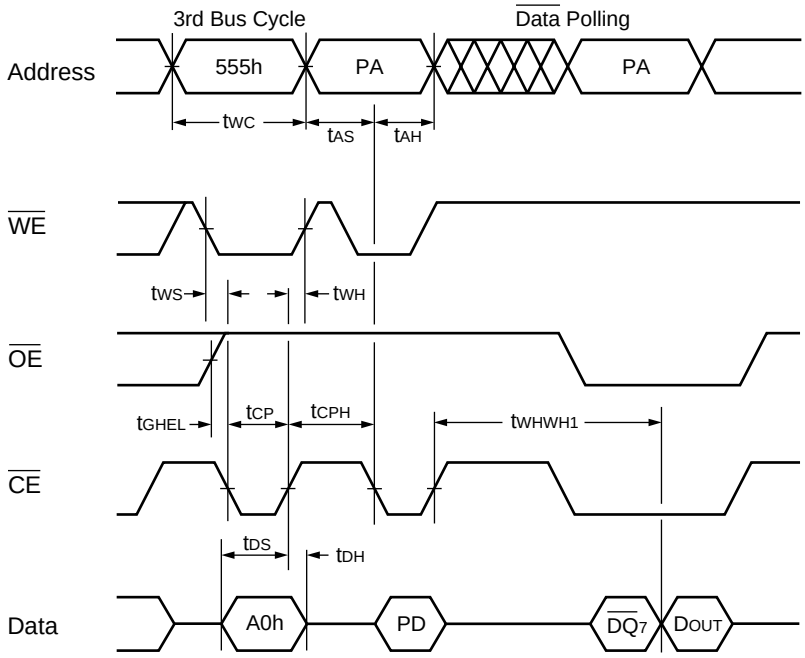


Figure 5.2 Page Read Operation Timing Diagram



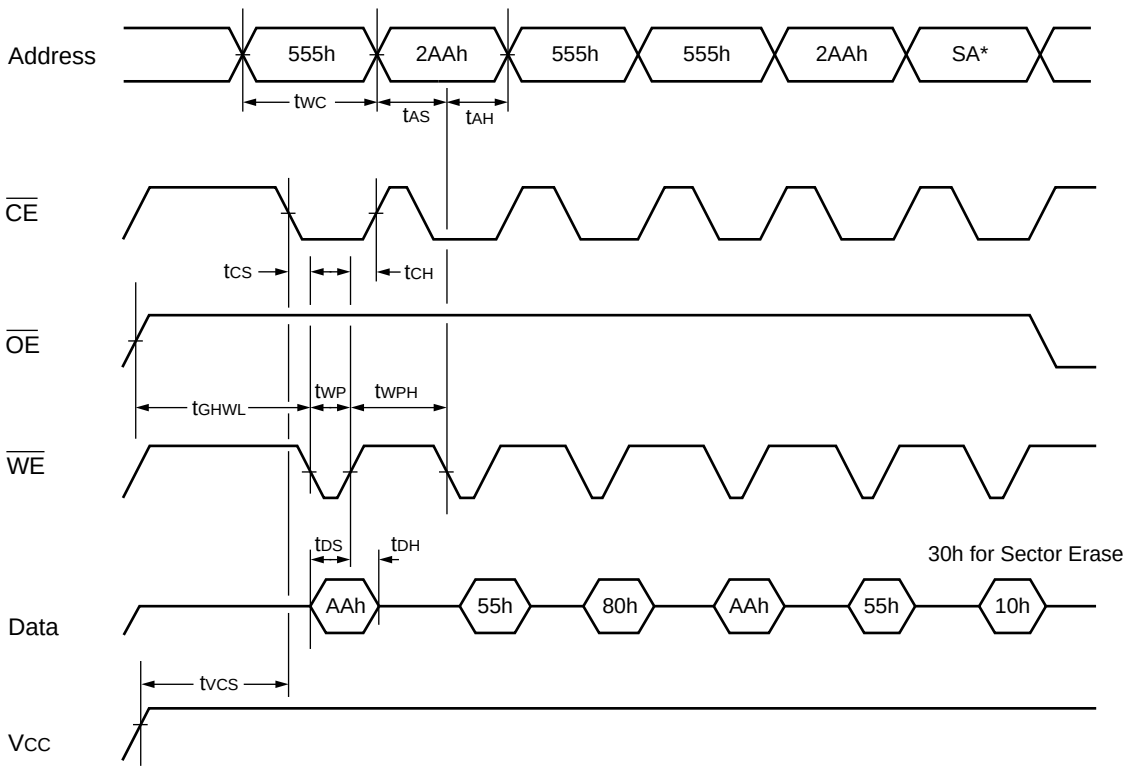
Notes : 1.PA is address of the memory location to be programmed.
2.PD is data to be programmed at word address.
3.$\overline{DQ}_7$ is the output of the complement of the data written to the device.
4.D_{OUT} is the output of the data written to the device.
5.Figure indicates last two bus cycles out of four bus cycle sequence.
6.These waveforms are for the × 32 mode. (The addresses differ from × 16 mode.)

Figure 6 Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram



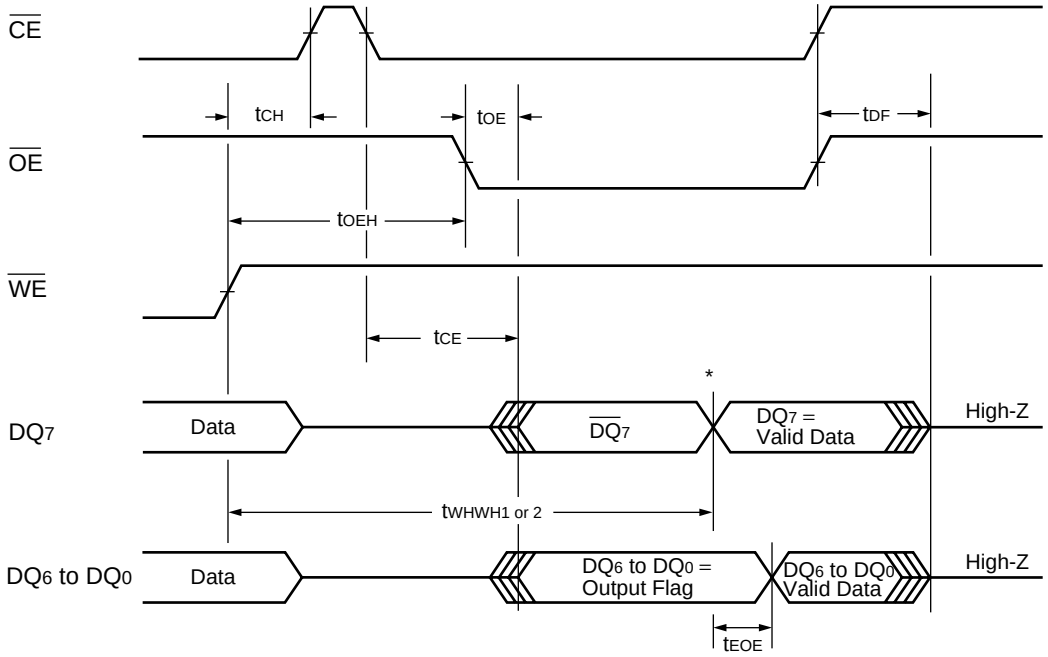
Notes : 1.PA is address of the memory location to be programmed.
2.PD is data to be programmed at word address.
3.$\overline{DQ}_7$ is the output of the complement of the data written to the device.
4.D_{OUT} is the output of the data written to the device.
5.Figure indicates last two bus cycles out of four bus cycle sequence.
6.These waveforms are for the × 32 mode. (The addresses differ from × 16 mode.)

Figure 7 Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram



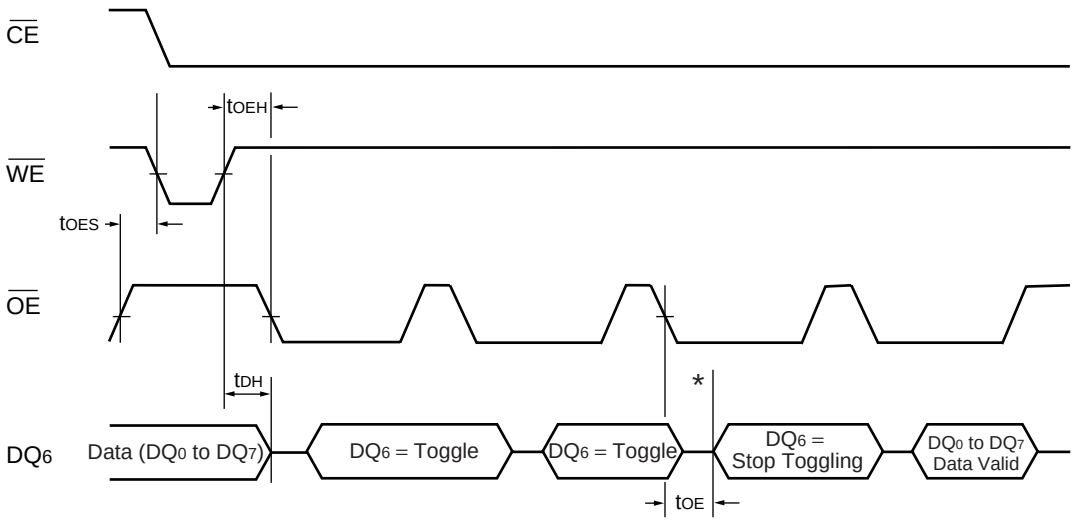
Note : 1.SA is the sector address for Sector Erase. Addresses = 555h (Double Word), AAAh (Word) for Chip Erase.
2.These waveforms are for the × 32 mode. (The addresses differ from × 16 mode.)

Figure 8 Chip/Sector Erase Operation Timing Diagram



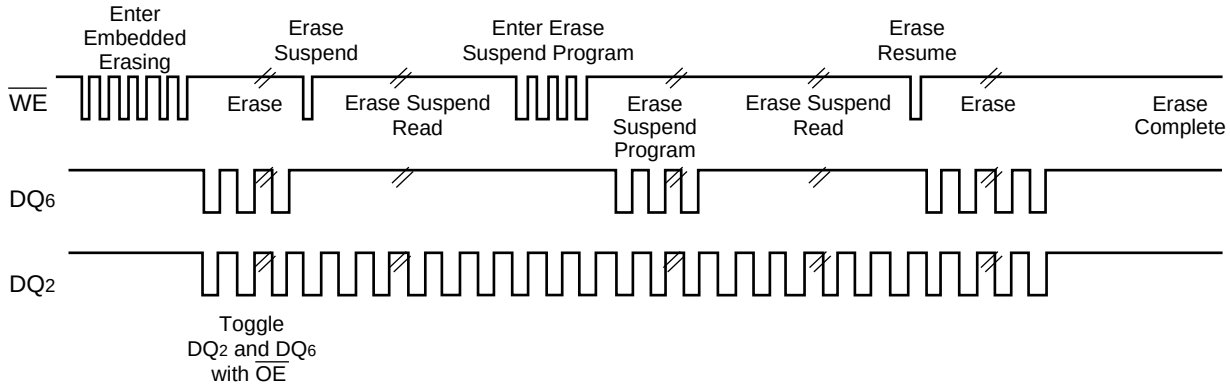
* : DQ_7 = Valid Data (The device has completed the Embedded operation)

Figure 9 $\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram



* : DQ_6 = Stops toggling. (The device has completed the Embedded operation.)

Figure 10 Toggle Bit I during Embedded Algorithm Operation Timing Diagram



Note : DQ_2 is read from the erase-suspended sector.

Figure 11 DQ_2 vs. DQ_6

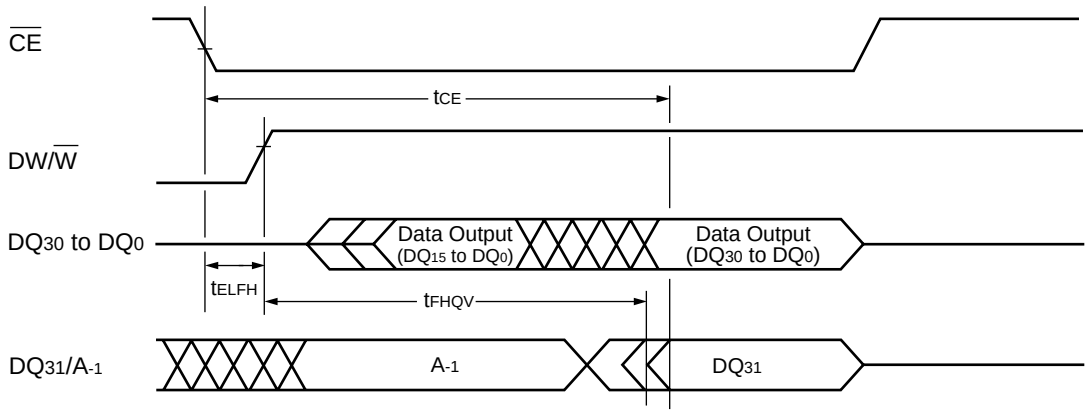


Figure 12 Double Word Mode Configuration Timing Diagram

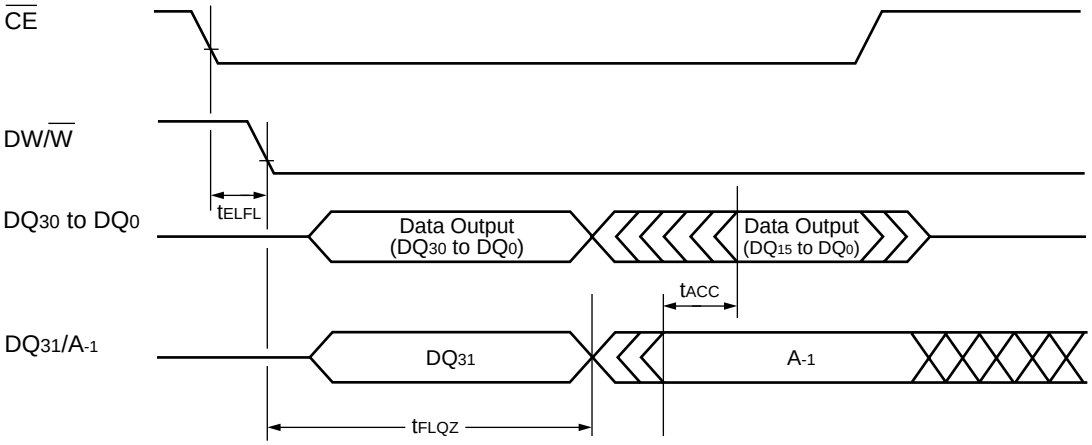


Figure 13 Word Mode Configuration Timing Diagram

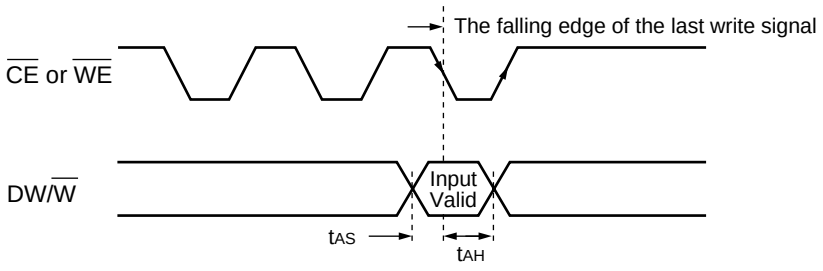
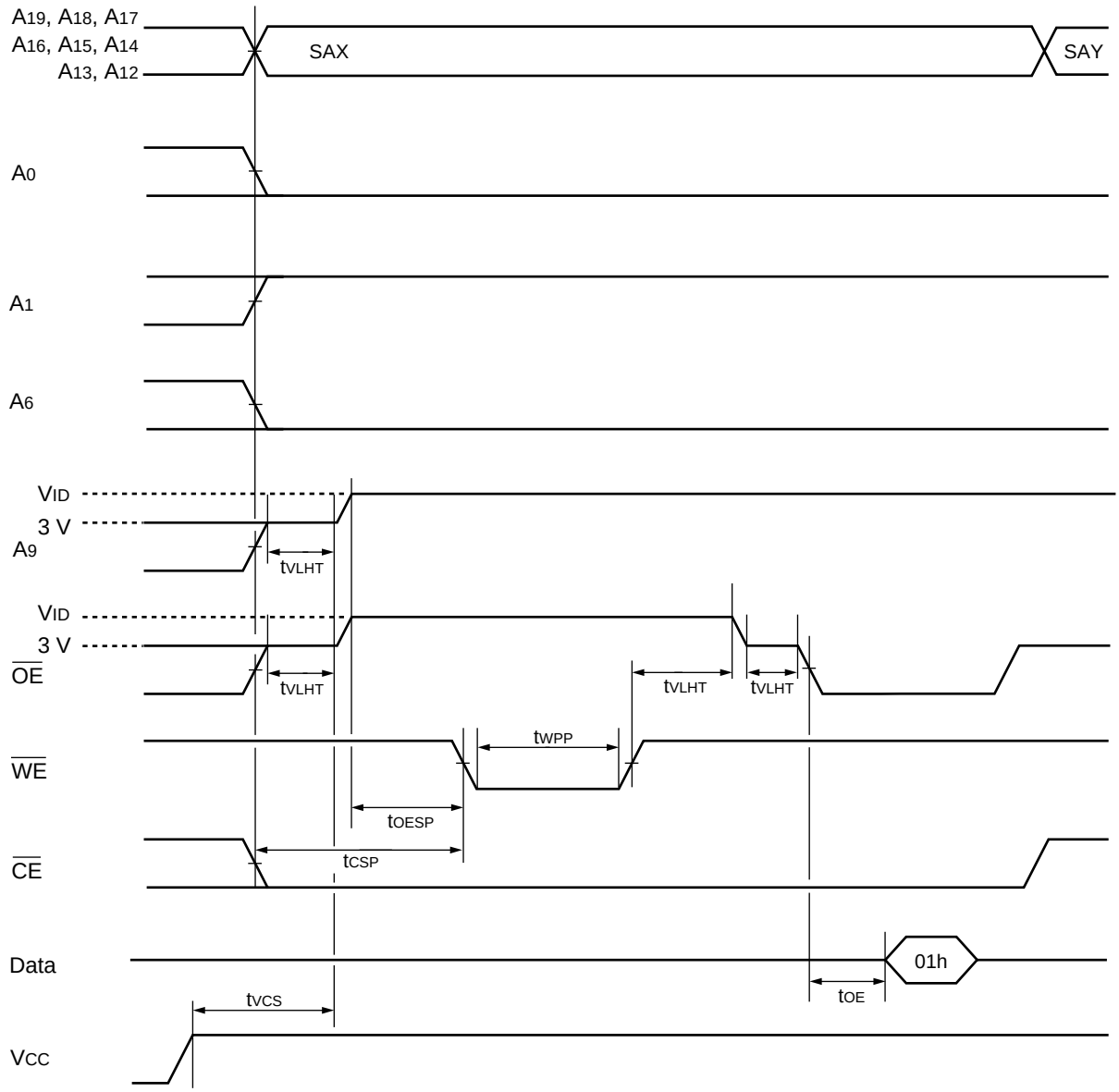


Figure 14 DW/W Timing Diagram for Write Operations



SAX : Sector Address for initial sector
SAY : Sector Address for next sector

Note : A_{-1} is V_{IL} on word mode.

Figure 15 Sector Protection Timing Diagram

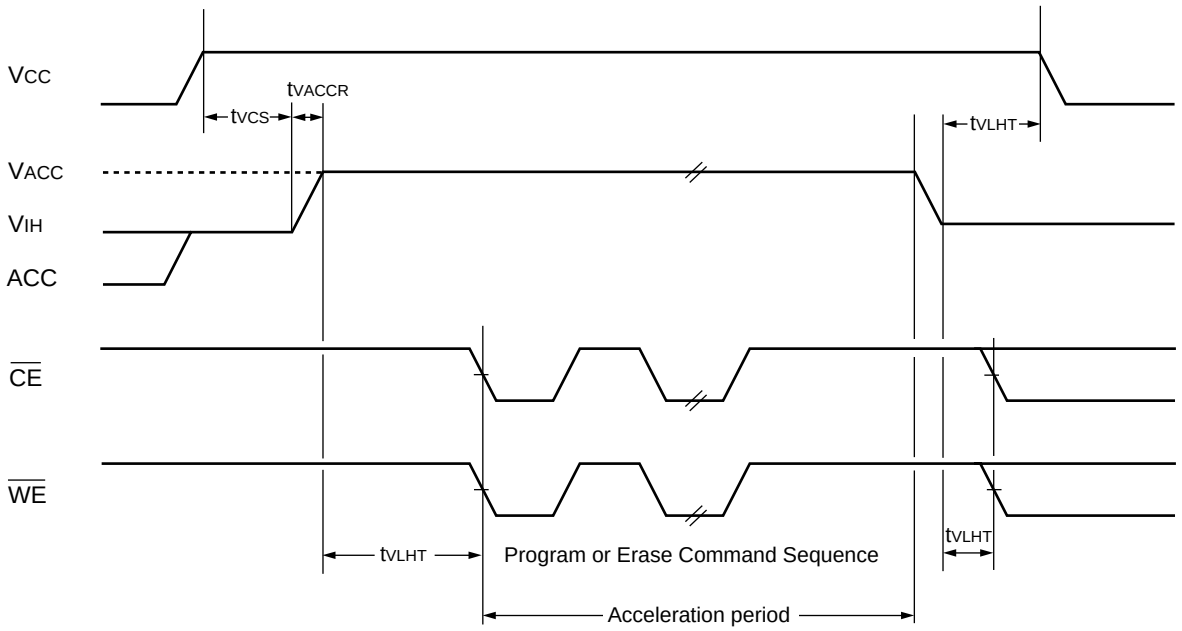
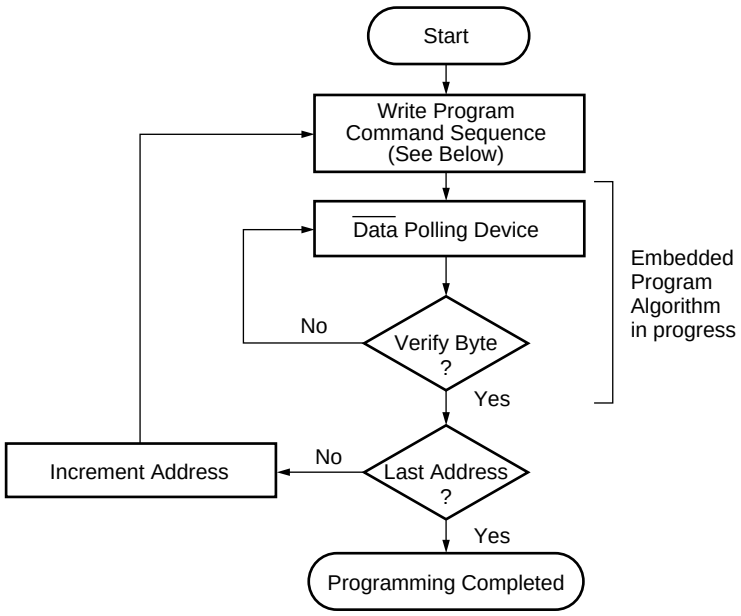
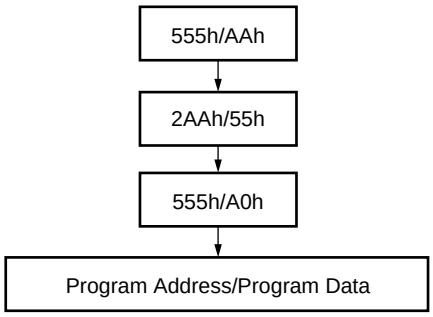


Figure 16 Accelerated Program Timing Diagram

EMBEDDED ALGORITHM



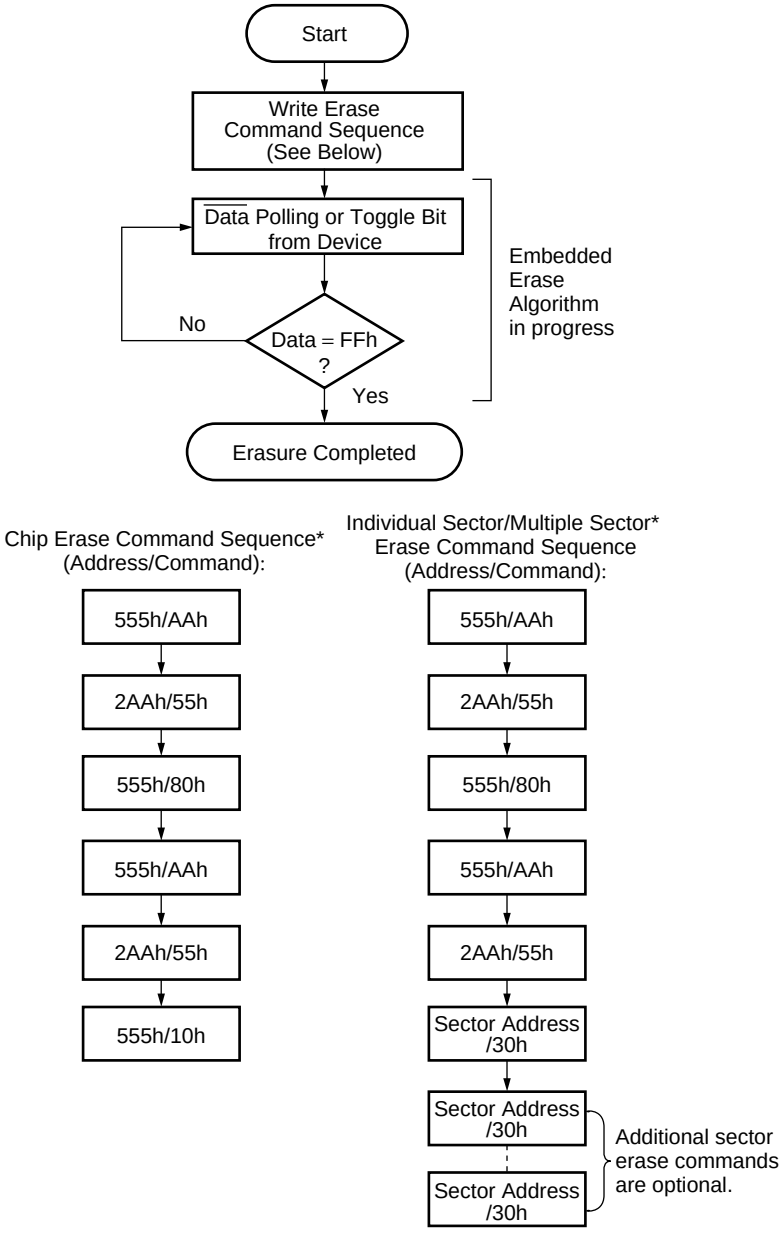
Program Command Sequence* (Address/Command):



* : The sequence is applied for × 32 mode.
The addresses differ from × 16 mode.

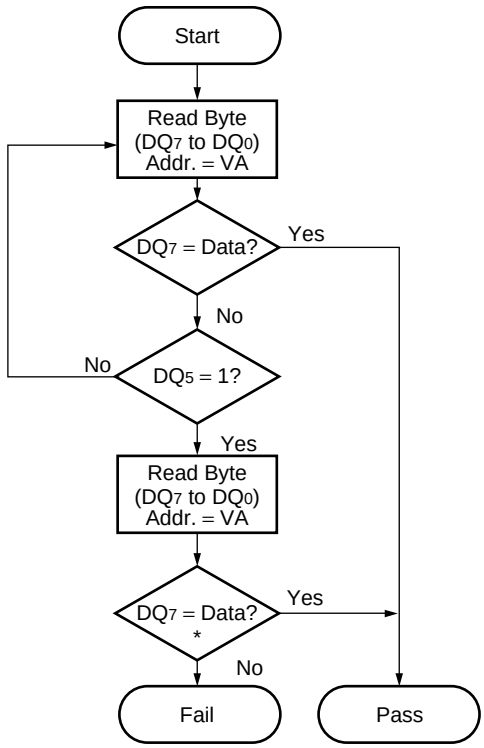
Figure 17 Embedded Program™ Algorithm

EMBEDDED ALGORITHM



* : The sequence is applied for × 32 mode.
The addresses differ from × 16 mode.

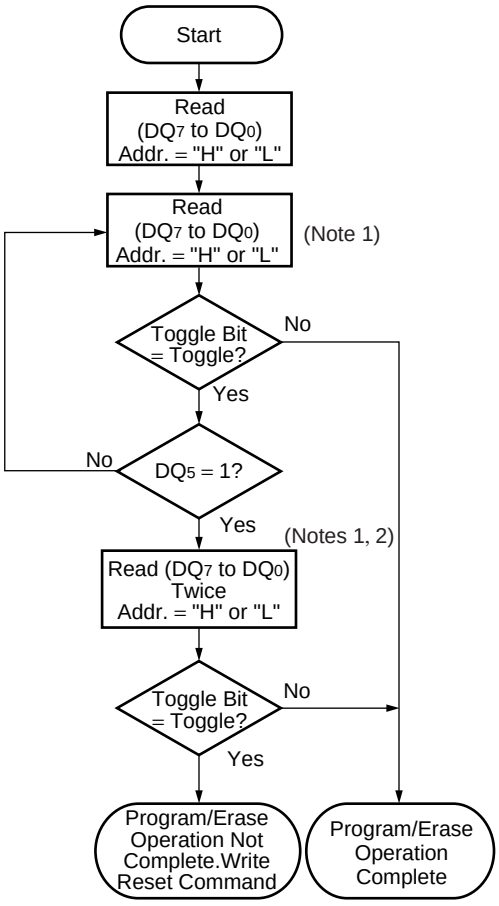
Figure 18 Embedded Erase™ Algorithm



VA = Address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.
= Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

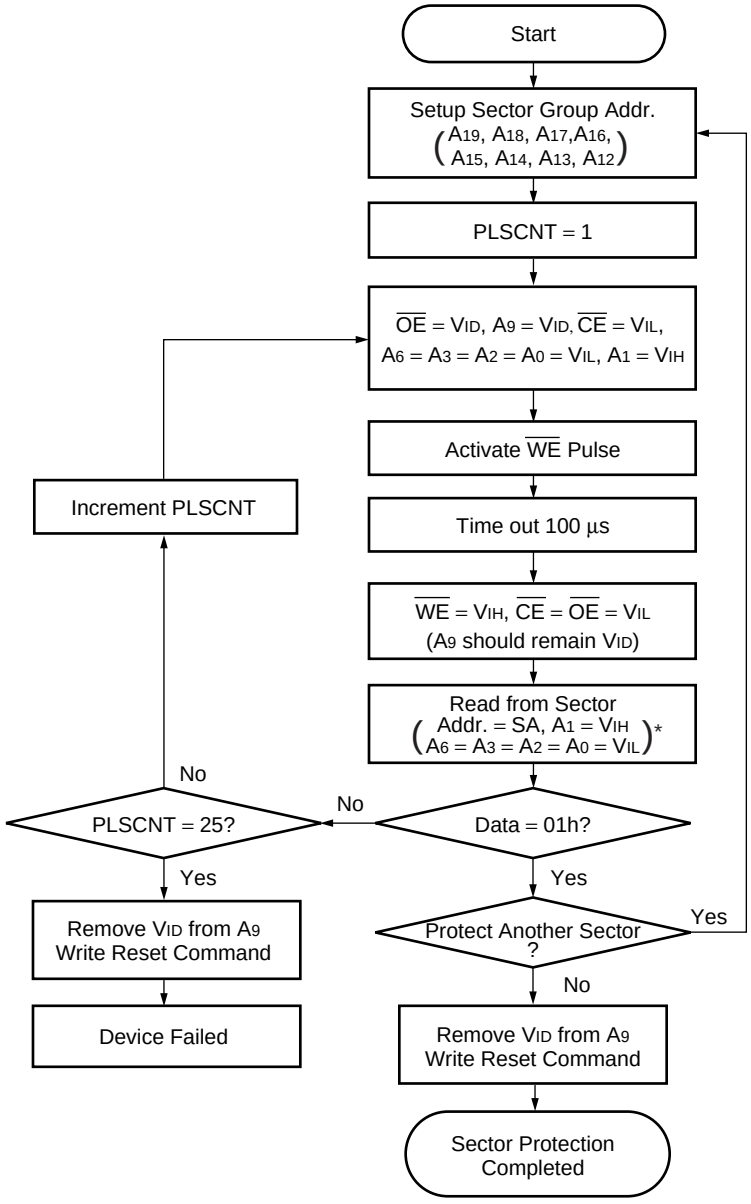
* : DQ_7 should be rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

Figure 19 $\overline{\text{Data}}$ Polling Algorithm



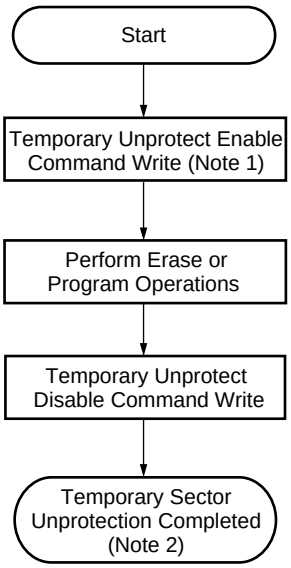
Notes : 1.Read toggle bit twice to determine whether or not it is toggling.
2.Recheck toggle bit because it may stop toggling as DQ_5 changes to “1”.

Figure 20 Toggle Bit Algorithm



* : A_{-1} is V_{IL} on word mode.

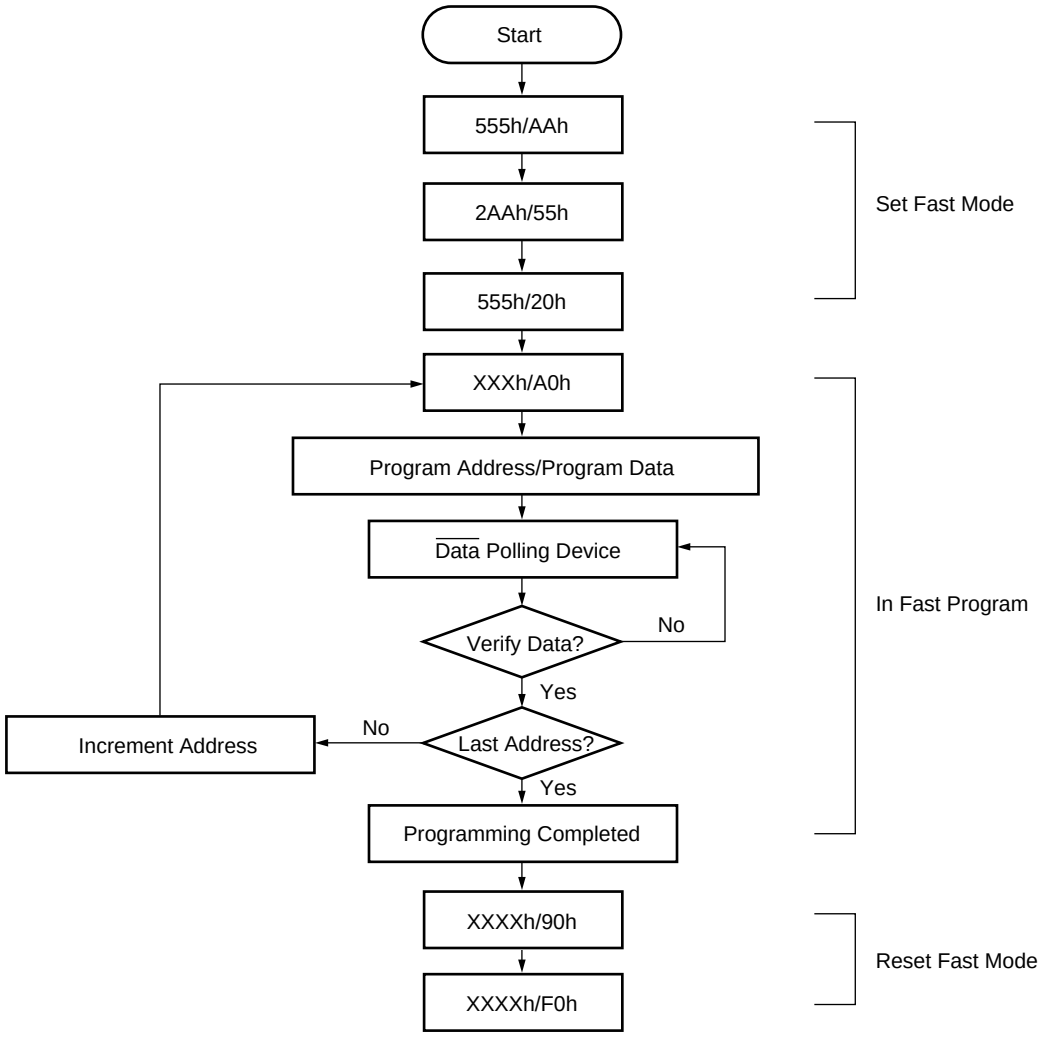
Figure 21 Sector Protection Algorithm



Notes : 1.All protected sectors are unprotected.
2.All previously protected sectors are protected once again.

Figure 22 Temporary Sector Unprotection Algorithm

FAST MODE ALGORITHM



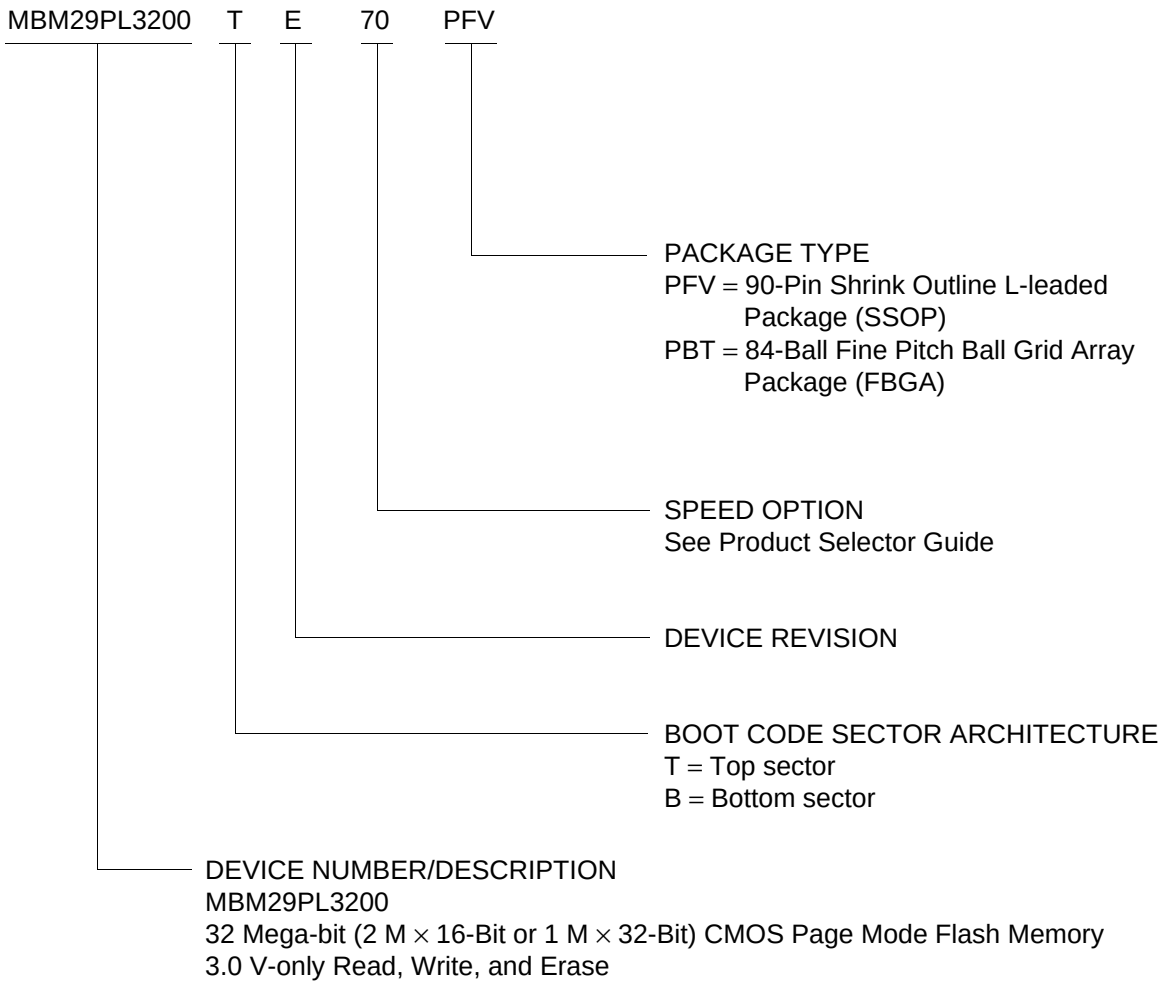
Notes 1 : The sequence is applied for × 32 mode.
2 : The addresses differ from × 16 mode.

Figure 23 Embedded Programming Algorithm for Fast Mode

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of:



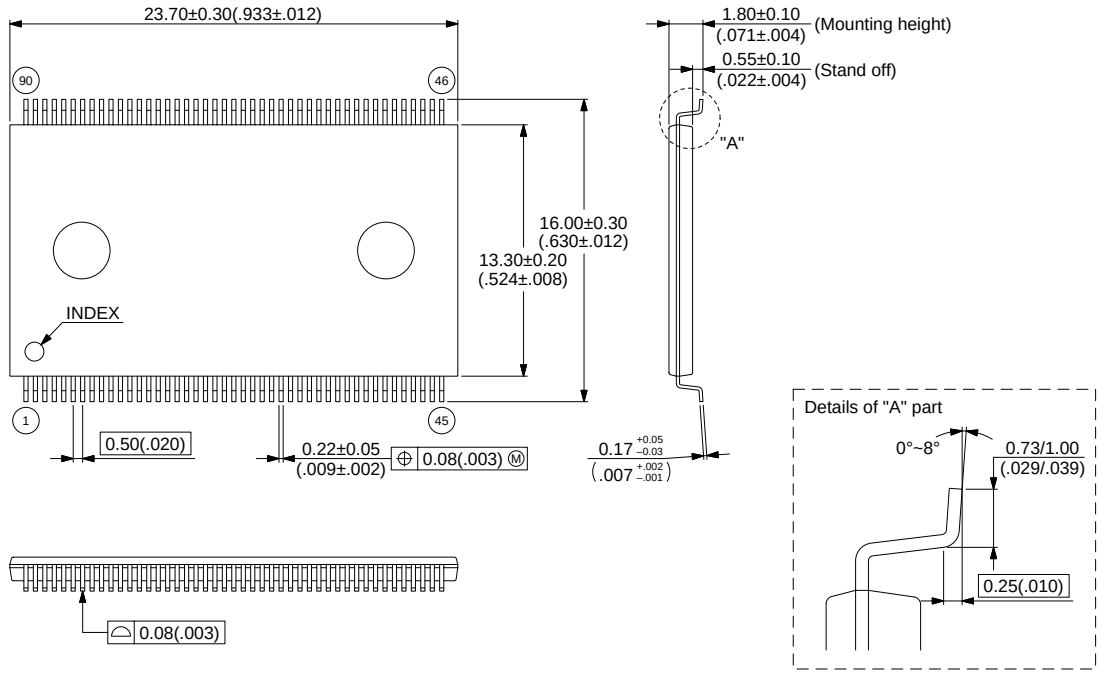
Valid Combinations		
MBM29PL3200TE/BE	70 90	PFV PBT

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

■ PACKAGE DIMENSIONS

90-pin plastic SSOP
(FPT-90P-M01)

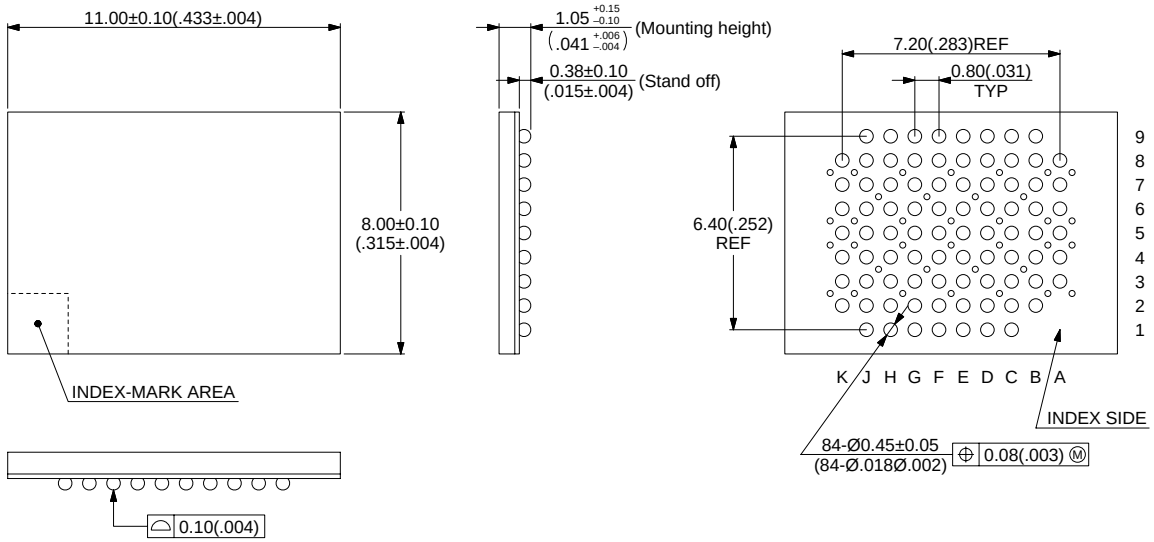


Dimensions in mm (inches)

(Continued)

(Continued)

84-ball plastic FBGA
(BGA-84P-M01)



Dimensions in mm (inches)

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