

### DESCRIPTION

M66010 Semiconductor Integrated Circuit inputs 24-bit data in series and outputs it in parallel and vice versa, using shift register function.

Equipped with 2 independent shift registers, one for serial-to-parallel, the other for parallel-to-serial, this IC is able to read serial input data into a shift register while converting data from parallel to serial. Parallel input/output pins are set to input or output according to the bit.

The M66010 is useful in a wide range of applications, such as MCU (micro controller unit) input/output port extension and serial bus system data communication.

### FEATURES

- Two-way serial data communication with MCU
- Serial data intake possible during parallel-to-serial conversion
- Parallel input/output switchable according to the bit
- Low power dissipation: 100 $\mu$ W maximum per package ( $V_{CC} = 5V$ ,  $T_a = 25^{\circ}C$ , quiescent)
- Schmidt input (DI, CLK,  $\bar{S}$ ,  $\bar{CS}$ )
- Open drain output (DO, D1 thru D24)
- Parallel data input and output (D1 thru D24)
- Wide operating supply voltage range ( $V_{CC} = 2V \sim 6V$ )

### APPLICATION

MCU-related serial-parallel data conversion, serial bus control by MCU, etc.

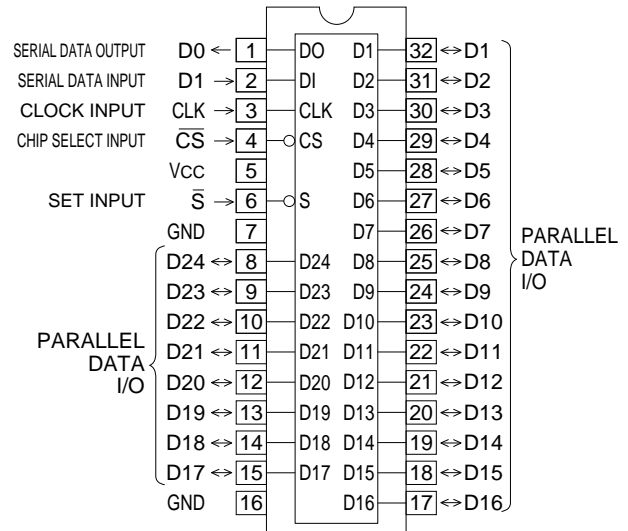
### FUNCTION

The M66010 is produced by using the silicon gate CMOS (complementary metal-oxide semiconductor) technology. It is distinguished for low power dissipation and high noise resistance.

Because two independent shift registers are built in, one for serial-to-parallel, the other for parallel-to-serial, this IC is able to read serial input data into a shift register while converting parallel data into serial data.

One cycle of latching 24-bit parallel data and outputting it in series while taking in serial data from MCU is initiated by  $\bar{CS}$ 's shift from "H" to "L". At  $\bar{CS}$  fall edges, 24-bit parallel data is latched, and output in series from pin DO synchronously with shift clock fall edges. At shift clock rise edges, serial data is taken in from MCU via pin DI. The data is read into shift register. The 25th and following shift clock pulses are ignored and read-in operation is masked. The pin DO status shifts to high-impedance. As  $\bar{CS}$  is then shifted from "L" to "H", 24-bit serial data taken in via pin DI is output in parallel to pins D1 thru D24. Because parallel output pins are the n-channel open drain output type, write data "H" for pins which should be set to input.

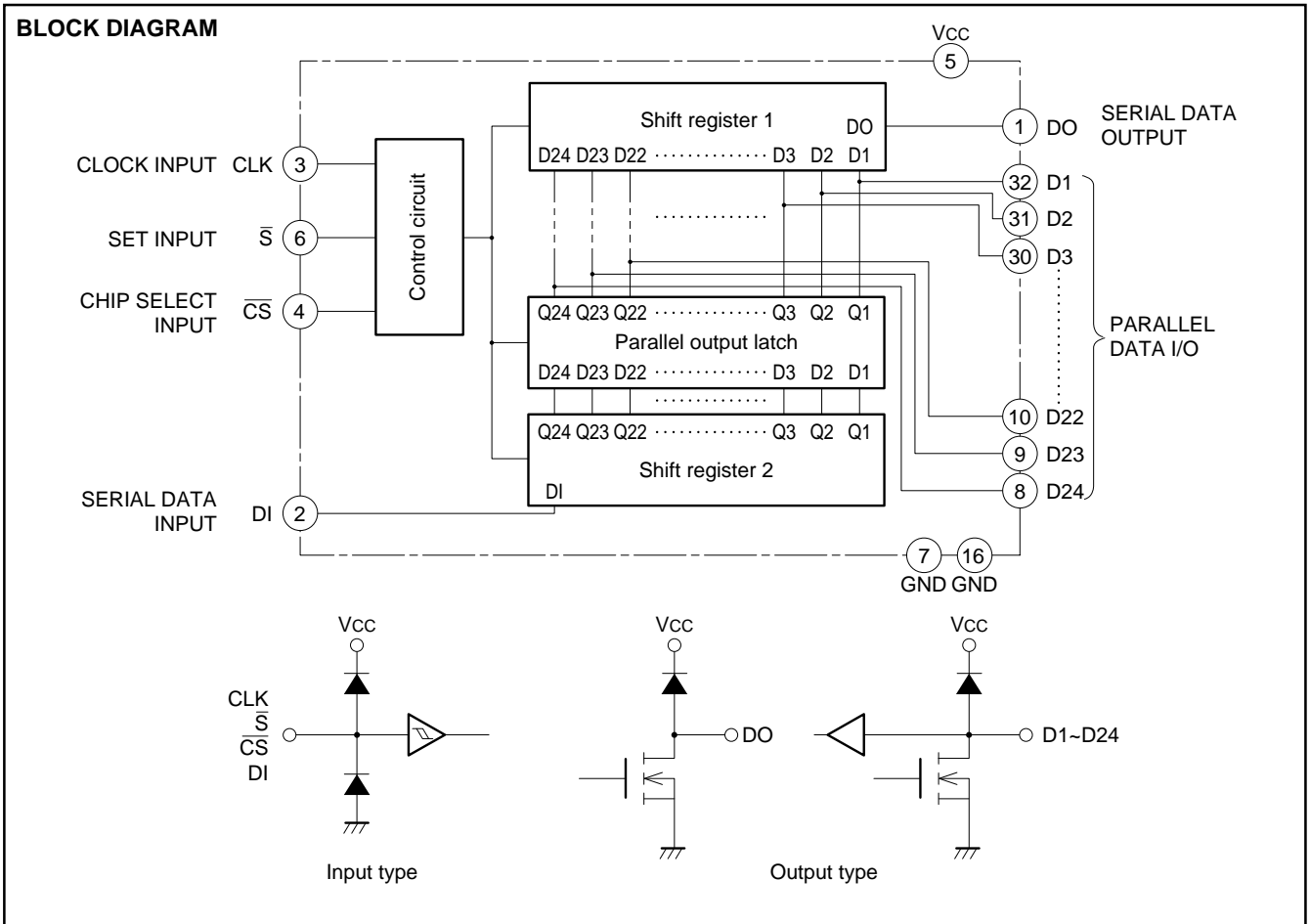
### PIN CONFIGURATION (TOP VIEW)



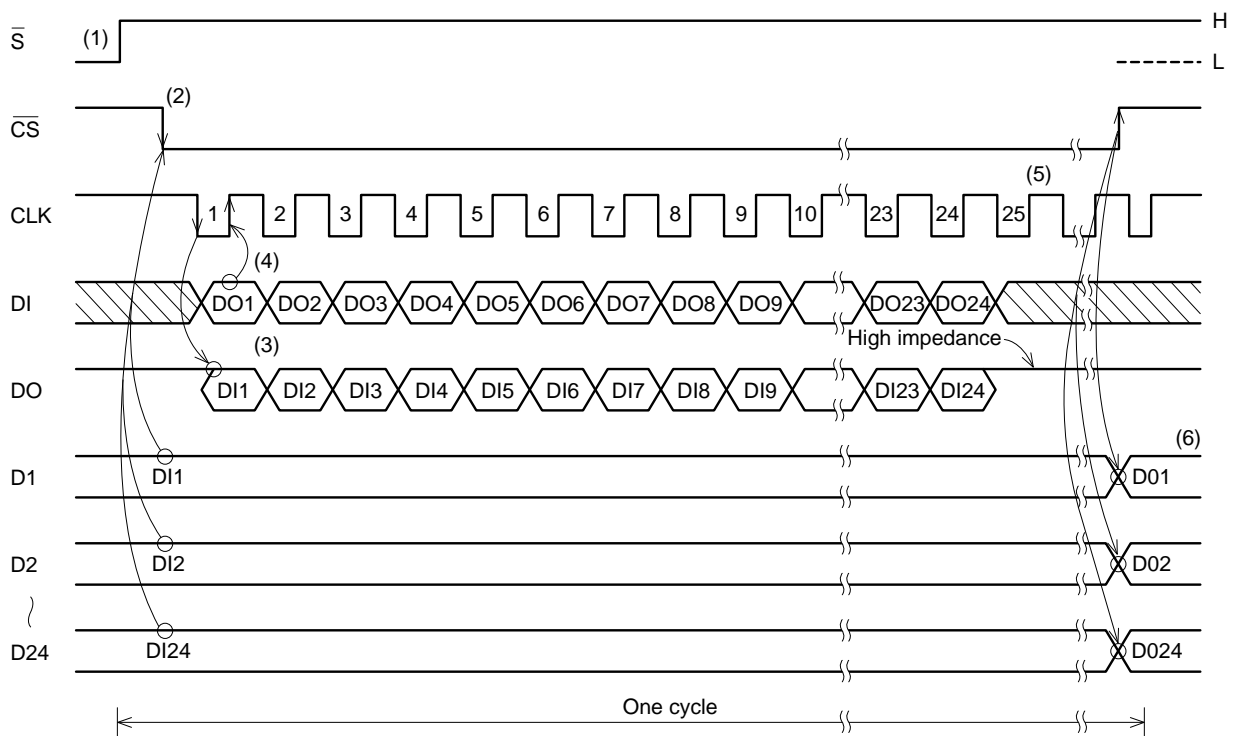
Outline 32P2W-A  
 32P2U-B

### OPERATION

- (1) When power is turned on, the status of pins D0 and D1 thru D24 is unstable. Their status turns high-impedance when  $\bar{S}$  is shifted to "L".
- (2) At  $\bar{CS}$  fall edges, the status of pins D1 thru D24 is loaded on shift register 1.
- (3) At CLK fall edges, 24-bit data loaded as described above is output in series from pin DO.
- (4) At CLK rise edges, 24-bit serial data is taken in from pin DI and written on shift register 2.
- (5) The 25th and following CLK pulses are ignored, and serial data write is discontinued. Pin DO status turns high-impedance.
- (6) At  $\bar{CS}$  rise edges, data written as described in (4) is output to pins D1 thru D24.
- (7) Shift register 1 loads data added from outside as well as AND tie data which has the same contents as data latched by serial output latch.
- (8) If the  $\bar{CS}$  rises before CLK reaches the 24th bit, parallel output latch latches data which has been written on shift register, and output it to pins D1 thru D24.
- (9) Pins D1 thru D24 are switched between input and output according to serial data input to pin DI. Pins for which "H" is written are set to input.



**OPERATION TIMING CHART**



**ABSOLUTE MAXIMUM RATINGS** (Ta = -20 ~ 75°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.5 ~ +7.0	V
Vi	Input voltage		-0.5 ~ Vcc + 0.5	V
Vo	Output voltage		-0.5 ~ Vcc + 0.5	V
Iik	Input protection diode current	Vi < 0V	-20	mA
		Vi > Vcc	20	
Iok	Output parasitic diode current	Vo < 0V	-20	mA
		Vo > Vcc	20	
IGND	GND current	GND	-150	mA
Tstg	Storage temperature		-65 ~ 150	°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc	Supply voltage	2		6	V
Vi	Input voltage	0		Vcc	V
Vo	Output voltage	0		Vcc	V
Topr	Operating temperature	-20		75	°C

**ELECTRICAL CHARACTERISTICS** (Vcc = 2 ~ 6V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits					Unit	
			Ta=25°C			Ta=-20~75°C			
			Min.	Typ.	Max.	Min.	Max.		
VT+	Upper threshold voltage	Vo=0.1V, Vcc=0.1V  Io =20μA	CLK, CS, S, DI	0.35 × Vcc		0.8 × Vcc	0.35 × Vcc	0.8 × Vcc	V
VT-	Lower threshold voltage	Vo=0.1V, Vcc=0.1V  Io =20μA		0.2 × Vcc		0.65 × Vcc	0.2 × Vcc	0.65 × Vcc	V
VIH	High-level input voltage	Vo=0.1V, Vcc=0.1V  Io =20μA	D1 ~ D24	0.75 × Vcc			0.75 × Vcc		V
VIL	Low-level input voltage	Vo=0.1V, Vcc=0.1V  Io =20μA				0.25 × Vcc		0.25 × Vcc	V
VOL	Open drain low-level output voltage	Vi=VT+, VT- Vcc=4.5V	IOL=5mA			0.4		0.5	V
Io	Output leakage current	Vi=VT+, VT- Vcc=6V	Vo=Vcc			1.0		10.0	μA
			Vo=GND			-1.0		-10.0	μA
IiH	High-level Input leakage current	Vi=Vcc	Vcc=6.0V			0.1		1.0	μA
IiL	Low-level output leakage current	Vi=GND	Vcc=6.0V			-0.1		-1.0	μA
Icc	Static power dissipation	Vi=Vcc, GND	Vcc=6.0V			20.0		200.0	μA

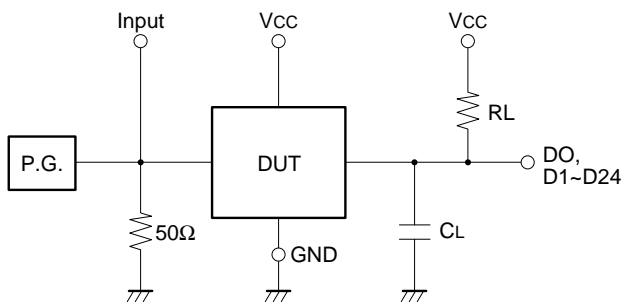
**SWITCHING CHARACTERISTICS** (Vcc = 5V)

Symbol	Parameter	Test conditions	Limits					Unit
			Ta=25°C			Ta=-20~75°C		
			Min.	Typ.	Max.	Min.	Max.	
fmax	Input clock maximum repetitive frequency	CL=50pF RL=1kΩ (Note)	2.5			1.9		MHz
tPLZ	"L-Z" and "Z-L" outputs propagation time				300		400	ns
tPZL	CLK-DO				300		400	ns
tPLZ	"L-Z" and "Z-L" outputs propagation time				300		400	ns
tPZL	CS-D1 to D24				300		400	ns
tPLZ	"L-Z" outputs propagation time S=DO, D1 to D24				300		400	ns

**TIMING CONDITIONS** ( $V_{CC} = 5V$ )

Symbol	Parameter	Test conditions	Limits					Unit
			Ta=25°C			Ta= -20~75°C		
			Min.	Typ.	Max.	Min.	Max.	
tw	CLK, $\overline{CS}$ and $\overline{S}$ pulse width		200			260		ns
tsu	DI setup time (in response to CLK)		100			130		ns
	$\overline{CS}$ setup time (in response to CLK)		100			130		
	DI thru D24 setup time (in response to $\overline{CS}$ )		100			130		
th	DI hold time (in response to CLK)		100			130		ns
	$\overline{CS}$ hold time (in response to CLK)		100			130		
	D1 thru D24 hold time (in response to $\overline{CS}$ )		100			130		
trec	$\overline{CS}$ recovery time (in response to $\overline{S}$ )		100			130		ns

**NOTE: TEST CIRCUIT**



- (1) Pulse generator (PG) characteristics:  $t_r=t_f=6ns$  (10% ~ 90%)
- (2) Capacitance CL includes connection floating capacitance and probe input capacitance.

TIMING CHARTS

