

CMOS 8-bit Single Chip Microcomputer

Piggyback/
evaluator type

Description

The CXP83200A is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP83120A/83124A and CXP83232/83240.

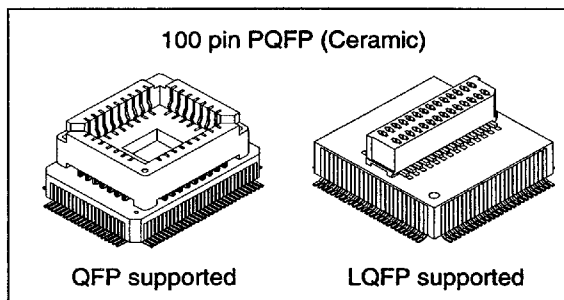
Features

- Wide-range instruction system (213 instructions) to cover various types of data
 - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation
 8 μ s at 500kHz operation
 122 μ s at 32kHz operation
- Applicable EPROM LCC type 27C512
 (Maximum 40K bytes are available.)
- Incorporated RAM capacity 1120 bytes (Including LCD display data area)
- Peripheral functions
 - A/D converter 8-bit, 8-channel, successive approximation method
 (Conversion time of 32 μ s/10 MHz)
 - Serial interface Incorporated 8-bit, 8-stage FIFO
 (Auto transfer for 1 to 8 bytes), 1 channel
 8-bit clock sync type, 1 channel
 - Timer 8-bit timer
 8-bit timer/counter
 19-bit time base timer
 16-bit capture timer/counter
 32kHz timer/counter
 - LCD controller/driver Maximum 160 segment display possible (for 1/4 duty)
 4 lines for common output, 40 lines for segment output
 Display method static: 1/2, 1/3, 1/4 duty
 Bias method: 1/2, 1/3 bias
 - Remote control reception circuit 8-bit pulse measurement counter with on-chip 6-stage FIFO
 - PWM output 14 bits, 1 channel
- Interruption 15 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin ceramic PQFP

Note) Mask option depends on the type of the CXP83200A. Refer to the Products List for details.

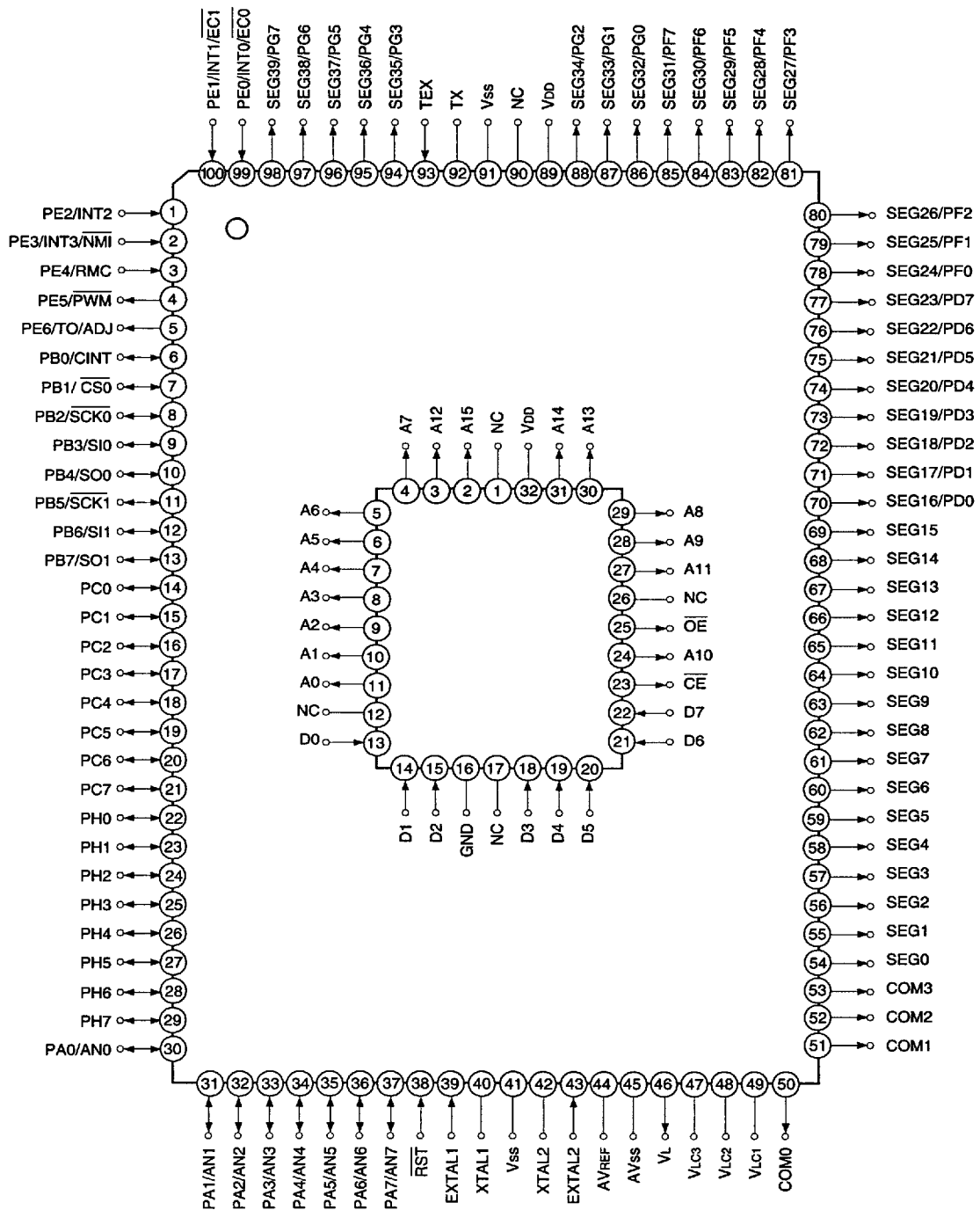
Structure

Silicon gate CMOS IC



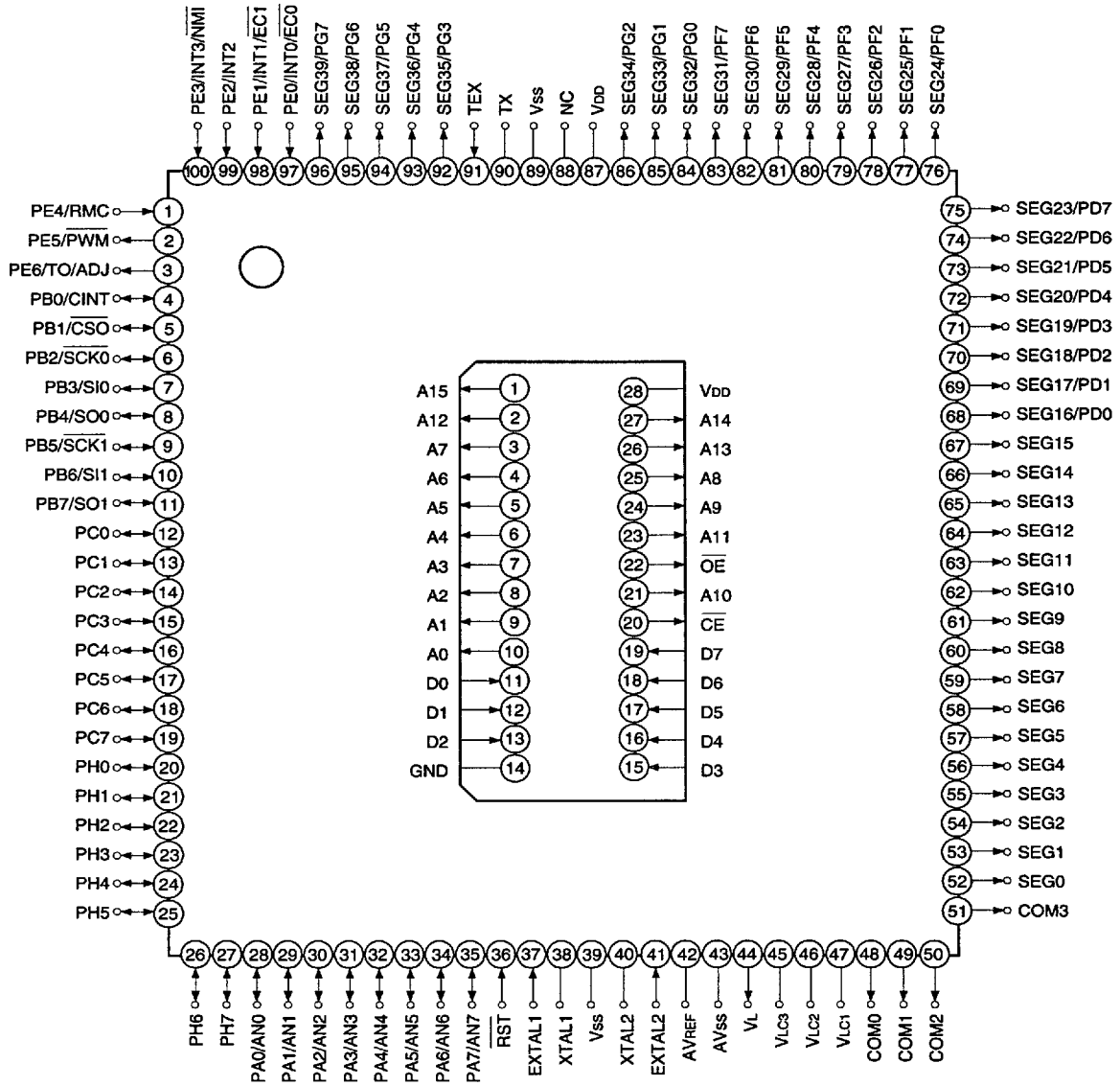
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Pin Configuration in Piggyback Mode (QFP package)



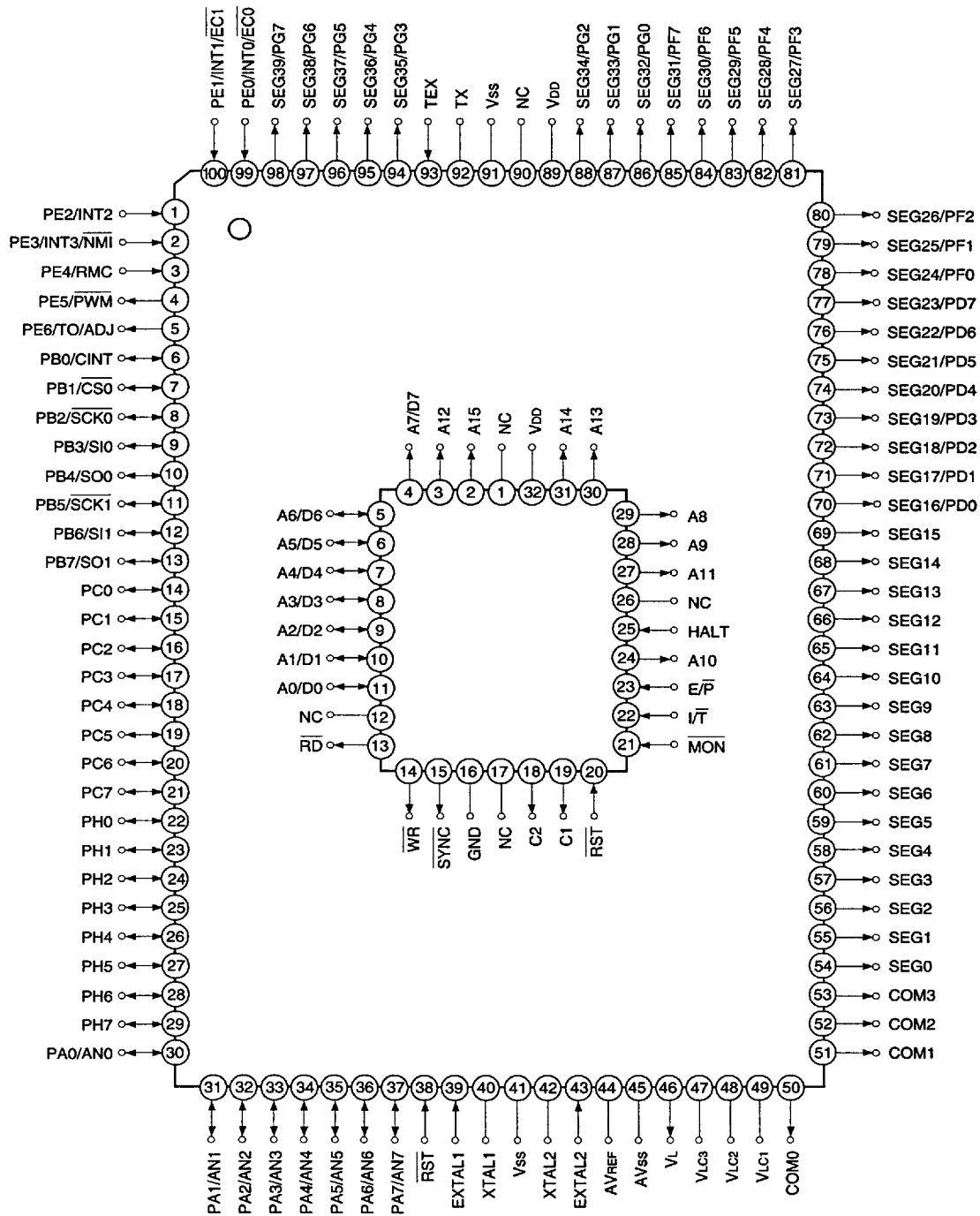
- Note)** 1. NC (Pin 90) is always connected to VDD.
 2. Vss (Pins 41 and 91) are both connected to GND.

Pin Configuration in Piggyback Mode (LQFP package)



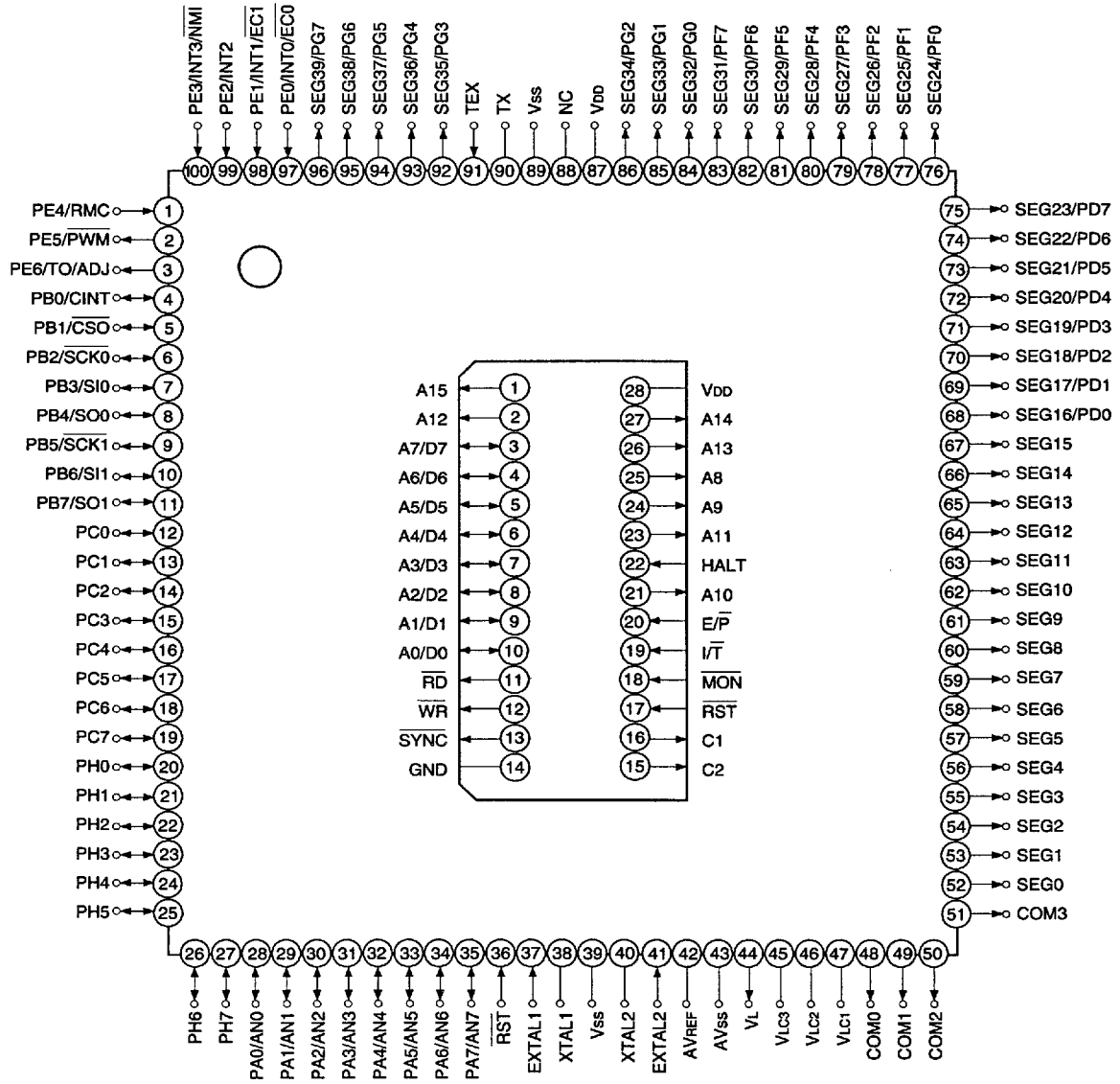
- Note)** 1. NC (Pin 88) is always connected to VDD.
 2. Vss (Pins 39 and 89) are both connected to GND.

Pin Configuration in Evaluator Mode (QFP package)



- Note)** 1. NC (Pin 90) is always connected to V_{DD}.
 2. V_{SS} (Pins 41 and 91) are both connected to GND.

Pin Configuration in Evaluator Mode (LQFP package)

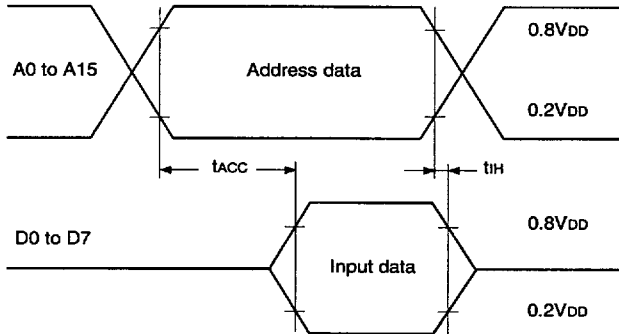


- Note)** 1. NC (Pin 88) is always connected to V_{DD}.
 2. V_{SS} (Pins 39 and 89) are both connected to GND.

EPROM Read Timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

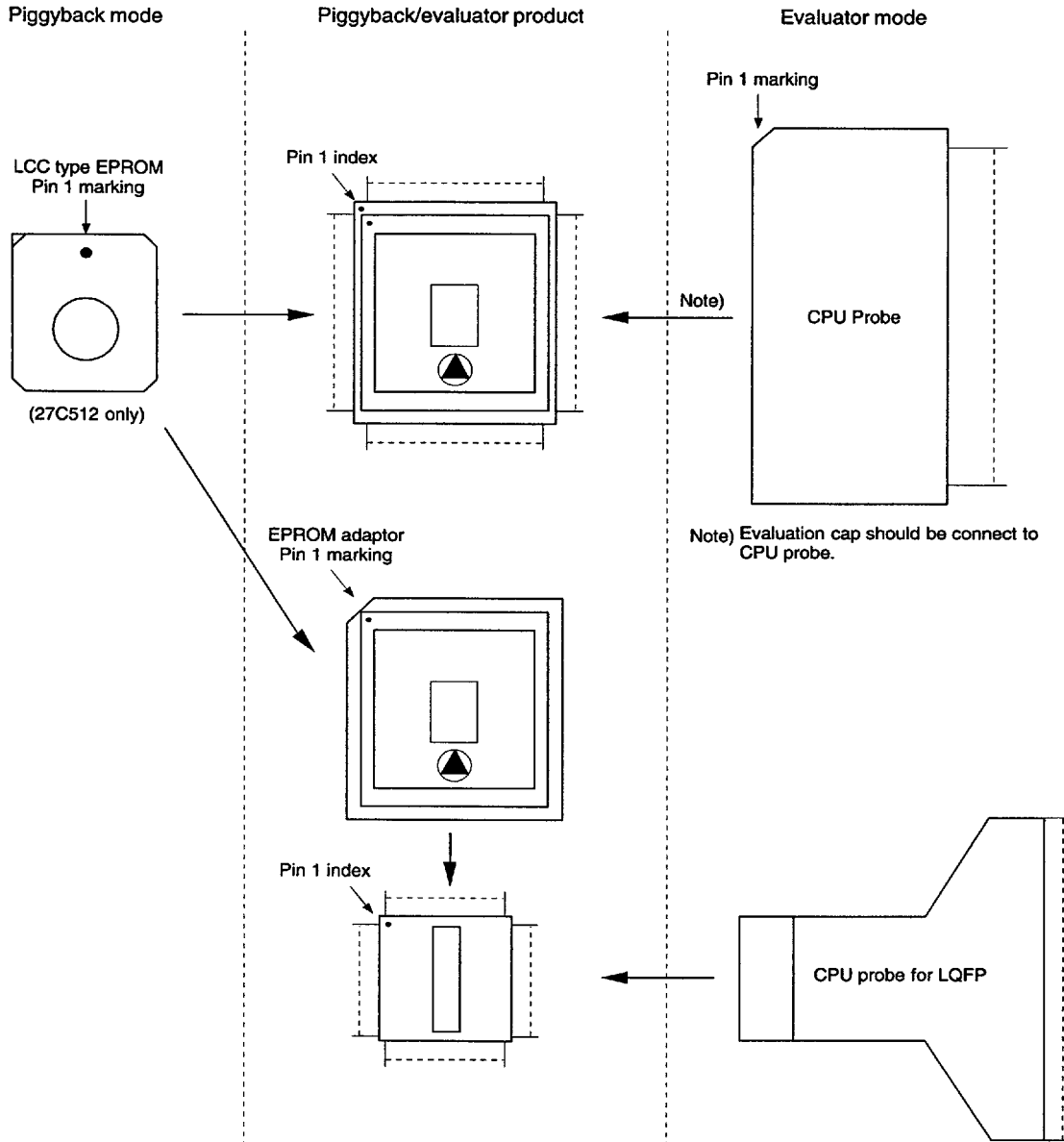
| Item | Symbol | Pins | Min. | Max. | Unit |
|---------------------------------|-----------|-----------------------|------|------|------|
| Address → Data input delay time | t_{acc} | A0 to A15 D0 to D7 | | 120 | ns |
| Address → Data Hold time | t_{IH} | A0 to A15 D0 to D7 | 0 | | ns |



Products List

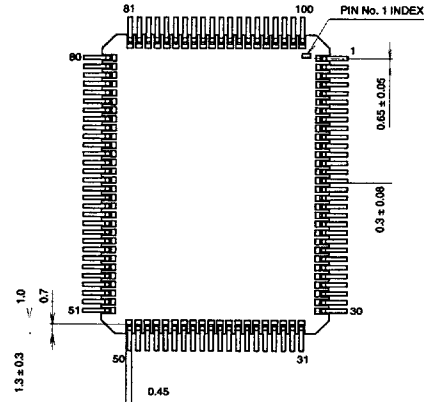
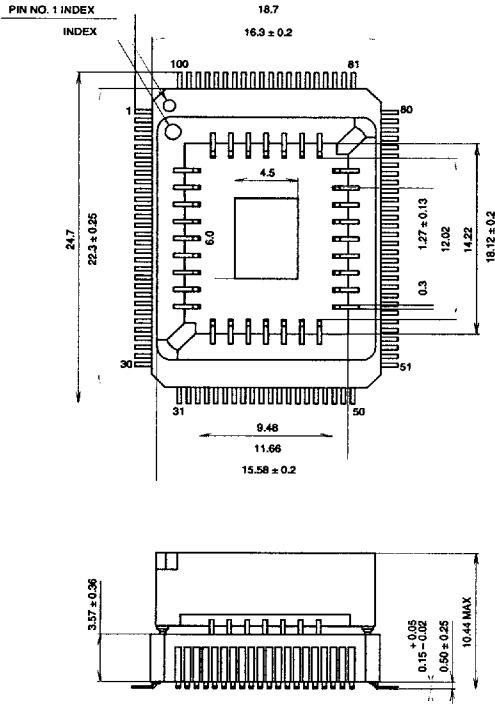
| Option item | Products | | | | |
|------------------------------|--------------------------|-----------|-----------|-----------|----------------------------------|
| | Mask type | | | | Piggyback/evaluator type |
| | CXP83120A | CXP83124A | CXP83232A | CXP83240A | CXP83200A-U01Q CXP83200A-U01R |
| Package | 100-pin plastic QFP/LQFP | | | | 100-pin ceramic PQFP |
| Rom capacitance | 20K bytes | 24K bytes | 32K bytes | 40K bytes | EPROM 40K bytes |
| RAM capacitance | 644 bytes | | 1120bytes | | 1120 bytes |
| Pull-up resistance for reset | Existent/Non-existent | | | | Existent |

Piggyback mode/evaluator mode can be switched as shown below.



Package Outline Unit: mm

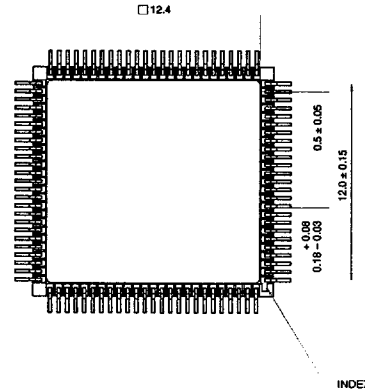
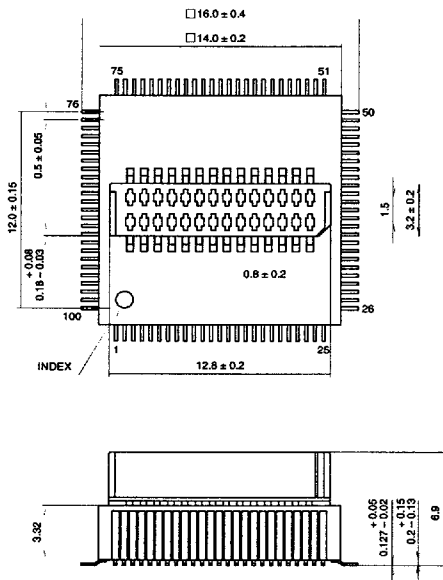
100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

| | | | |
|------------|------------------|------------------|--------------|
| SONY CODE | PQFP-100C-L01 | PACKAGE MATERIAL | CERAMIC |
| EIAJ CODE | AQFP100-C-0000-A | LEAD TREATMENT | GOLD PLATING |
| JEDEC CODE | | LEAD MATERIAL | 42 ALLOY |
| | | PACKAGE WEIGHT | 6.7g |

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

| | | | |
|------------|------------------|------------------|--------------|
| SONY CODE | PQFP-100C-L02 | PACKAGE MATERIAL | CERAMIC |
| EIAJ CODE | AQFP100-C-1414-A | LEAD TREATMENT | GOLD PLATING |
| JEDEC CODE | | LEAD MATERIAL | 42 ALLOY |
| | | PACKAGE WEIGHT | 2.2g |