10BIT 30MSPS Single-Channel DAC DAC1243X_SR

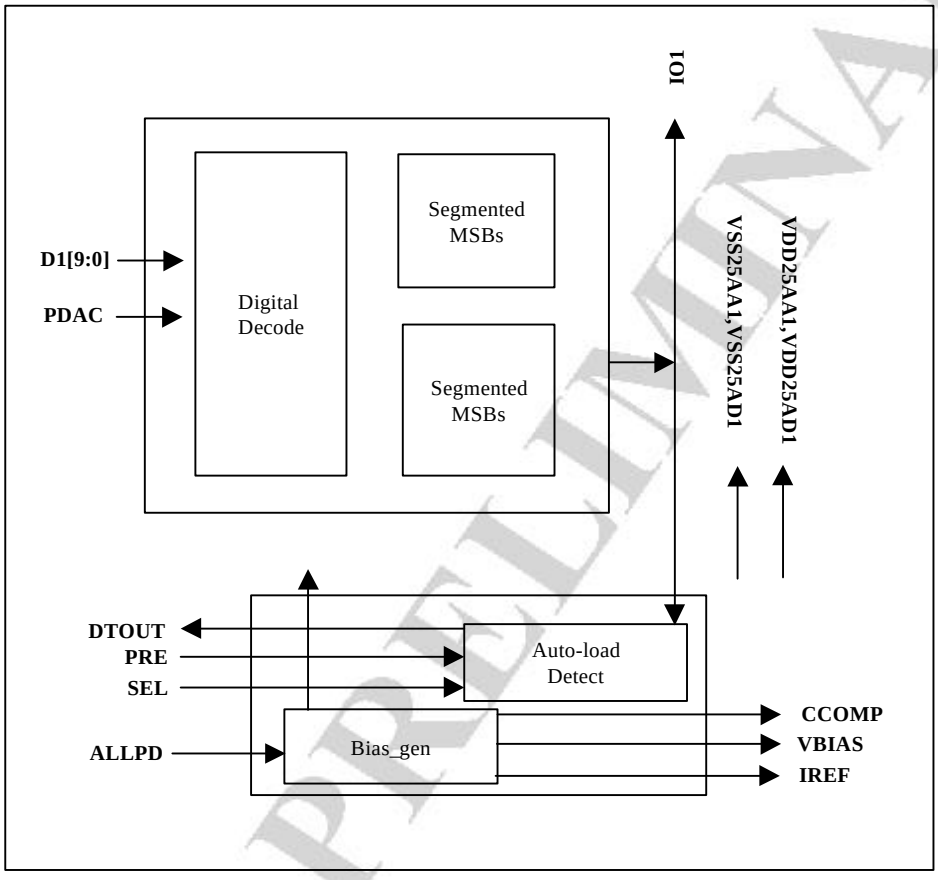
GENERAL DESCRIPTION

This core is a CMOS single-channel 10bit 30MSPS D/A converter for general & video applications. The dac1243x_sr core is implemented in the Samsung 0.25um 2.5V CMOS process. Digital inputs are coded as straight binary. This DAC includes independent power down control and the ability to sense output load. An external(optional) or internal 0.7V reference voltage(VBIAS) and a single external resister control the full-scale output current together. It uses the two architecture of current-segment and binerary-weighted.

FEATURES

- **Maximum conversion rate is 40MSPS**
- **+2.5V CMOS monolithic construction**
- **±0.75LSB differential linearity (typical)**
- **±1.0LSB integral linearity (typical)**
- **External or internal voltage reference (Including Band Gap Reference Block)**
- **single Channel DAC**
- **10-Bit parallel Straight Binary Digital input**
- **DAC auto-load detection circuitry**
- **Temperature : 0 ~ 70°C**
- **Just analog switch Power_Down enable**

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION

- High Definition Television(HDTV)
- High Resolution Color Graphics
- Hard Disk Driver(HDD)
- CAE/CAD/CAM
- Image Processing
- Instrumentation

Ver 1.0 (Jan. 2000)

PIN CONFIGURATION

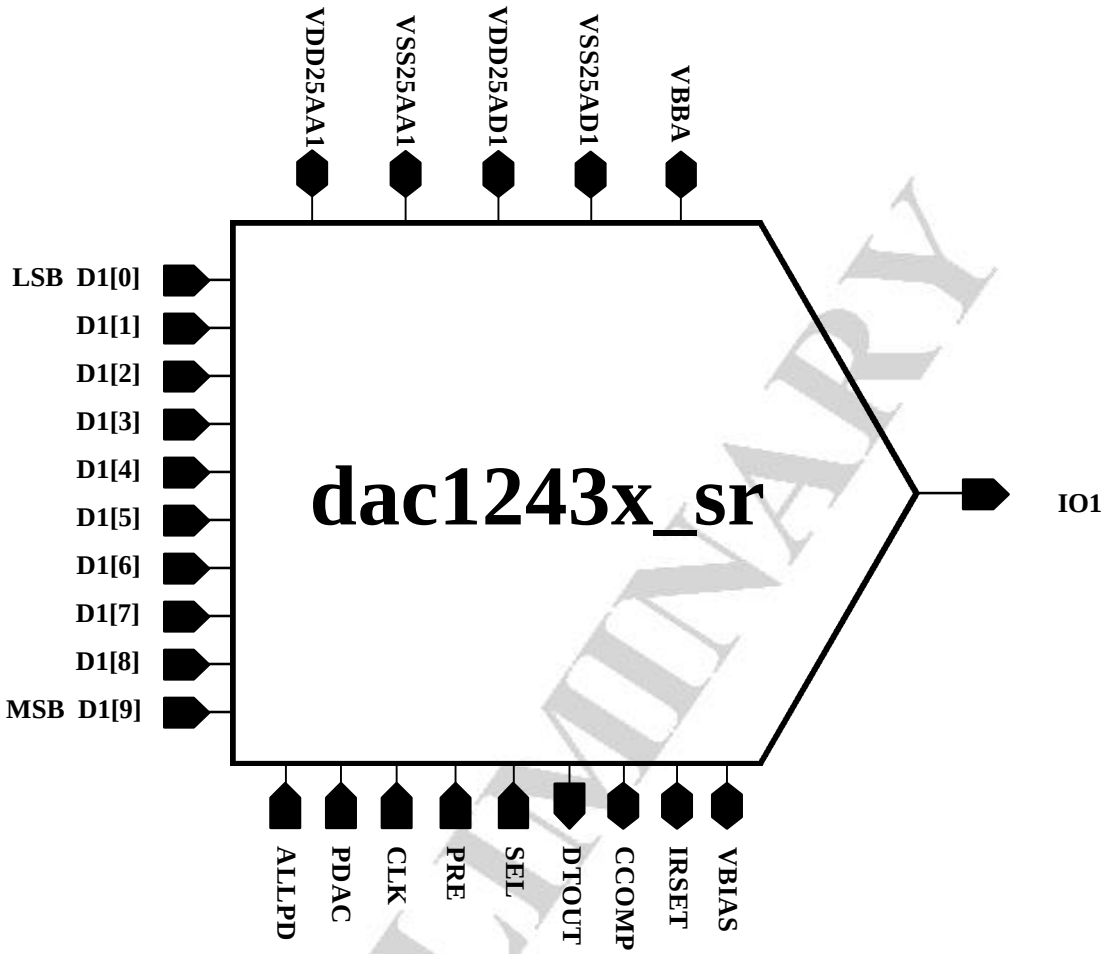
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
PDAC	DI	piar50_abb	Just Analog Switch Block power down control. When activated(high) all current switches are disabled.
CLK	DI	picc_abb	DAC master clock. Input data is latched into the DACs on the rising edge of **CLK**.
PRE	DI	piar50_abb	Control strobe for the DAC auto-load detection comparator. When **PRE** transitions high-to-low, the auto-load detect circuit evaluates its analog input. Appropriate settling time must be allowed before the comparator output **(DTOUT)** is used. When not used, **PRE** should be left high.
D1[9:0]	DI	picc_abb	10-bit straight binary, parallel digital input
ALLPD	DI	piar50_abb	Power down control for Bandgap and all blocks. A high level disables all analog switchs and digital blocks plus the bandgap reference regardless of the states of **PDAC**
DTOUT	DO	pot8_abb	Comparator output for detection of resistive load at DAC output. A low at the detect output indicates that the output voltage of the current selected DAC is above 0.53V and therefore that no load is attached.
CCOMP	AB	poa_abb_50option	Internal DAC compensation node. Connect external 0.1uF cap to **VDD25AA1**.
IRSET	AB	poa_abb_50option	External resistor from this node to **VSS25AA1** defines the full scale output current for the DACs.
VBIAS	AB	poa_abb_50option	External reference voltage output.
VDD25AA1	AP	vdd2t_abb	Analog Power (2 pads for this node is recommended.)
VSS25AA1	AG	vss2t_abb	Analog Ground (2 pads for this node is recommended)
VDD25AD1	DP	vdd2t_abb	Digital Power
VSS25AD1	DG	vss2t_abb	Digital Ground
VABB	AG	vbb_abb	Substrate Bias(the same with ground level)
IO1	AO	poa_abb_50option	Analog Current Output

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- AG : Analog Ground
- DP : Digital Power
- DG : Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Supply Voltage	VDD25AA1 - VSS25AA1 VDD25AD1 - VSS25AD1	2.5	V
Voltage on Any Digital Pin	CLK	VSS25AD1-0.25 to VDD25AD1+0.25	V
Storage Temperature Range	T_{stg}	-45 ~ 125	°C

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to GND unless otherwise specified
3. Applied voltage must be limited to specified range.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Operating Supply Voltage	VDD25AD1,VDD25AA1	2.25	2.5	2.75	V
Digital Input Voltage High	V_{IH}	1.75	2.5	-	V
Digital Input Voltage Low	V_{IL}	-	0.0	0.75	V
Operating Temperature Range	Topr	0	25	70	°C
Output Load(effective)	R_L	-	37.5	-	Ω
Reference Load(effective) Resistor	Rset	-	658	-	Ω
Reference Voltage	$V_{BIA}S$	-	0.7	-	V
Data Input Setup Time	T_S	4	-	-	ns
Data Input Hold Time	T_H	1	-	-	ns
Clock Cycle Time	T_{CLK}	25	-	-	ns
Clock Pulse Width High	T_{PWH}	12	-	-	ns
Clock Pulse Width Low	T_{PWL}	12	-	-	ns
Zero_level Voltage	V_{OZ}	-10	-5	+10	mV
irset Current	$i_{rse}t$	0.9	1.06	1.1	mA

NOTES

1. It is strongly recommended that all the supply pins (VDD25AA1,VDD25AD1) be powered from the same source and all the ground pins(VSS25AA1,VSS25AD1,VBBA) avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Resolution	-	-	-	10	Bits
Full Scale Current per Channel	Ifs	-	34	-	mA
Differential Linearity Error	DLE	-	±0.75	±1.0	LSB
Integral Linearity Error	ILE	-	±1.0	±2.0	LSB
Monotonicity	-	Guaranteed			-
Output Compliance	VOC	0	-	+1.3	V
Power Dissipation	PDISS	80	95	110	mW

NOTES

1. Converter Specifications (unless otherwise specified) : VDD25AA1=VDD25AD1=2.5V VSS25AA1=VSS25AD1=VBBA=GND, Ta=25°C, Rset=658Ω, R_{LOAD1}=R_{LOAD2}=R_{LOAD3}==R_{LOAD4}=R_{LOAD5}=R_{LOAD6}=37.5Ω C_{CCOMP}=0.1uF
2. TBD : To Be Determined

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Analog DAC output capacitance	C_{IN}	-	20	-	pF
Minimum delay from sel transition to PRE transition low	T_{selL}	100	-	-	ns
Minimum delay from PRE transition low to valid dtout output	T_{DET_VAL}	100	-	-	ns
Minimum Pulse width low for PRE	T_{SPWL}	200	-	-	ns
Mismatching	mm	-	11	-	LSB
Power Supply Rejection Ratio(5.8KHz)	PSRR	35	45	-	dB
Conversion Rate	F_{CON}	-	30	40	MHz
Analog Output Delay	Td	-	10	-	ns
Analog Output Rise Time	Tr	-	5	-	ns
Analog Output Fall Time	Tf	-	5	-	ns
Analog Output Settling Time	Tset	-	60	-	ns
Clock & Data Feedthrough	FDTHR	25	30	-	dB
Glitch Impulse	Gl	-	±100	±200	pv*sec
Pipeline Delay	Top	0.5	0.7	1.0	CLK
Supply Current	Is	30	38	45	mA

NOTE:

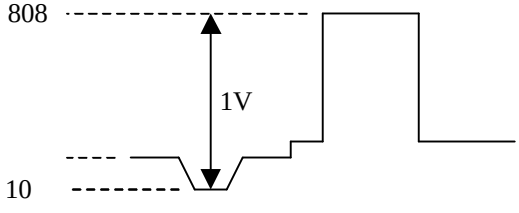
- The above parameters are not tested through the temperature range, but these are guaranted over the full temperature range.
- Clock & data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs.
- Settling time does not include clock and data feedthrough . Glitch impulse include clock and data feedthrough.

This is single 10bit 30MSPS digital to analog data converter and uses current-segment architecture for 4bits of MSB sides and binerary-weighted architecture for 6bits of LSB side. It contains of 1st latch block, decoder block,2nd latch block,OPA block,CM(current mirror)block ,BGR(Band Gap Reference) block, Auto-load detect block and analog switch block, etc. This core uses reference current which decide the 1LSB current by dividing the reference current by 32times. So the reference current must be constant and it can be constant by using OPA block with high DC gain. The most significant block of this core is analog switch block and it must maintain the uniformity at each switch, so layout designer must care of it. And more than 90% of supply current is dissipated at analog switch block. And it uses samsung standard cell as all digital cell of latch, decoder and buffer, etc. And to adjust full current output range, you must decide the Rset value(connected to IRSET pin) and. Its voltage output can be obtained by connecting external R_{L1} to IO1 pin. Its maximum output voltage limit is Compliance vlotage. So you must decide the R_{L1}, Vbias and Rset carefully not to exceed the output voltage limit. It contains PDAC pins for power-save of only analog switch and ALLPD for power-down mode of all blocks. Even though analog switch block enter power-save mode by setting PDAC high, the reference block(OPA block,CM block, BGR block) is still alive, but if ALLPD is activated(high), then all blocks of this core is disable regardless of PDAC, so at this case supply current is almost just about the sum of leakage. You cant check the BGR's output voltage by checking the VBIAS pin.

The user can detect the presence of an expected load on the output by configuring the DAC digital inputs such that the detection comparator threshold(0.53V) is a useful threshold for presence of load resistance. Set SEL high to select the DAC output as a input of autoload detection block input. Transition PRE to low, wait for settling DTOUT value and return PRE back to high.

The IRSET pin creates a +0.7VDC reference that can be forced with an external reference voltage ap pin VBIAS. This voltage when combined with the external resistor attached to the IRSET pin sets the output current range for all six DACs. The following example shows how to create a 1Vpk-pk output for a 100 IRE NTSC signal. ANy other required variations can easily be calculated from the supplied equations. Please remember that these are ideal equations, the mismatch tolerances from the data sheet should be taken into account for any calculations.

The <figure 1> diagram shows a typical relationship between DAC input and voltage output.



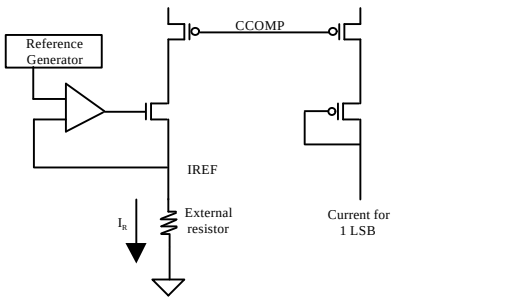
An example 10-bit DAC relationship input code verse output level

<figure 1>

The <figure 2> diagram shows the basic bias-generator and analog current switch.

From this diagram the number of DAC codes for a 1V delta output is :

C100 = 808 - 10 = 798



<figure 2>

If a standard doubly terminated 75 Ohm line is assumed :

$$I_{100} = \frac{V_{100}}{R_{LOAD}} = \frac{1}{37.5} = 26.666mA$$

The relationship between the IR reference current and DAC output current is shown below.

IR = 32 LSB

From the previous equation we have:

$$R_{SET} = \frac{irset}{I_R} = \frac{0.7V}{1.069mA} = 654\Omega$$

Summation of all equations gives :

$$R_{SET} = \frac{irset * C_{100} * R_{LOAD}}{32 * V_{100}}$$

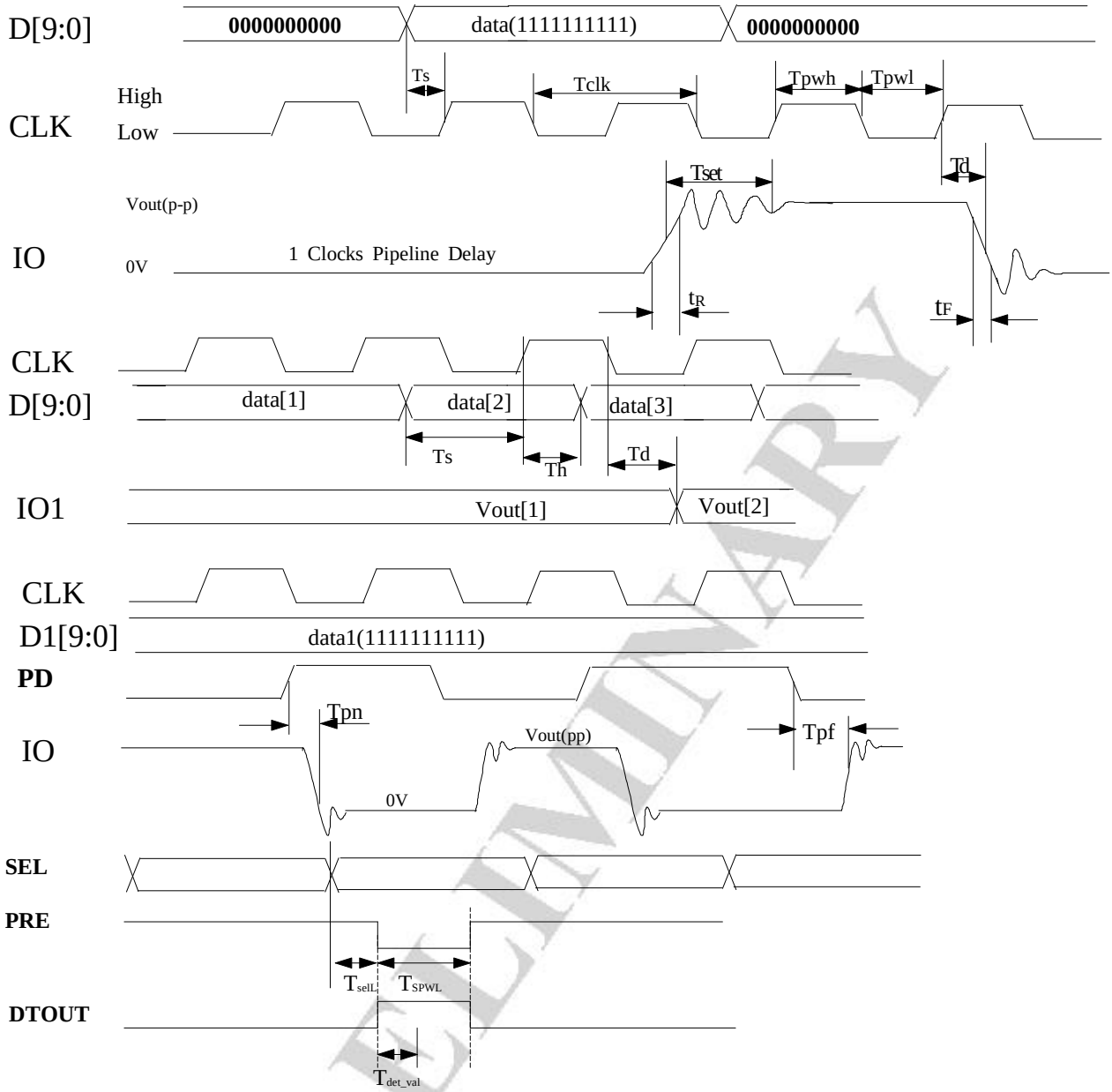
For most video applications an external resistor of 649Ω(+/– 1%) would be selected when driving doubly terminated loads (37.5Ω), and an external resistor of 1.3KΩ (+/– 1%) would be selected when driving loads of 75Ω, in order to have 798 DAC codes correspond to a 1V delta output voltage swing. Then the DAC output levels and the associated codes are as shown below.

Table 1:Summary of DAC Voltage and Codes

Signal Level	CVBS/LUMA DAC Code	IRE Value	DAC Voltage
Max output	1023	137.2	1.282V
100% White	810	100	1.015V
Black	282	7.37	353mV
Sync	12	-40	15mV
White - Black	570	100	714mV delta
White - Wync	798	140	1V delta
Color burst	228	40	285mV delta

DAC voltages assume the standard 140 IRE = 1V. Numbers shown are for NTSC type video with a pedestal.

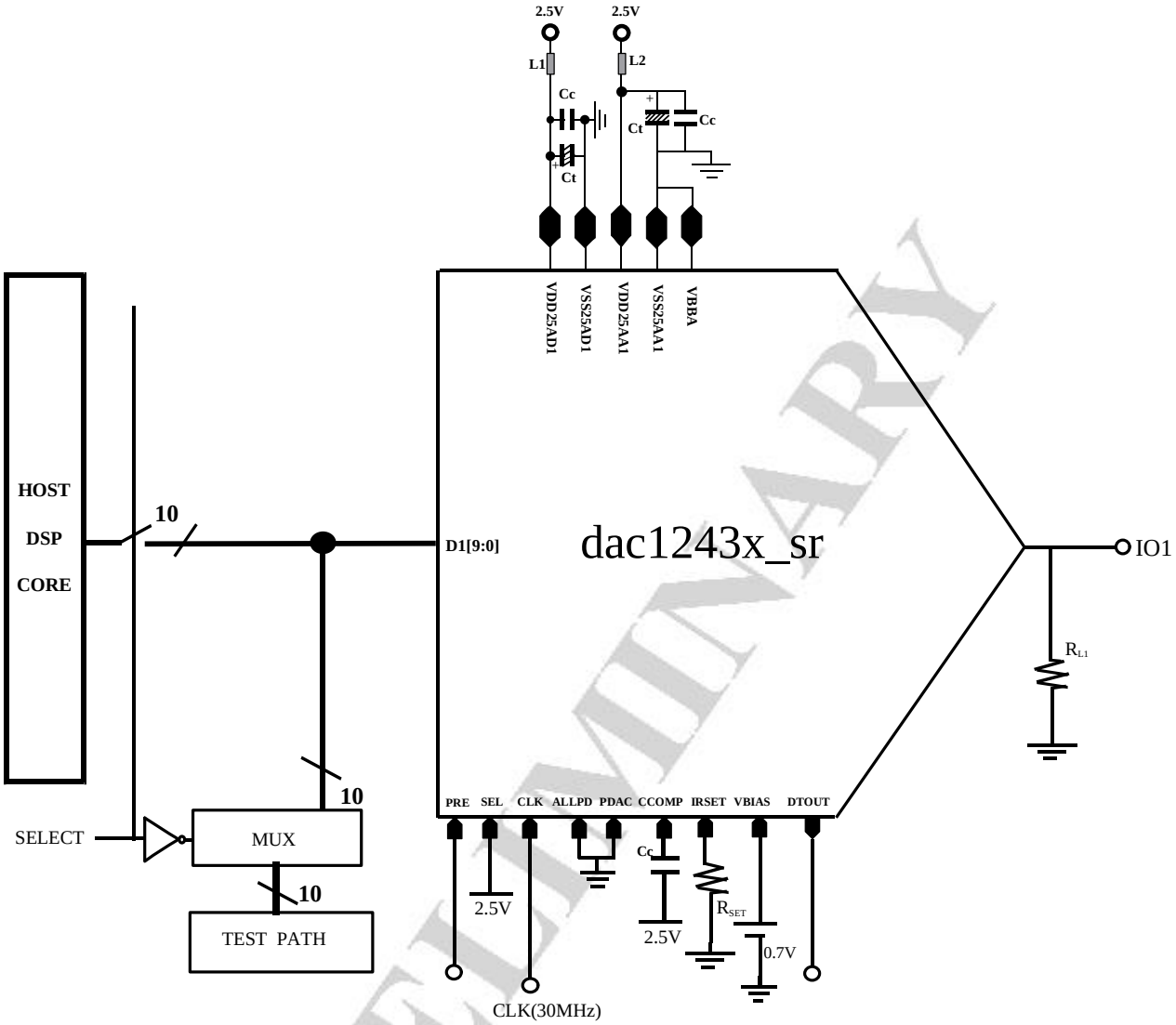
TIMING DIAGRAM



NOTES:

- The Behavioral Modeling is provided by Verilog
- Output delay(Td) measured from the 50% point of the rising edge of CLK to the full scale trasition
- Settling time(Tset) measured from the 50% point of full scale transition to the output remaining within ±1LSB iteration.
- Output rising(Tr)/falling(Tf) time measured between the 10% and 90% points of full scale transition.
- Any power_down doesn't need clock signal.
- ALLPD makes all of the blocks disable regardless of PDAC.
- The minimum Pulse Width Low of ALLPD should be longer than 1ms.
- The minimum Pulse Width Low of PDAC should be longer than 50ns.
- The minimum Pulse Width Low of ALLPD and PDAC should be longer than 20ns.

CORE EVALUATION GUIDE



LOCATION	DESCRIPTION
Cc	0.1μF
Ct	10μF
R_{SET}	658Ω
R_{L1}	37.5Ω
V_{BIAS}	0.7V

CORE LAYOUT GUIDE (OPTIONAL)

Layout DAC core replacement

- It is recommended that you use thick analog power metal. when connecting to PAD, the path should be kept as short as possible, and use branch metal to connect to the center of analog switch block.
- It is recommended that you use thick analog output metal(at least more than 30μm) when connecting to PAD, and also the path length should be kept as short as possible.
- Digital power and analog power are separately used.
- When it is connected to other blocks, it must be double shielded using N-well and P+ active to remove the substrate and coupling noise. In that case, the power metal should be connected to PAD directly.
- Bulk power is used to reduce the influence of substrate noise.
- It is recommended that analog metal line(including IRSET,VBIAS,IO1) and analog power metal line should be layouted alone and should not mixed with other noisy digital metal lines.
- If this core is used as a function block in larger main chip, you can join digital power metal of this core with the main digital power instead of using new digital power pad for this core. But you must use new analog power pad for the analog power of this core.

NOTE

To minimized noise pickup and reflections due to impedance mismatch, the DAC1243X_SR should be located as close as possible to the output connector.
The line between DAC output and monitor input should also be regarded as a transmission line. Due to the fact, it can cause problems in transmission line mismatch. As a solution to these problems, the double-termination methods used.
By using this, both ends of the termination lines are matched, providing an ideal, non-reflective system.