

FQD2N60C/FQU2N60C 600V N-Channel MOSFET

Features

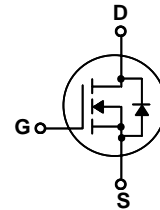
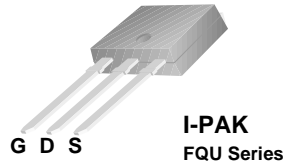
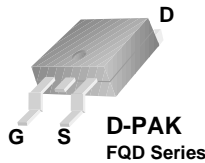
- 1.9A, 600V, $R_{DS(on)} = 4.7\Omega @ V_{GS} = 10V$
- Low gate charge (typical 8.5 nC)
- Low Crss (typical 4.3 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS Compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.



Absolute Maximum Ratings

Symbol	Parameter	FQD2N60C / FQU2N60C	Units
V_{DSS}	Drain-Source Voltage	600	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	1.9	A
	- Continuous ($T_C = 100^\circ\text{C}$)	1.14	A
I_{DM}	Drain Current - Pulsed (Note 1)	7.6	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	120	mJ
I_{AR}	Avalanche Current (Note 1)	1.9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)*	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	44	W
	- Derate above 25°C	0.35	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.87	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	--	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD2N60C	FQD2N60C	D-PAK	-	-	
FDU2N60C	FDU2N60C	I-PAK	-	-	

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	600	--	--	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 480 V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.95 A	--	3.6	4.7	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 0.95 A (Note 4)	--	5.0	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	180	235	pF
C _{oss}	Output Capacitance		--	20	25	pF
C _{rss}	Reverse Transfer Capacitance		--	4.3	5.6	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 2 A, R _G = 25 Ω	--	9	28	ns
t _r	Turn-On Rise Time		--	25	60	ns
t _{d(off)}	Turn-Off Delay Time		--	24	58	ns
t _f	Turn-Off Fall Time		(Note 4, 5)	--	28	66
Q _g	Total Gate Charge	V _{DS} = 480 V, I _D = 2 A, V _{GS} = 10 V	--	8.5	12	nC
Q _{gs}	Gate-Source Charge		--	1.3	--	nC
Q _{gd}	Gate-Drain Charge		(Note 4, 5)	--	4.1	--
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.9	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	7.6	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.9 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 2 A, di _F / dt = 100 A/μs (Note 4)	--	230	--	ns
Q _{rr}	Reverse Recovery Charge		--	1.0	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 56mH, I_{AS} = 2A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 2A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

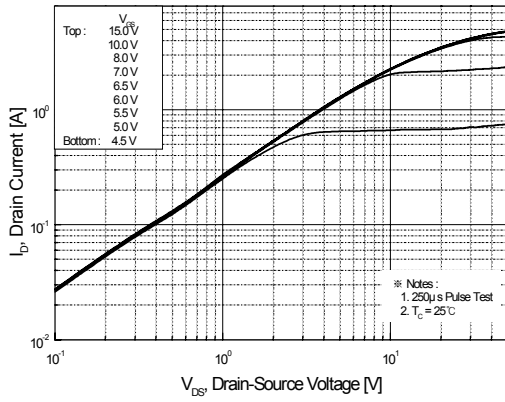


Figure 2. Transfer Characteristics

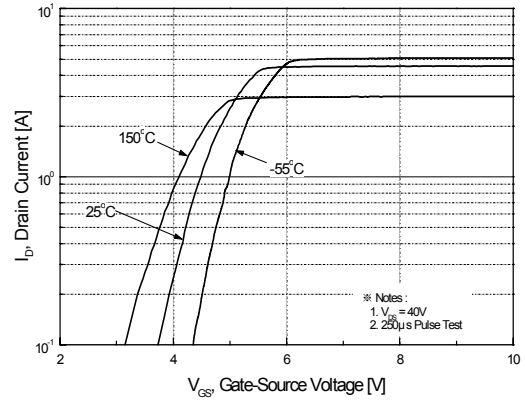


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

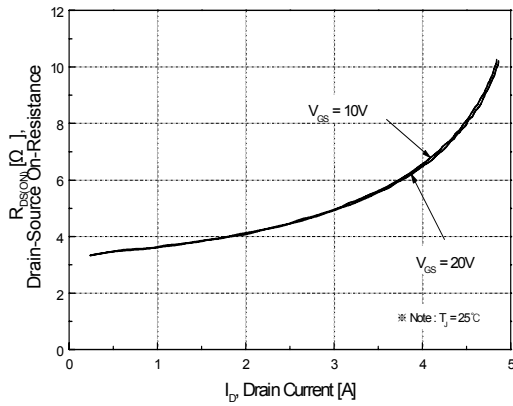


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

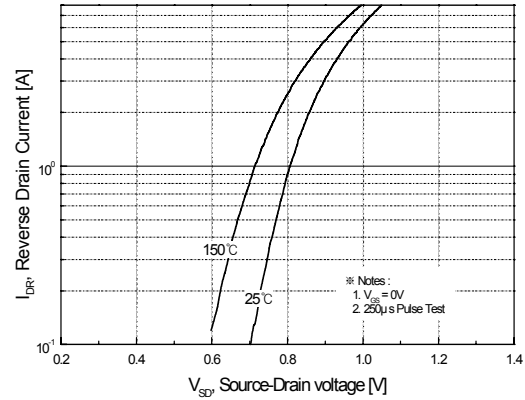


Figure 5. Capacitance Characteristics

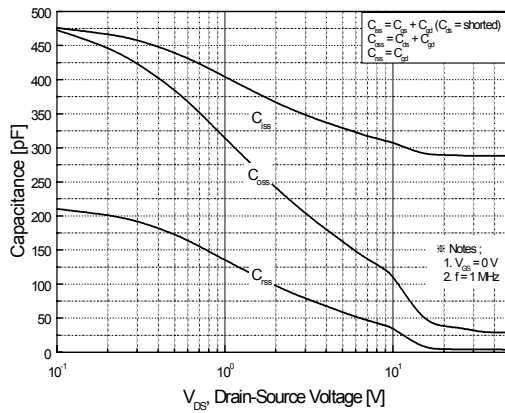
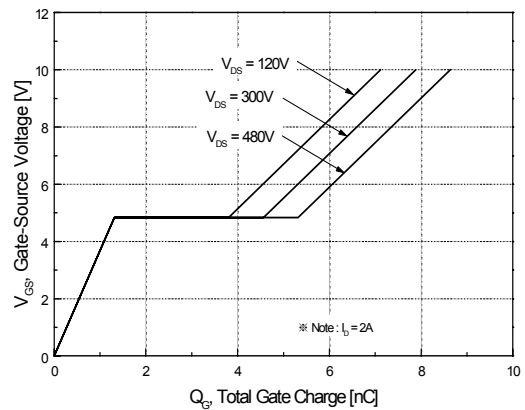


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

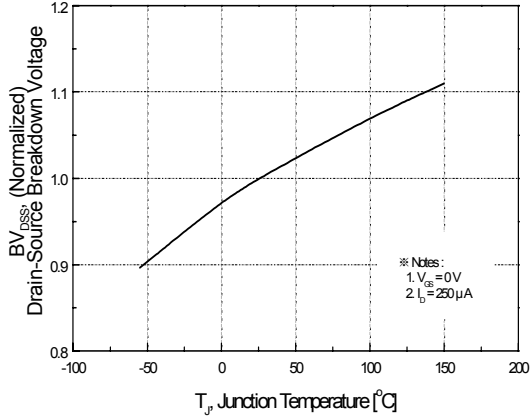


Figure 8. On-Resistance Variation vs. Temperature

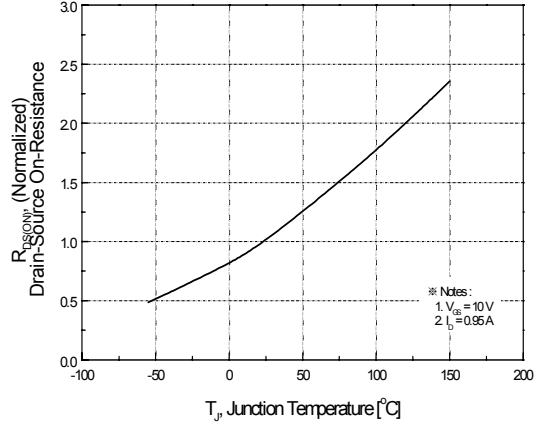


Figure 9. Maximum Safe Operating Area

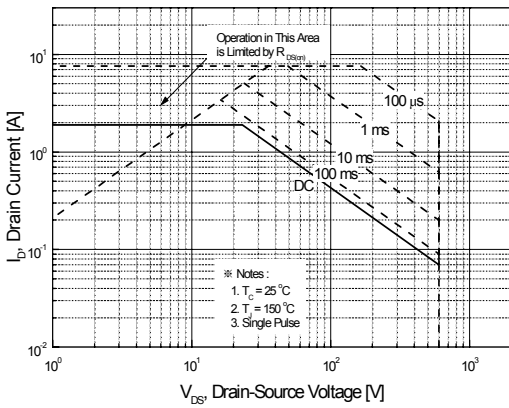


Figure 10. Maximum Drain Current vs. Case Temperature

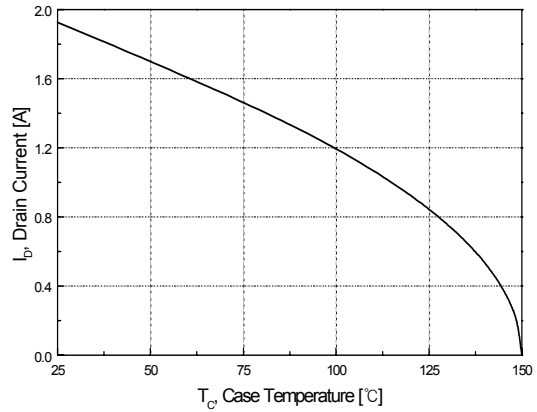


Figure 11. Typical Drain Current Slope vs. Gate Resistance

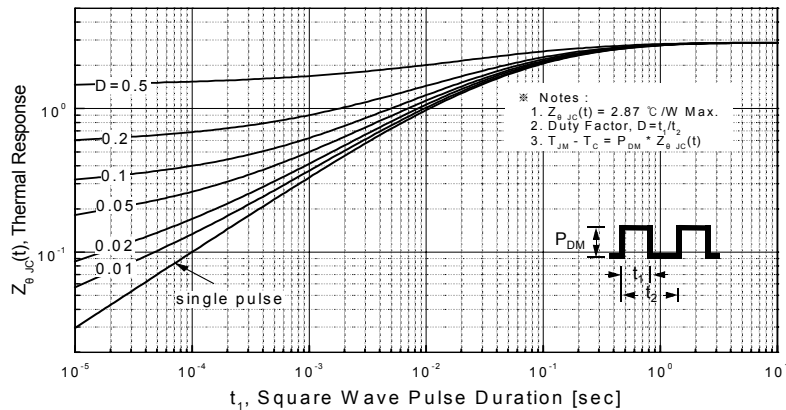
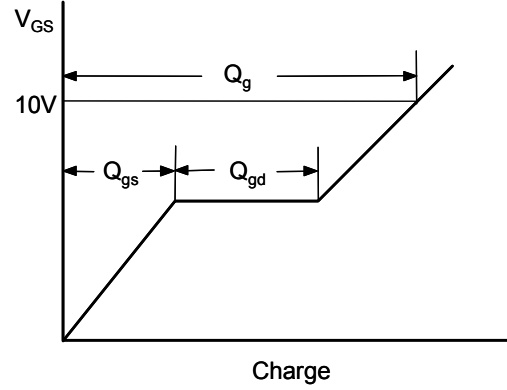
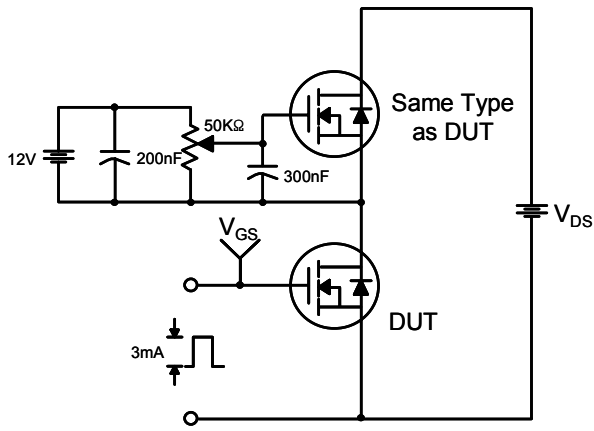
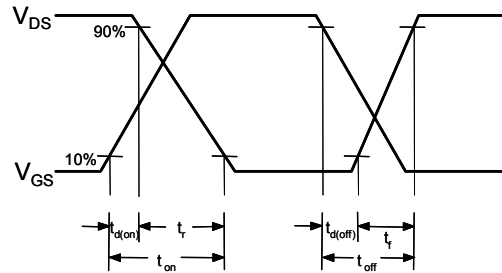
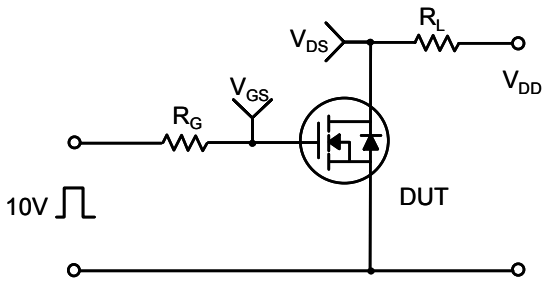


Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance

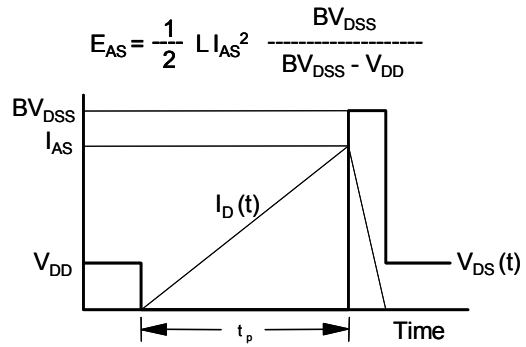
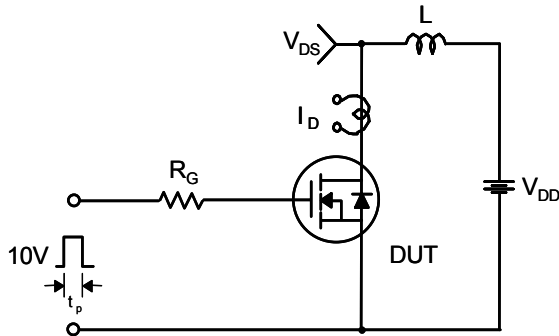
Gate Charge Test Circuit & Waveform



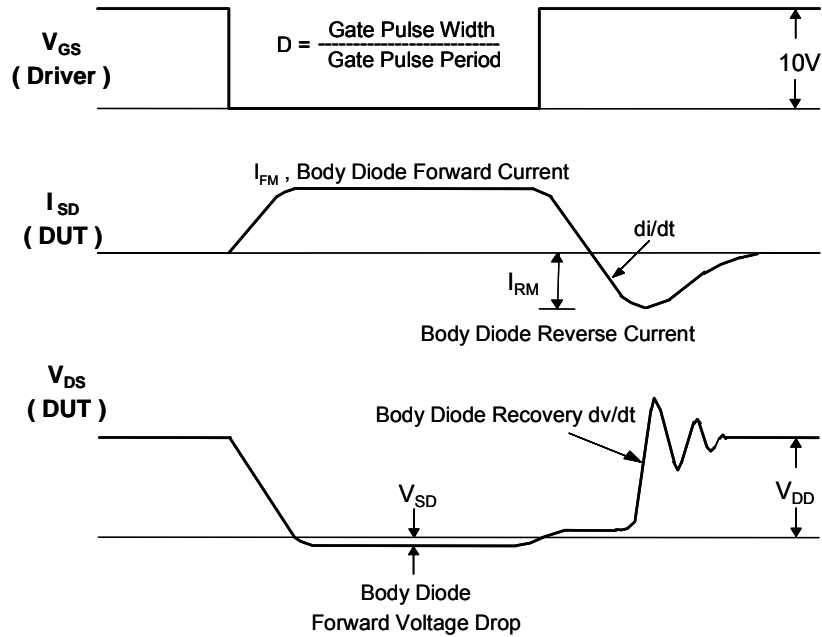
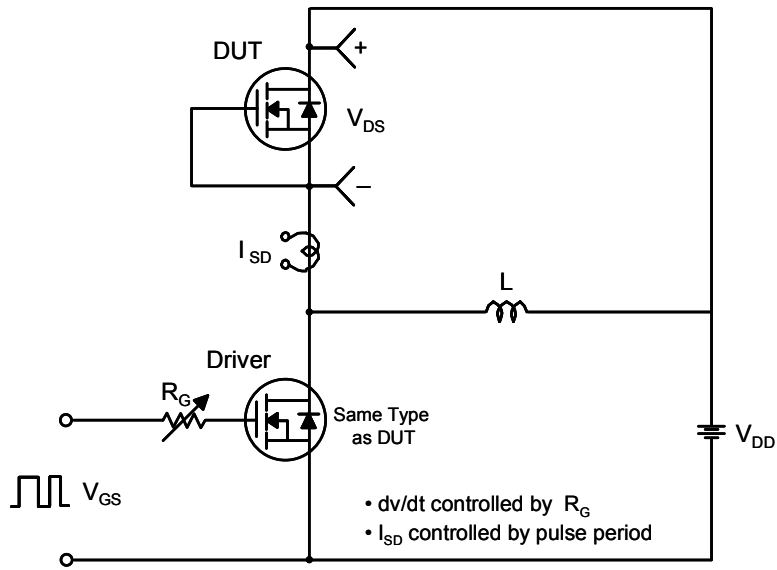
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

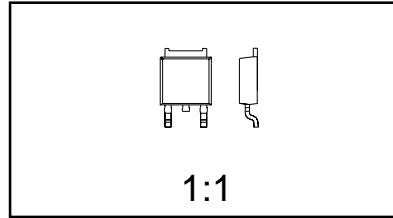
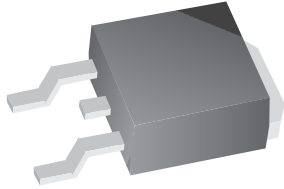


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-252 (DPAK) (FS PKG Code 36)

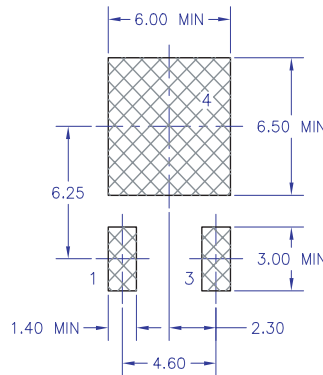
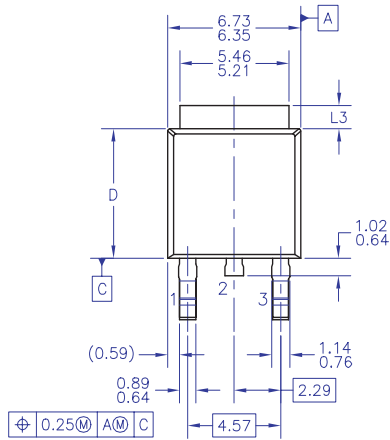


1:1

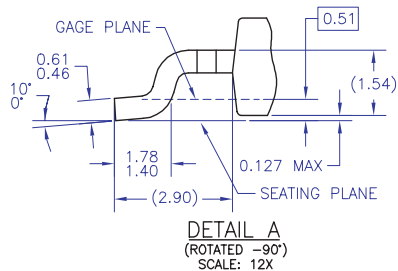
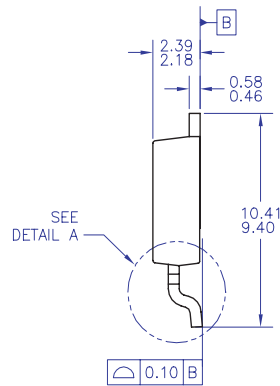
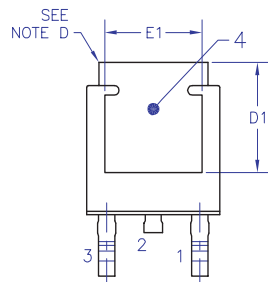
Scale 1:1 on letter size paper

Dimensions shown below are in:
millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION



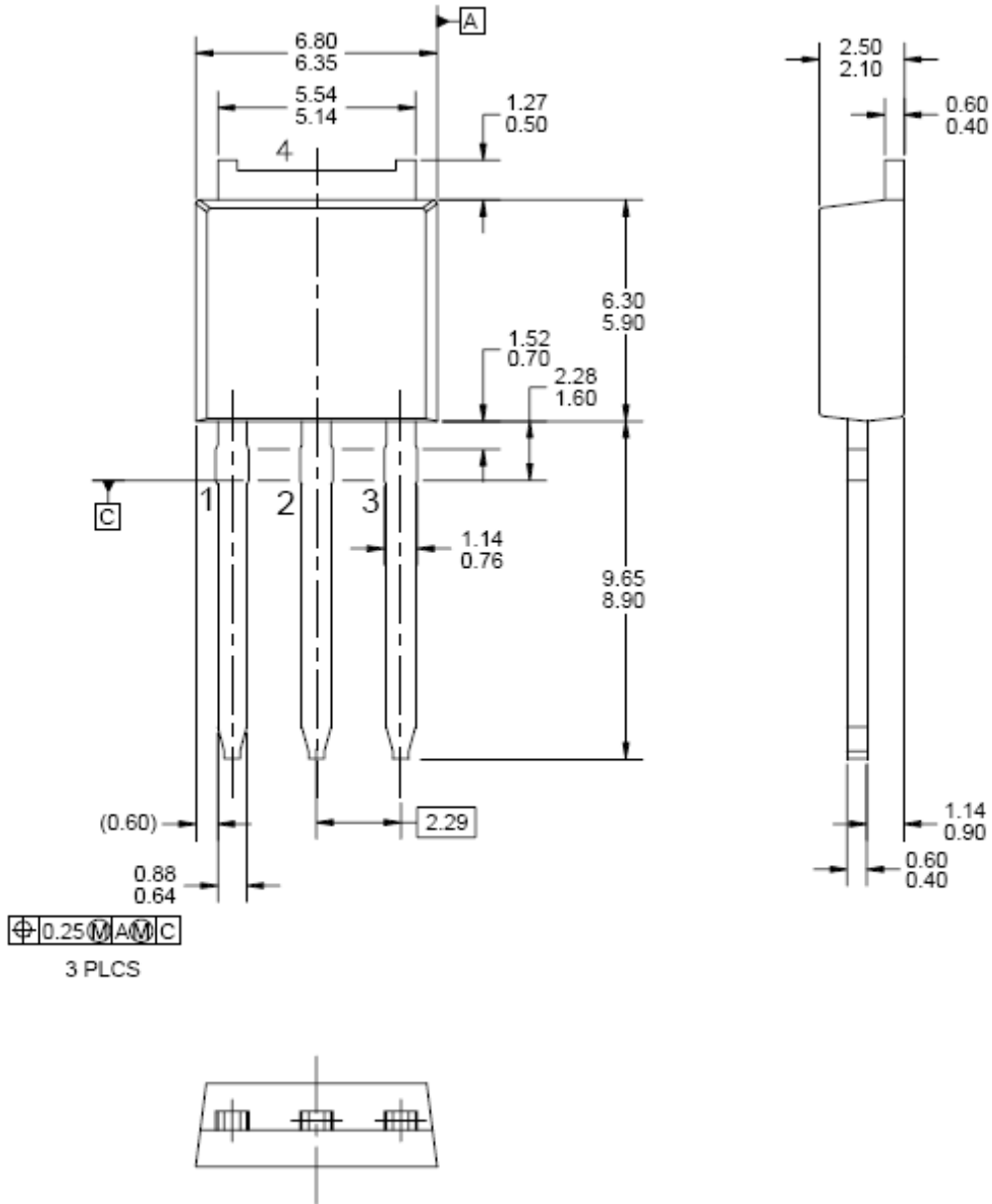
NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

Mechanical Dimensions

I - PAK



Dimensions in Millimeters


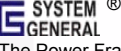


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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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