OKI Semiconductor

MSM6789A/6789L

SBC Solid-State Recorder IC

GENERAL DESCRIPTION

The MSM6789A / 6789L, an improved version of MSM6788, is a solid-state recorder developed using the Sub Band Coding (SBC) method.

Just like MSM6788, the MSM6789A/6789L has a stand-alone mode and a microcontroller interface mode. In the stand-alone mode, record/playback conditions can be selected from pins and the MSM6789A/6789L can be controlled by a simple drive timing. In the microcontroller interface mode, record/playback can be controlled by commands from the microcontroller, and more functions are available than in the stand-alone mode.

The MSM6789A/6789L can directly drive serial voice ROM as external memory as well as serial register or general-purpose DRAM* (1-bit \times or 4-bit \times type selectable) as external memories, which allows a recording and playback circuit with fixed messages to be built easily. The method from microcontroller is the same as the MSM6788.

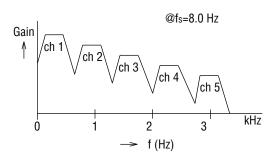
* Only for MSM6789A

Difference between MSM6788 and MSM6789A

	MSM6788	MSM6789A
General DRAM	Unavailable	Available
Unvoiced-part elimination function	No	Yes
PCM playback	No	Yes

• SBC method:

The SBC method divides voice frequencies into five bands and codes the component for each of the bands separately, as shown below.



Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

• Difference between MSM6789A and MSM6789L

Parameter	MSM6789A	MSM6789L
Operating voltage	4.5 to 5.5 V	3.0 to 3.6 V
External memory	General-purpose DRAM, 32 Mbits (max.)	16 Mbits (max.)
	1-Mbit DRAM (MSM514256B, MSM511000B)	4 Mbits (MSM66V84B)
	4-Mbit DRAM (MSM514400C, MSM514100C)	
	16-Mbit DRAM (MSM511740CA, MSM5116100A)	
	ARAM*, 32 Mbits (max.)	
	Serial register, 32 Mbits (max.)	
	4 Mbits (MSM6684B)	
	8 Mbits (MSM6685)	

^{*} Use ARAM which has no failed bits in its first 64 Kbits.

STAND-ALONE MODE

FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in 12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter

Attenuation characteristics -40 dB/oct

• External memories

MSM6789A (5 V version)

General-purpose DRAM, 32 Mbits maximum (for variable messages)

1-Mbit DRAM: Can be directly driven (MSM514256B, MSM511000B)

4-Mbit DRAM: Can be directly driven (MSM514400C, MSM514100C)

16-Mbit DRAM: Can be directly driven (MSM5117400A, MSM5116100A)

ARAM, 32 Mbits maximum (for variable messages)

Note: Use the first 64 Kbits with no failed bits for the ARAM.

Serial register, 32 Mbits maximum (for variable messages)

4-Mbit serial register: Can be directly driven (MSM6684B)

8-Mbit serial register: Can be directly driven (MSM6685)

MSM6789L (3.3 V version)

Serial register, 16 Mbits maximum (for variable messages)

4-Mbit serial resister: Can be directly driven (MSM66V84B)

MSM6789A (5 V version) and MSM6789L (3.3 V version)

Serial voice ROM, 4 Mbits maximum (for fixed messages)

1-Mbit serial voice ROM: Can be directly driven (MSM6595A)

2-Mbit serial voice ROM: Can be directly driven (MSM6596A)

3-Mbit serial voice ROM: Can be directly driven (MSM6597A)

• Bit rate

 $10.0,\,12.6,\,16.0$ kbps (at 8~kHz sampling freq.)

7.5, 9.5, 12.0 kbps (at 6 kHz sampling freq.)

Maximum recording time (when one 8-Mbit serial register is connected)

13.8 minutes (for 10.0 kbps SBC)
11.0 minutes (for 12.6 kbps SBC)
14.6 minutes (for 9.5 kbps SBC)

8.6 minutes (for 16.0 kbps SBC) 11.5 minutes (for 12.0 kbps SBC)

Number of phrases

63 phrases for variable messages

63 phrases for fixed messages

- Standard linear PCM playback or OKI nonlinear PCM playback can be selected.
- Voice triggered starting function (voice detect level can be set)
- Unvoiced-part elimination function (voice detect level can be set)
- Pausing function

Master clock frequency:
 6.0 MHz to 8.192 MHz

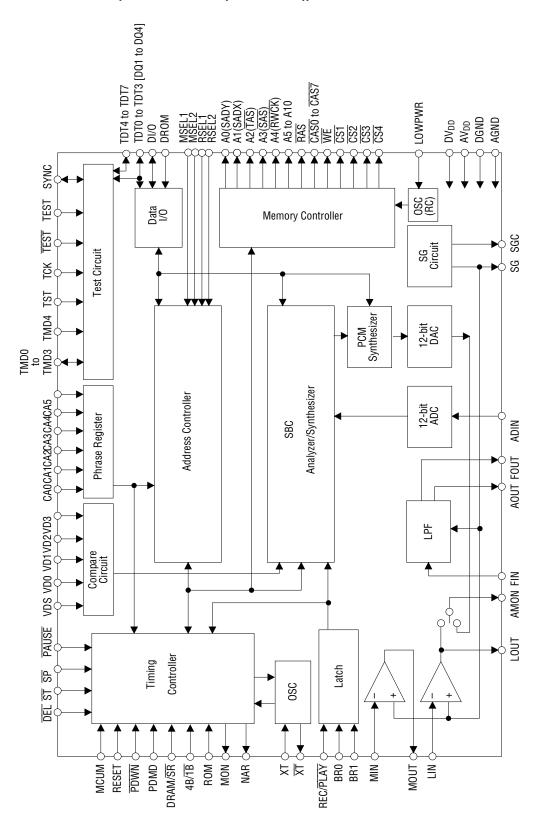
• Power supply voltage:

MSM6789A: Single 5 V power supply MSM6789L: Single 3.3 V power supply

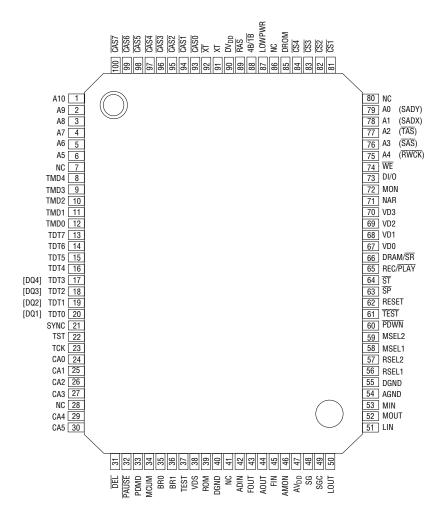
Package options:

MSM6789A: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789AGS-BK) MSM6789L: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789LGS-BK)

BLOCK DIAGRAM (for MSM6789A (5 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789A (5 V Version))



100-Pin Plastic QFP

(): Pins for connecting serial voice ROM[]: Pins for connecting 4-bit × type DRAM

NC: No-connection pin

PIN DESCRIPTIONS (for MSM6789A (5 V Version))

Pin	Symbol	Туре	Description
90	DV _{DD}		Digital power supply. Insert a bypass capacitor of 0.1 µF or more between this
90			pin and the DGND pin.
47	۸۱/		Analog power supply. Insert a bypass capacitor of 0.1 µF or more between this
41	AV _{DD}		pin and the AGND pin.
40, 55	DGND	_	Digital ground.
54	AGND	_	Analog ground.
48, 49	SG, SGC	_	Output for analog circuit reference voltage (signal ground).
53	MIN	ı	Inverting input of the built-in OP amplifier. The non-inverting input pin is
51	LIN	'	internally connected to SG (signal ground).
52	MOUT	0	Output of the built-in OP amplifier for MIN and LIN.
50	LOUT	0	Output of the built-in OF amplifier for wind and Line.
46	AMON	0	Connected to the LOUT pin in the recording mode and to the DA converter
	AIVION	0	output in the playback mode. This pin connects the built-in LPF input (FIN pin).
45	FIN	I	Input of the built-in LPF.
43	FOUT	0	Output of the built-in LPF. This pin connects the AD converter input (ADIN pin).
42	ADIN	I	Input of the built-in 12-bit AD converter.
44	AOUT	0	Output of the built-in LPF. This pin outputs playback waveforms and connects
	AUUT	U	an external speaker drive amplifier.
			This pin selects whether memory to be connected externally is DRAM or serial register.
66	DRAM/SR	I	Low level : Serial register
			High level : DRAM
			This pin selects either 1-bit \times type DRAM or 4-bit \times type DRAM.
88	4B/1B	I	Low level : 1-bit × type
			High level : 4-bit × type
79	A0 (SADY)		These pins connect to A0 and A1 of DRAM at the time of DRAM selection. They also
78	A1 (SADX)	0	connect to SAD pin of serial register and serial voice ROM at the time of serial
	AT (OADA)		register selection. These pins output leading addresses of read/write.
			This pin connects to A2 of DRAM at the time of DRAM selection. It also connects
77	A2 (TAS)	0	to TAS pin of serial register and serial voice ROM at the time of serial register selection.
	/12 (1710)		This pin is used to set serial addresses from the SADX and SADY pins into the
			internal address counter of the serial register and serial voice ROM.
			This pin connects to A3 of DRAM at the time of DRAM selection. It also connects
76	A3 (SAS)	0	to the \overline{SAS} pin of the serial register and the \overline{SASX} and \overline{SASY} pins of the serial voice
			ROM at the time of serial register selection. Clock pin to write serial addresses.
			This pin connects to A4 of DRAM at the time of DRAM selection. It also connects
75	A4 (RWCK)	F(RWCK) 0	to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM at
			the time of serial register selection. Clock pin to read data from and write data into
			the serial register.
1-6	1-6 A10-A5 O	0	This pin connects to pins A5-A10 of DRAM at the time of DRAM selection.
I-U AIU			This pin outputs addresses of read/write.

7.4				Description					
	WE	_	Write Enable.	This pin conn	ects to the WE	pin of the seri	al register and DRAM.		
74	VVE	0	This pin selects	This pin selects either read or write mode.					
70	DI/O	1/0	Data I/O. This	pin connects t	o the DIN and	DOUT pins of	the serial register and		
73	טווט	1/0	DRAM. This pin	outputs write	data and input	s read data.			
85	DROM	ı	Data ROM. Th	is pin connect	s to the DOUT	pin of the seri	al voice ROM.		
89	RAS	0	This is a row add	dress strobe pi	n of DRAM at	the time of DR	AM selection.		
03_100 I	CASO- CAS7	0	CAS7, an addres	ss output pin,	-		ime of DRAM selection. RAM at the time 16-Mbit		
			DRAM selection.						
	CS1								
	CS2	0	-	•	•	of the serial reg	gister and the $\overline{\text{CS}}$ ($\overline{\text{CS1}}$,		
	CS3		$\overline{\text{CS2}}, \overline{\text{CS3}})$ pins of	of the serial vo	ice ROM.				
	CS4								
I	MSEL1	I	These nins selec	These pins select the capacity of the memory to be connected externally.					
59	MSEL2	I	-						
			• When DRAM	1 is selected (D	RAM/SR = Hig	h level)	be connected externallly.		
			MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity		
			<u>L</u>	L	L	L	1M × 4		
			L	L	L	H .	4M × 1		
			<u>L</u>	L .	H	L	1M × 8		
			<u>L</u>	L	H .	H	$1M \times 4 + 4M \times 1$		
			<u>L</u>	H	L	L	4M × 2		
56	RSEL1	l	<u>L</u>	H	L	H	4M × 2		
	RSEL2	' 	L	H	Н	L	4M × 3		
37	HOLLZ		L	H	H	H	4M × 3		
			H	L	L	L	4M × 4		
			H	L	L	H	16M×1		
			H	L	Н	L	4M × 6		
			H	L	H	H	4M × 6		
			H	H	L	L	4M × 8		
			H	Н	L	H	4M × 8		
			H	Н	H	L	16M × 2		
			H	Н	Н	Н	16M × 2		

Pin	Symbol	Туре			Descript	ion		
			• When serial	register is sele	cted (DRAM/SI	\overline{R} = Low level)		
			MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity	
			L	L	L	L	4M × 1	
			L	L	L	Н	4M × 2	
56	RSEL1	ı	L	L	Н	L	4M × 3	
57	RSEL2	' I	L	L	Н	Н	4M × 4	
07	TIOLLE	'	L	Н	L	L	8M×1	
			L	Н	L	Н	8M × 2	
			L	Н	Н	L	8M×3	
			L	Н	Н	Н	8M × 4	
87	LOWPWR	I	This pin selects power down w Low level : 15 High level : 125	hen DRAM is s µs max.	•	riod of DRAM	at the time of	
			Mode Select	tion.				
34	MCUM	I	Low level : Sta	nd-alone mode	!			
			High level : Mid	crocontroller in	terface mode			
62	RESET	ı	A high input le	vel causes the	MSM6789A to	be initialized	and to go into the power	
		-	down state.					
					-		goes to the power down	
20	DD14/AL			· ·	-		SM6789A to be reset.	
60	PDWN	I	is halted, and w	ill be maintaine	d in the power	down state wh	pperation, the MSM6789A ile PDWN is low level.	
			-				recording will be performed.	
91	XT	I					ed, input the clock through	
							et to the ground level.	
92	XT	0	Oscillator Co	onnection. W	/hen an extern	al clock is use	d, this pin must be left	
37	TEST			.		TEOT win and	- blab level to the TFOT also	
61	TEST	ı	MSM6789A	est. Input a id	ow level to the	1EST pin and a	a high level to the TEST pin.	
9-12	TMD3-TMD0							
13-20	TDT7-TDT0	1/0	MSM6789A	Test. This pin	must be left o	pen.		
21	SYNC							
17-20	TDT3-TDT0	I/O	Connect these pins to DQ1-DQ4 of DRAM at the time of 4-bit × type DRAM					
11-20	[DQ4]-[DQ1]	1/0	selection. Othe	erwise these pi	ns must be lef	t open as they	are MSM6789A test pins.	
22	TST							
23	TCK	I	MSM6789A	Test. Input a l	ow level signa	l.		
8	TMD4							

Pin	Symbol	Туре						Desc	ription	
39	ROM	I	operation	Playback Operation. When set to low, this pin selects the record/playback operation (only for the SBC method). When set to high, it selects the ROM playback operation (for the SBC and PCM methods).						
65	REC/PLAY	ı	the ROI	VI play	back c	perati	on. WI	nen se		. This pin is invalid during is the playback mode.
64	ST	ı	Start F or ROM	-				evel pı	ılse is applied to	this pin, the record/playback
63	SP	I	Stop F or ROM	_				vel pu	lse is applied to	this pin, the record/playback
32	PAUSE	I	Playba or ROM							o this pin, the record/playback
31	DEL	I	or spec through ch00: ch01 After po	Phrase Delection. When a low level pulse is applied to this pin, all phrase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5, ch00:All phrase deletion ch01 to ch3F:Specified phrase deletion After power up, be sure to input a RESET signal and then delete all phrases. After completing this procedure, start the record/playback operation.						
24-30	CAO-CA5	I	Desire	ed Pho	rase \$	Speci s can b	ficati ne spe	on. cified in	•	the record/playback operation Remarks All phrase deletion A total of 63 phrases can be used for both record /playback and ROM playback operation.

Pin	Symbol	Туре		Description				
				•		of the following three ty n is invalid during the R0		
				BR1	BR0	Bit rate		
35	BRO	1		L	L	16.0 kbps	_	
36	BR1	'		L	Н	12.6 kbps	_	
				Н	L	10.0 kbps		
				Н	Н	Unused		
			Transition to t	he Power	-down Sta	te.		
			Low level: Ti	he MSM678	9A automati	cally goes to the power	r-down state, except	
						k operation is perform		
			_			ically goes to the stand	-	
33	PDMD*1		1			ot when the record/pla	-	
				-		se, the MSM6789A car	•	
					-	ting the RESET or PDV		
							ed for the built-in LPF, lying a high level to th	•
						igning a might level to the		
67-70	VD0-VD3	1	elimination.	e voice dete	נו ופעפו וטו נוו	ie voice inggered starti	ng and unvoiced-part	
				ne voice tria	nered starting	g or the unvoiced-part e	elimination	
			Voice triggere	•		th level to the VDS pin.		
						el with VD0 to VD3 pins		
38	VDS	ı	Unvoiced-par	t elimination	:Input a Low	level to the VDS pin. T	hen set the voice	
			·			l with VD0 to VD3 pins		
			Note: When neith	er the voice	triggered sta	arting nor the unvoiced	-part elimination is	
			used, input a Lov	level to VD	0 to VD3.			
72	MON	0	This pin outputs	a high level	while the re	cord/playback operation	on is being performed.	
			Output to indicat	e the enable	or disable s	tate of the operation f	or specifying a	
71	NAR	0	l ·			k is performed, the ne	xt phrase can	
			be specified after	the NAR pi	n goes to hi	gh positively.		

^{*1} When DRAM is selected, be sure to set the PDMD pin to a High level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V _{DD}	Ta=25°C	-0.3 to +7.0	V
Input voltage	V _{IN}	Ta=25°C	-0.3 to V _{DD} +0.3	V
Storage temperature	T _{STG}	_	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.5 to +5.5*4	V
Operating temperature	T _{op}	_	0 to +70	°C
Master clock frequencuy	f _{OSC}	_	6.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6789A (5 V Version))

DC Characteristics

 DV_{DD} = AV_{DD} =4.5 to 5.5 V^{*4} DGND=AGND=0 V, Ta=0 to 70° C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High input voltage	V _{IH}	_	0.8×V _{DD}	_	_	V
Low input voltage	V _{IL}	_	_	_	$0.2 \times V_{DD}$	V
High output voltage	V _{OH}	I _{0H} =-40 μA	V _{DD} -0.3	_		V
Low output voltage	V _{OL}	I _{OL} =2 mA	_	_	0.45	V
High input current *1	I _{IH1}	V _{IH} =V _{DD}	_	_	10	μΑ
High input current *2	I _{IH2}	V _{IH} =V _{DD}	_	_	20	μΑ
Low input currcent *1	I _{IL1}	V _{IL} =GND	-10	_	_	μΑ
Low input current *2	I _{IL2}	V _{IL} =GND	-20	_	_	μΑ
Low input current *3	I _{IL3}	V _{IL} =GND	-400	_	-20	μΑ
Operating current consumption	I _{DD}	f _{OSC} =8 MHz, no load	_	20	35	mA
	1 .	No load			10	
Dower down ourrent	I _{DDS1}	Serial register connected	_	_	10	μΑ
Power down current		No load		200		
	I _{DDS2}	DRAM connected	_	200		μΑ

^{*1} Applies to all inputs excluding the XT pin.

^{*2} Applies to the XT pin.

^{*3} Applies to the input pins with pull-up resistor (ST, SP, PAUSE, DEL) excluding the XT pin.

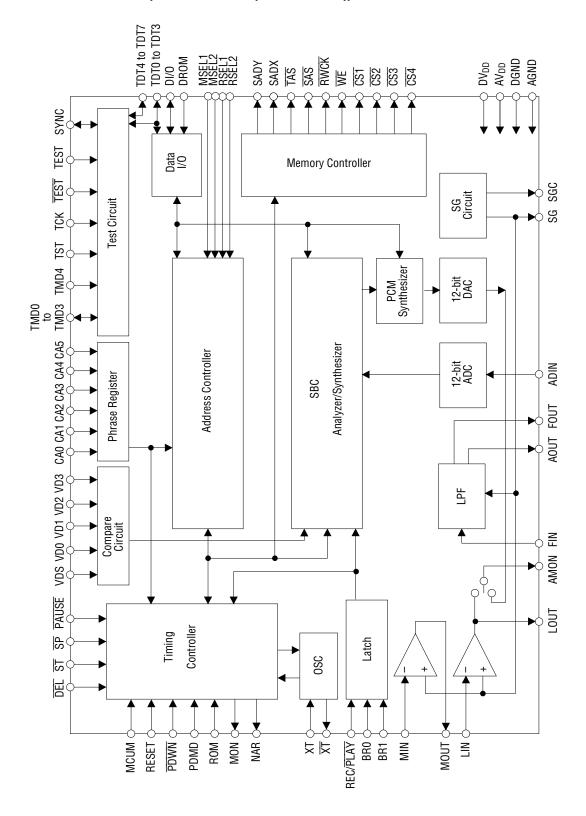
^{*4} The record/playback operation must be performed at the power supply voltage of 4.5 to 5.5 V. The MSM6789A operates at 3.5 to 5.5 V when the serial register is backed up.

Analog Characteristics

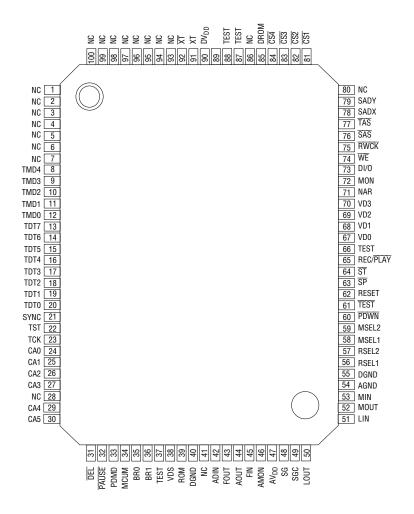
DV_{DD}=AV_{DD}=4.5 to 5.5 V DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DA output relative error	V _{DAE}	no load	_	_	10	mV
FIN admissible input voltage range	V _{FIN}	_	1	_	V _{DD} -1	V
FIN input impedance	R _{FIN}	_	1	_	_	ΜΩ
Op-map open loop gain	G _{OP}	f _{IN} =0 to 4kHz	40	_	_	dB
Op-amp input impedance	R INA	_	1	_	_	ΜΩ
Op-amp load resistance	R _{OUTA}	_	200	_	_	kΩ
AOUT load resistance	R _{AOUT}	_	50	_	_	kΩ
FOUT load resistance	R _{FOUT}	_	50	_	_	kΩ

BLOCK DIAGRAM (for MSM6789L (3.3 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789L (3.3 V Version))



100-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version))

DVDD DVDD Digital power supply. Insert a bypass capacitor of 0.1 μF or more between this pin and the DGND pin.	Pin	Symbol	Туре	Description
pin and the D6ND pin.	90	DVpp		Digital power supply. Insert a bypass capacitor of 0.1 μF or more between this
AVDD		טטיס		pin and the DGND pin.
pin and the AGND pin. 40, 55 DGND — Digital ground. 54 AGND — Analog ground. 58 SG, SGC — Output for analog circuit reference voltage (signal ground). 59 ILIN	47	AVnn	_	
Section 2015 Sect				
48, 49 SG, SGC — Output for analog circuit reference voltage (signal ground). 1 Inverting input of the built-in OP amplifier. The non-inverting input pin is internally connected to SG (signal ground). 52 MOUT 50 Output of the built-in OP amplifier for MIN and LIN. 6 AMON 0 Output of the built-in OP amplifier for MIN and LIN. 6 AMON 0 Output of the built-in OP amplifier for MIN and LIN. 6 FIN 1 Input of the built-in LPF. This pin connects the built-in LPF input (FIN pin). 45 FIN 1 Input of the built-in LPF. This pin connects the AD converter output in the playback mode. This pin connects the AD converter input (ADIN pin). 42 ADIN 1 Input of the built-in LPF. This pin connects the AD converter input (ADIN pin). 44 AOUT 0 Output of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. 79 SADY 0 They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write. This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. Wite Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin connects t	-	+	_	
Inverting input of the built-in OP amplifier. The non-inverting input pin is internally connected to SG (signal ground). Tourname	-		_	
Internally connected to SG (signal ground).	-	1	_	
Solution Output of the built-in OP amplifier for MIN and LIN.			ı	
Counce to the built-in OP amplifier for MIN and LIN.				internally connected to SG (signal ground).
AMON Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. This pin connects the built-in LPF input (FIN pin). Input of the built-in LPF. Input of the built-in LPF. This pin connects the AD converter input (ADIN pin). Input of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. Dutput of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write. This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and the TASX and TASX pins of the serial voice ROM. This pin connects to the SAS pin of the serial register and the TASX and TASX pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the TASX pin of the serial register and the TASX and TASX pins of the serial voice ROM. Clock pin to read data from and write data into the serial register. WE WE WE WRITE Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DUN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. DATA CST CST CST Chip Select. These pins connects to TS pin of the serial register and the CS (CST, CSS) pins of the serial voice ROM.			0	Output of the built-in OP amplifier for MIN and LIN.
output in the playback mode. This pin connects the built-in LPF input (FIN pin). Input of the built-in LPF. Input of the built-in LPF. Input of the built-in LPF. This pin connects the AD converter input (ADIN pin). Input of the built-in LPF. This pin connects the AD converter input (ADIN pin). Input of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. Output of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write. This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and the SASX and SASY pins of the serial voice ROM. This pin connects to the SAS pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. WE Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. DI/O Chip Select. These pins connect to CS pin of the serial register and the CS (CS1, CS3) pins of the serial voice ROM.	50	LOUT		
output in the playback mode. This pin connects the built-in LPF input (FIN pin). Input of the built-in LPF. Input of the built-in LPF. This pin connects the AD converter input (ADIN pin). Input of the built-in LPF. This pin connects the AD converter input (ADIN pin). Input of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write. This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. WE WRITE Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. CSI CSI CSI Chip Select. These pins connect to CS pin of the serial register and the CS (CSI, CSI) pins of the serial voice ROM.	46	AMON	0	
FOUT 0 Output of the built-in LPF. This pin connects the AD converter input (ADIN pin). 42 ADIN 1 Input of the built-in 12-bit AD converter. 44 AOUT 0 Output of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. 79 SADY 78 SADX 0 They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write. 78 TAS 0 This pin connects to TAS pin of serial register and serial voice ROM. 78 TAS 0 This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. 76 SAS 0 This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. 75 RWCK 0 This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. 74 WE 0 Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. 73 DI/O I/O Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. 85 DROM I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. 81 CST CSZ CSS OCSS DIN Select. These pins connect to CS pin of the serial register and the CS (CST CSS) pins of the serial voice ROM.				
42 ADIN I Input of the built-in 12-bit AD converter. 44 AOUT 0 Output of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. 79 SADY 78 SADX 0 They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write. 77 TAS 0 This pin connects to TAS pin of serial register and serial voice ROM. 78 This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. 78 TAS 0 This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. 78 This pin connects to the TAS pin of the serial register and the TASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. 79 This pin connects to the TASY pin of the serial register and the TASY pins of the serial voice ROM. Clock pin to read data from and write data into the serial register. 79 TASY ON THIS pin connects to the TASY pin of the serial register and DASY pins of the serial voice ROM. This pin connects to the TASY pin of the serial register and DASY pins of the serial voice ROM. 70 This pin selects either read or write mode. 71 DIVO THIS pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. 82 DROM THIS PIN THIS PIN THIS PIN CONNECTS TO THE SERIAL POUT PIN OF THE SERIA			I	
AOUT Output of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier. They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write. This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. Bornam I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. Chip Select. These pins connect to CS pin of the serial register and the CS (CS1, CS3) pins of the serial voice ROM.		+	0	Output of the built-in LPF. This pin connects the AD converter input (ADIN pin).
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an external speaker drive amplifier. 79 SADY 78 SADX 0 They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write. 77 TAS 0 This pin connects to TAS pin of serial register and serial voice ROM. 78 TAS 0 This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. 78 TAS 0 This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. 79 THIS pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. 79 WE 0 Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. 70 DI/O Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. 85 DROM I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. 81 CS1 82 CS2 0 Chip Select. These pins connect to CS pin of the serial register and the CS (CS1, CS3) pins of the serial voice ROM.	44	AOUT	n	Output of the built-in LPF. This pin outputs playback waveforms and connects
output leading addresses of read/write. This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. WE Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. BE DROM Data ROM. This pin connects to the DOUT pin of the serial voice ROM. CST CST CST CST CST This pins of the serial register and the RDCK pin of the serial register and DRAM. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin connects to the DOUT pin of the serial voice ROM.		7.001		an external speaker drive amplifier.
This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. WE 0 Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. BE DROM I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. CST CST CST pin of the serial register and the CS (CST, CST) pins of the serial register and the CS (CST, CST) pins of the serial voice ROM.	79	SADY	0	They also connect to SAD pin of serial register and serial voice ROM. These pins
This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM. This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. DRAM. This pin outputs write data and inputs read data. Data ROM. This pin connects to the DOUT pin of the serial voice ROM. CSI CSI CSI Chip Select. These pins connect to CS pin of the serial register and the CS (CSI, CSI) pins of the serial voice ROM.	78	SADX	U	output leading addresses of read/write.
internal address counter of the serial register and serial voice ROM. This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. WE 0 Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. BE DROM I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. CST CSZ CSZ Dipin of the serial register and the CS (CST, CSZ) pins of the serial voice ROM.				This pin connects to TAS pin of serial register and serial voice ROM.
This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. WE 0 Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. BE DROM I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. CST CSS CSS CSS CSS CSS CSS CSS Dins of the serial voice ROM.	77	TAS	0	This pin is used to set serial addresses from the SADX and SADY pins into the
of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. DRAM. This pin outputs write data and inputs read data. Data ROM. This pin connects to the DOUT pin of the serial voice ROM. CSI CSI CSI Chip Select. These pins connect to CS pin of the serial register and the CS (CSI, CSS) pins of the serial voice ROM.				internal address counter of the serial register and serial voice ROM.
of the serial voice ROM. Clock pin to write serial addresses. This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register. WE Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. BE DROM Data ROM. This pin connects to the DOUT pin of the serial voice ROM. CS1 CS2 CS2 CS5 CS5 CS5 CS5 DROM Chip Select. These pins connect to CS pin of the serial register and the CS (CS1, CS3) pins of the serial voice ROM.	76	CAC		This pin connects to the SAS pin of the serial register and the SASX and SASY pins
serial voice ROM. Clock pin to read data from and write data into the serial register. Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode. Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data. BE DROM I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. CST CSS CSS CSS Chip Select. These pins connect to CS pin of the serial register and the CS (CST), CSS) pins of the serial voice ROM.	70	SAS	0	of the serial voice ROM. Clock pin to write serial addresses.
Serial voice ROM. Clock pin to read data from and write data into the serial register. This pin selects either read or write mode.	75	DWOV		This pin connects to the RWCK pin of the serial register and the RDCK pin of the
This pin selects either read or write mode. This pin selects either read or write mode.	75	RWCK	U	serial voice ROM. Clock pin to read data from and write data into the serial register.
This pin selects either read or write mode. This pin selects either read or write mode.	7.4	WE		Write Enable. This pin connects to the $\overline{\text{WE}}$ pin of the serial register and DRAM.
DRAM. This pin outputs write data and inputs read data. B5 DROM I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. B1 CS1 B2 CS2 B3 CS3 Chip Select. These pins connect to CS pin of the serial register and the CS (CS1, CS2, CS3) pins of the serial voice ROM.	74	WE	0	This pin selects either read or write mode.
B5 DROM I Data ROM. This pin outputs write data and inputs read data. 85 DROM I Data ROM. This pin connects to the DOUT pin of the serial voice ROM. 81 CS1 82 CS2 83 CS3 Chip Select. These pins connect to CS pin of the serial register and the CS (CS1, CS2, CS3) pins of the serial voice ROM.	70	D1/0		Data I/O. This pin connects to the DIN and DOUT pins of the serial register and
81 $\overline{\text{CS1}}$ 82 $\overline{\text{CS2}}$ 83 $\overline{\text{CS3}}$ 0 $\overline{\text{CS2}}$ Chip Select. These pins connect to $\overline{\text{CS}}$ pin of the serial register and the $\overline{\text{CS}}$ ($\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$) pins of the serial voice ROM.	/3	טו/ט	1/0	DRAM. This pin outputs write data and inputs read data.
81 $\overline{\text{CS1}}$ 82 $\overline{\text{CS2}}$ 83 $\overline{\text{CS3}}$ 0 $\overline{\text{CS2}}$ Chip Select. These pins connect to $\overline{\text{CS}}$ pin of the serial register and the $\overline{\text{CS}}$ ($\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$) pins of the serial voice ROM.	85	DROM	I	·
82 $\overline{CS2}$ $\overline{CS3}$ 0 Chip Select. These pins connect to \overline{CS} pin of the serial register and the \overline{CS} ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.				
83 $\overline{\text{CS3}}$ $\overline{\text{CS2}}, \overline{\text{CS3}}$) pins of the serial voice ROM.				Chip Select. These pins connect to \overline{CS} pin of the serial register and the \overline{CS} ($\overline{CS1}$).
			0	
	84	CS4		, , _F

Pin	Symbol	Туре			Descripti	on				
58	MSEL1	I	Those pine cold	at the conseit	, of the memor	, to be some	sated externally			
59	MSEL2	I	These pins seit	ect the capacity	or the memor	y to be conne	ected externally.			
			These pins sele	ct the number o	of and serial reg	isters to be co	nnected externallly.			
			MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity			
56	RSEL1	1	L	L	L	L	4M × 1			
57	RSEL2	i	L	L	L	Н	4M × 2			
		·	L	L	Н	L	4M × 3			
			L	L	Н	Н	$4M \times 4$			
			Mode Select	ion.						
34	MCUM	1	Low level : Star		l					
			High level : Mic							
						be initialized	and to go into the power			
62	RESET	I	down state.							
60	PDWN	1	state. Unlike th When a Low le is halted, and w	Power Down. When a low level is input, the MSM6789L goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789L to be reset. When a Low level is applied to this pin during recording operation, the MSM6789L is halted, and will be maintained in the power down state while PDWN is low level. After this pin is restored to a high level, postprocessing for recording will be performed.						
91	XT	I					d, input the clock through et to the ground level.			
92	XT	0					d, this pin must be left			
37 61	TEST TEST	İ	MSM6789L 1	est. Input a lo	w level to the 1	EST pin and a	high level to the \overline{TEST} pin.			
9-12	TMD3-TMD0									
13-20	TDT7-TDT0	1/0	MSM6789L Test. This pin must be left open.							
21	SYNC									
17-20	TDT3-TDT0	1/0	These pins mu	st be left open	as they are MS	SM6789L test	pins.			
22	TST									
23	TCK	I	MSM6789L 7	Fest. Input a lo	ow level signal	•				
8	TMD4									

Pin	Symbol	Туре						Desc	ription	
39	ROM	ı	operati	Playback Operation. When set to low, this pin selects the record/playback operation (only for the SBC method). When set to high, it selects the ROM playback operation (for the SBC and PCM methods).						
65	REC/PLAY	I	the RO	Recording mode or playback mode selection. This pin is invalid during the ROM playback operation. When set to low, it selects the playback mode. When set to high, it selects the recording mode.						
64	ST	ı	Start I	-				evel pı	ılse is applied to	this pin, the record/playback
63	SP	I	Stop I or ROM	-				vel pu	lse is applied to	this pin, the record/playback
32	PAUSE	I								o this pin, the record/playback
31	DEL	I	or spec through ch00 ch01 After po	or ROM operation is stopped temporarily. Phrase Delection. When a low level pulse is applied to this pin, all phrase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5, ch00:All phrase deletion ch01 to ch3F:Specified phrase deletion After power up, be sure to input a RESET signal and then delete all phrases. After completing this procedure, start the record/playback operation.					ng to the setting of pins CAO	
24-30	CAO-CA5	I	Desire	ed Pho of 63 p	rase s	Speci s can b	ficati be spec	on. cified in		the record/playback operation Remarks All phrase deletion A total of 63 phrases can be used for both record /playback and ROM playback operation.

Pin	Symbol	Туре			Descri	iption	
				•		of the following three ty n is invalid during the R0	•
				BR1	BR0	Bit rate	
35	BRO			L	L	16.0 kbps	_
36	BR1			L	Н	12.6 kbps	
				Н	L	10.0 kbps	
				Н	Н	Unused	
			Transition to	the Power	-down Sta	te.	
			Low level: 1	The MSM678	9L automati	cally goes to the power	-down state, except
		PDMD*1	when the record/playback operation is performed.				
	33 PDMD*1		High level: The MSM6789L automatically goes to the standby state, instead of t				
33			power-down state, except when the record/playback operation is performed. In this case, the MSM6789L can be placed in the				
				•			•
					-	-	WN pin to a high level.
						ed for the built-in LPF,	•
						lying a high level to the	
67-70	VD0-VD3	ı	elimination.	ie voice dete	ct level for th	ie voice triggered starti	ng and unvoiced-part
				the voice tria	nered starting	g or the unvoiced-part e	elimination
			Voice trigger	•	•	jh level to the VDS pin.	
			voice ingge	ou otal illig.		el with VD0 to VD3 pins	
38	VDS		Unvoiced-pa	rt elimination		level to the VDS pin. T	
			,		-	I with VD0 to VD3 pins	
			Note: When neither the voice triggered starting nor the unvoiced-part elimination is				
			used, input a Lo			•	•
72	MON	0	This pin outputs	a high level	while the re	cord/playback operation	on is being performed.
			Output to indica	te the enable	or disable s	state of the operation f	or specifying a
71	NAR	0	phrase. When o	continuous R	OM playbac	k is performed, the nex	xt phrase can
			be specified after	er the NAR pi	n goes to hi	gh positively.	

^{*1} When DRAM is selected, be sure to set the PDMD pin to a High level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V _{DD}	Ta=25°C	-0.3 to +7.0	V
Input voltage	V _{IN}	Ta=25°C	-0.3 to V _{DD} +0.3	V
Storage temperature	T _{STG}	_	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V _{DD}	DGND=AGND=0 V	+3.0 to +3.6	V
Operating temperature	T _{op}	_	0 to +70	°C
Master clock frequencuy	fosc	_	6.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6789L (3.3 V Version))

DC Characteristics

 $\mbox{DV}_{\mbox{DD}}\mbox{=}\mbox{AV}_{\mbox{DD}}\mbox{=}\mbox{3.0 to 3.6 V}$ $\mbox{DGND=AGND=0 V, Ta=0 to 70°C}$

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High input voltage	V _{IH}	_	0.85×V _{DD}	_	_	V
Low input voltage	V _{IL}	_	_	_	0.15×V _{DD}	V
High output voltage	V _{OH}	I_{OH} = $-40 \mu A$	V _{DD} -0.3	_	_	V
Low output voltage	V _{OL}	I _{OL} =2 mA	_	_	0.45	V
High input current *1	I _{IH1}	$V_{IH}=V_{DD}$	_	_	10	μΑ
High input current *2	I _{IH2}	V _{IH} =V _{DD}	_	_	20	μΑ
Low input currcent *1	I _{IL1}	V _{IL} =GND	-10	_	_	μΑ
Low input current *2	I _{IL2}	V _{IL} =GND	-20	_	_	μΑ
Low input current *3	I _{IL3}	V _{IL} =GND	-400	_	-20	μΑ
Operating current consumption	I _{DD}	f _{OSC} =8 MHz, no load	_	20	35	mA
		No load			10	
Power down current	I _{DDS1}	Serial register connected		_	10	μΑ
rower down cuffellt	1 .	No load		200	_	
	I _{DDS2}	DRAM connected				μΑ

^{*1} Applies to all inputs excluding the XT pin.

^{*2} Applies to the XT pin.

^{*3} Applies to the input pins with pull-up resistor (ST, SP, PAUSE, DEL) excluding the XT pin.

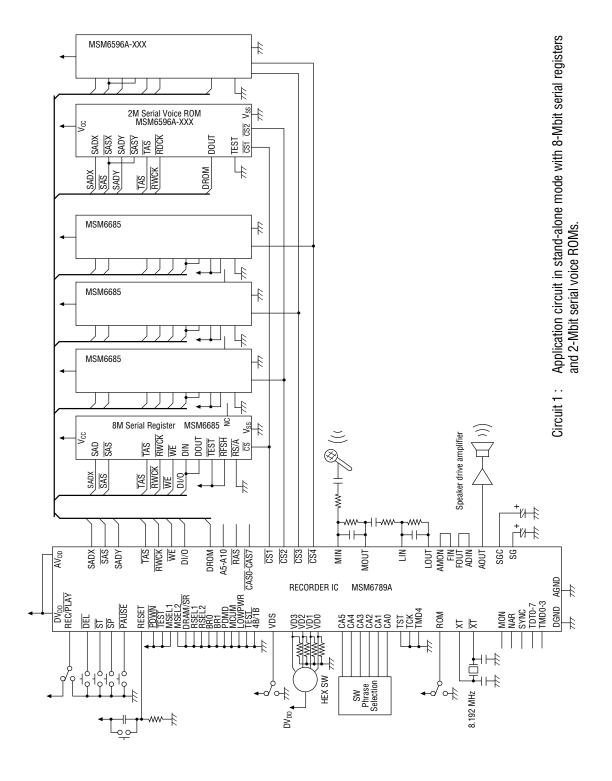
Analog Characteristics

DV_{DD}=AV_{DD}=3.0 to 3.6 V DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DA output relative error	$ V_{DAE} $	no load	_	_	20	mV
FIN admissible input voltage range	V_{FIN}	_	1	_	V _{DD} -1	V
FIN input impedance	R _{FIN}	_	1	_	_	MΩ
Op-map open loop gain	G _{OP}	f _{IN} =0 to 4kHz	40	_	_	dB
Op-amp input impedance	R _{INA}	_	1	_	_	$M\Omega$
Op-amp load resistance	R _{OUTA}	_	400	_	_	kΩ
AOUT load resistance	R _{AOUT}	_	100	_	_	kΩ
FOUT load resistance	R _{FOUT}	_	100	_	_	kΩ

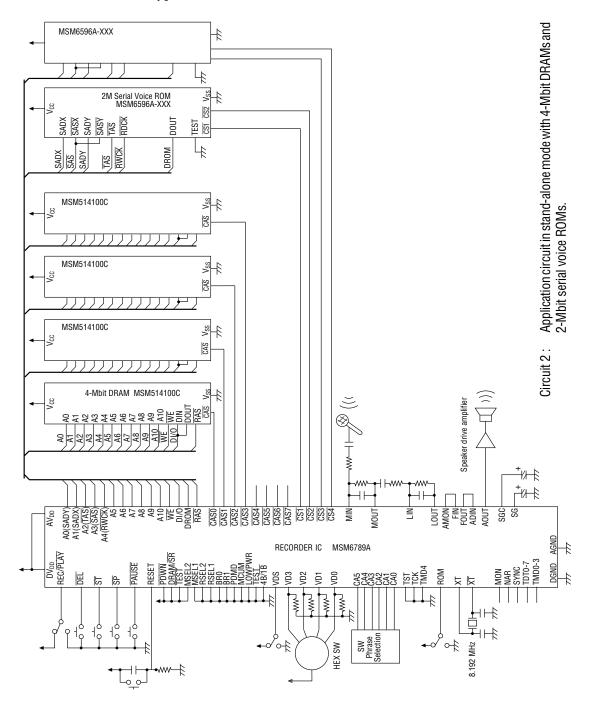
APPLICATION CIRCUITS (for MSM6789A (5 V version))

This is an application circuit example when the MSM6789A is used in stand-alone mode with four 8-Mbit serial registers and two 2-Mbit serial voice ROMs.



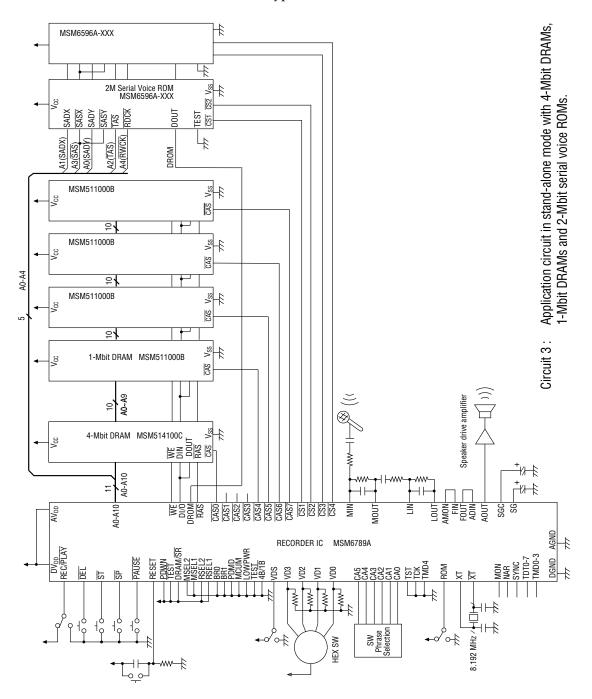
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with four 4-Mbit DRAMs (1-bit \times type) and two 2-Mbit serial voice ROMs.



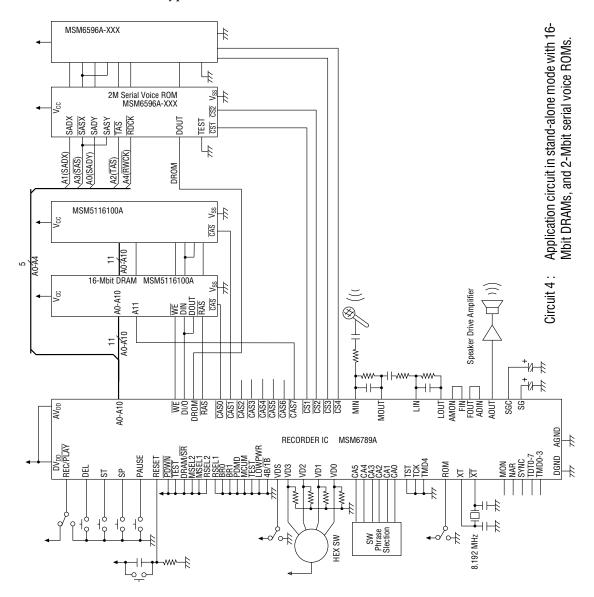
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



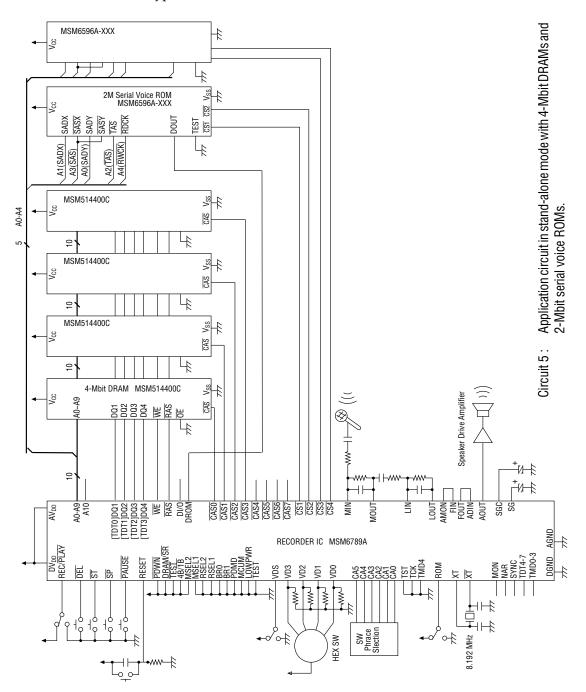
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with two 16-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



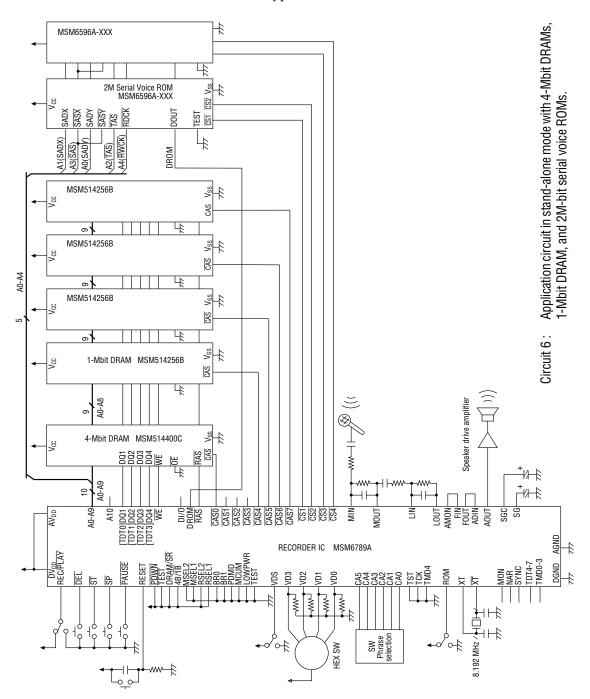
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with four 4-Mbit DRAMs (4-bit \times type) and two 2-Mbit serial voice ROMs.



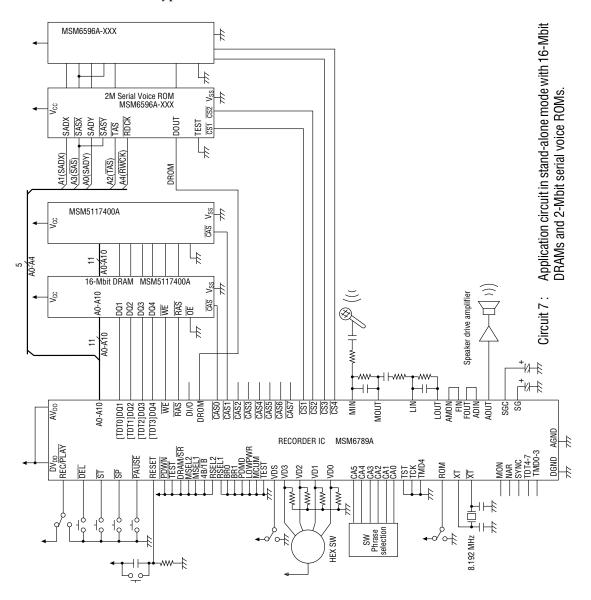
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (4-bit × type), and two 2-Mbit serial voice ROMs.



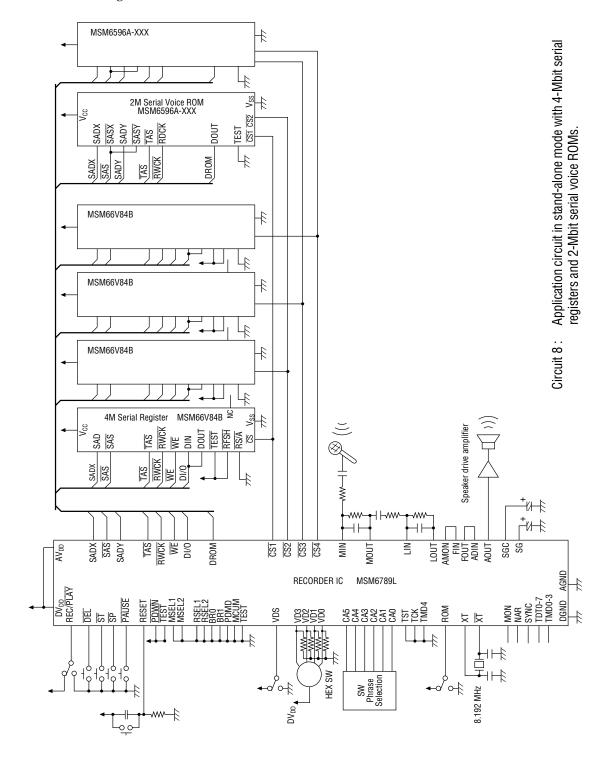
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with two 16-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



APPLICATION CIRCUITS (for MSM6789L (3.3 V Version))

This is an application circuit example when the MSM6789L is used in stand-alone mode with four 4-Mbit serial registers and two 2-Mbit serial voice ROMs.



MICROCONTROLLER INTERFACE MODE

FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in 12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter

Attenuation characteristics -40 dB/oct

• External memories

MSM6789A (5 V version)

General-purpose DRAM, 32 Mbits maximum (for variable messages)

1-Mbit DRAM : Can be directly driven (MSM514256B, MSM511000B)

4-Mbit DRAM: Can be directly driven (MSM514400C, MSM514100C)

16-Mbit DRAM: Can be directly driven (MSM5117400A, MSM5116100A)

ARAM, 32 Mbits maximum (for variable messages)

Note: Use the first 64 Kbits with no failed bits for the ARAM.

Serial register, 32 Mbits maximum (for variable messages)

4-Mbit serial register: Can be directly driven (MSM6684B)

8-Mbit serial register: Can be directly driven (MSM6685)

MSM6789L (3.3 V version)

Serial register, 16 Mbits maximum (for variable messages)

4-Mbit serial register: Can be directly driven (MSM66V84B)

MSM6789A (5 V version) and MSM6789L (3.3 V version)

Serial voice ROM, 4 Mbits maximum (for fixed messages)

1-Mbit serial voice ROM: Can be directly driven (MSM6595A)

2-Mbit serial voice ROM: Can be directly driven (MSM6596A)

3-Mbit serial voice ROM: Can be directly driven (MSM6597A)

• Bit rate

 $10.0,\,12.6,\,16.0$ kbps (at 8~kHz sampling freq.)

7.5, 9.5, 12.0 kbps (at 6 kHz sampling freq.)

• Maximum recording time (when one 8-Mbit serial register is connected)

13.8 minutes (for 10.0 kbps SBC)
11.0 minutes (for 12.6 kbps SBC)
14.6 minutes (for 9.5 kbps SBC)
14.6 minutes (for 9.5 kbps SBC)
11.5 minutes (for 12.0 kbps SBC)

Number of phrases

63 phrases for variable messages

255 phrases for fixed messages

- Standard linear PCM playback or OKI nonlinear PCM playback can be selected.
- Voice triggered starting function (voice detect level can be set)
- Uuvoiced-part elimination function (voice detect level can be set)
- · Pausing function

Master clock frequency:
 6.0 MHz to 8.192 MHz

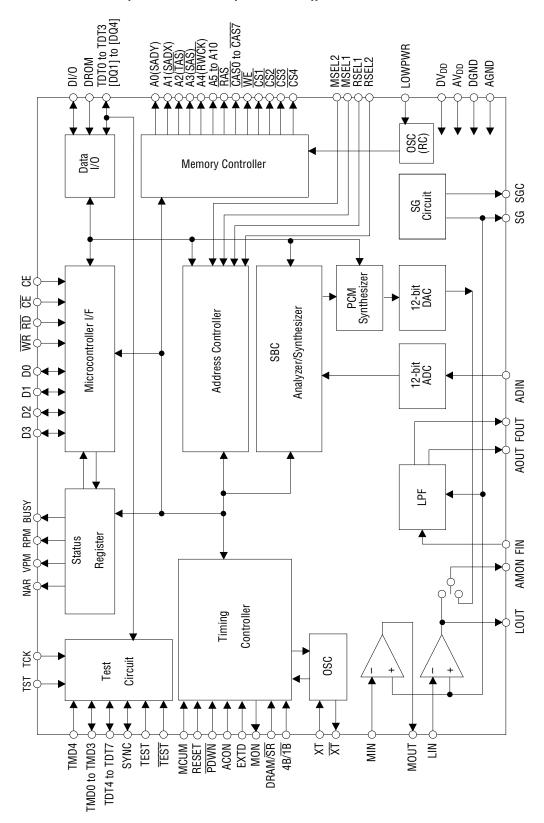
• Power supply voltage:

MSM6789A: Single 5 V power supply MSM6789L: Single 3.3 V power supply

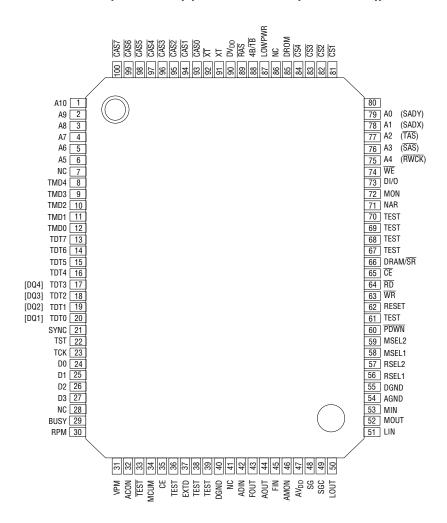
• Package options:

MSM6789A: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789AGS-BK) MSM6789L: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789LGS-BK)

BLOCK DIAGRAM (for MSM6789A (5 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789A (5 V Version))



100-Pin Plastic QFP

(): Pins for connecting serial voice ROM.[]: Pins for connecting 4-bit × type DRAM.

NC: No-connection pin

PIN DESCRIPTIONS (for MSM6789A (5 V Version))

Pin	Symbol	Туре	Description
90	DV		Digital power supply. Insert a bypass capacitor of 0.1µF or more between this
90	DV _{DD}		pin and the DGND pin.
47	۸۱/		Analog power supply. Insert a bypass capacitor of $0.1\mu F$ or more between this
47	AV _{DD}		pin and the AGND pin.
40, 55	DGND	_	Digital ground.
54	AGND	_	Analog ground.
48, 49	SG, SGC	0	Output for analog circuit reference voltage (signal ground).
53	MIN	I	Inverting input of the built-in OP amplifier. The non-inverting input pin is
51	LIN	'	internally connected to SG (signal ground).
52	MOUT	0	Output of the built-in OP amplifier for MIN and LIN.
50	LOUT		output of the bank in or unipliner for wint and Ent.
46	AMON	0	Connected to the LOUT pin in the recording mode and to the DA converter
	AUVION	0	output in the playback mode. This pin connects the built-in LPF input (FIN pin).
45	FIN	I	Input of the built-in LPF.
43	FOUT	0	Output of the built-in LPF. This pin connects the AD converter input (ADIN pin).
42	ADIN	I	Input of the built-in 12-bit AD converter.
44	AOUT	0	Output of the built-in LPF. This pin outputs playback waveforms and connects
	7.001		an external speaker drive amplifier.
			This pin selects whether memory to be connected externally is DRAM or serial
66	DRAM/SR	1	register.
			Low level : Serial register
			High level : DRAM
			This pin selects either 1-bit \times type DRAM or 4-bit \times type DRAM.
88	4B/1B	I	Low level : 1-bit × type
			High level : 4-bit × type
79	A0 (SADY)		These pins connect to A0 and A1 of DRAM at the time of DRAM selection. They also
78	A1 (SADX)	0	connect to SAD pin of serial register and serial voice ROM at the time of serial
	,		register selection. These pins output leading addresses of read/write.
			This pin connects to A2 of DRAM at the time of DRAM selection. It also connects
77	A2 (TAS)	0	to TAS pin of serial register and serial voice ROM at the time of serial register selection.
	, ,		This pin is used to set serial addresses from the SADX and SADY pins into the
			internal address counter of the serial register and serial voice ROM.
70	40 (040)	•	This pin connects to A3 of DRAM at the time of DRAM selection. It also connects
76	A3 (SAS)	0	to the SAS pin of the serial register and the SASX and SASY pins of the serial voice
			ROM at the time of serial register selection. Clock pin to write serial addresses.
			This pin connects to A4 of DRAM at the time of DRAM selection. It also connects
75	A4 (RWCK)	0	to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM at
			the time of serial register selection. Clock pin to read data from and write data into
			the serial register.
1-6	A10-A5	0	These pins connect to pins A5-A10 of DRAM at the time of DRAM selection.
			These pins output addresses of read/write.

Pin	Symbol	Туре	Description							
74	WE		Write Enable.	This pin conn	ects to the WE	pin of the seri	al register and DRAM.			
74	WE	0	This pin selects	either read or v	write mode.					
73	DI/O	1/0		Data I/O. This pin connects to the DIN and DOUT pins of the serial register and						
	2224		-	DRAM. This pin is used to output write data and inputs read data. Data ROM. This pin connects to the DOUT pin of the serial voice ROM.						
85	DROM			•		•				
89	RAS	0	This is a row add							
93-100	CASO- CAS7	0		ss output pin,	•		ime of DRAM selection. RAM at the time of 16-			
81	CS1									
82	CS2	0	Chip Slect. Th	ese pins conne	ect CS pin of the	ne serial registo	er and the $\overline{\text{CS}}$ ($\overline{\text{CS1}}$,			
83	CS3	0	$\overline{\text{CS2}}, \overline{\text{CS3}})$ pins (of the serial vo	ice ROM.					
84	CS4									
58 59	MSEL1 MSEL2	l I	These pins selec	These pins select the capacity of the memory to be connected externally.						
			externallly. • When DRAN MSEL2	l is selected (D	RAM/SR = Hig	h level)	Memory capacity			
			L	L	L	L	1M × 4			
			L	L	L	Н	4M × 1			
			L	L	Н	L	1M × 8			
			L	L	Н	Н	$1M \times 4 + 4M \times 1$			
			L	Н	L	L	4M × 2			
56	RSEL1		L	Н	L	Н	4M × 2			
57	RSEL2	;	L	Н	Н	L	4M × 3			
01	HOLLE	'	L	Н	Н	Н	4M × 3			
			Н	L	L	L	4M × 4			
			Н	L	L	Н	16M×1			
			Н	L	Н	L	4M × 6			
			Н	L	Н	Н	4M × 6			
			Н	Н	L	L	4M × 8			
			Н	Н	L	Н	4M × 8			
			Н	Н	Н	L	16M × 2			
			Н	Н	Н	Н	16M × 2			

Pin	Symbol	Туре			Descrip	tion					
			• When serial	register is sele	cted (DRAM/S	\overline{R} = Low level)					
			MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity				
			L	L	L	L	4M×1				
			L	L	L	Н	4M × 2				
56	RSEL1	ı	L	L	Н	L	4M × 3				
57	RSEL2	' 	L	L	Н	Н	4M × 4				
31	HOLLZ	'	L	Н	L	L	8M × 1				
			L	Н	L	Н	8M × 2				
			L	Н	Н	L	8M × 3				
			L	Н	Н	Н	8M × 4				
87	LOWPWR	I	This pin selects power down wh Low level : 15 µ: High level : 125	en DRAM is se s max.	•	iod of DRAM a	at the time of				
				Mode Selection.							
34	MCUM	I	Low level : Stan	d-alone mode							
			_	ligh level : Microcontroller interface mode							
62	RESET	ı		A high input level causes the MSM6789A to be initialized and to go into the pow							
			down state.								
60	PDWN	I	state. Unlike the I When an Low le is halted, and wil	RESET pin, this vel is applied to I be maintained	pin does not fo this pin durin in the power d	rce the MSM6 g recording op own state whil	es to the power down 789A to be reset. Peration, the MSM6789A e PDWN is low level.				
24	D0										
25	D1	1/0	Bidirectional dat	a bus to trans	fer commands	and data to a	nd from an external				
26	D2	1/0	microcontroller.								
27	D3										
63	WR	ı		-	g a low pulse t	o WR pin caus	ses a command or data				
64	RD	I	Read Pulse In	to be input via D0 to D3 pins. Read Pulse Input. Inputting a low pulse to RD pin causes status bits or data to							
			be output via DO		ho CE nin io co	t to low lovel	and the CE pin is set to a				
65 35	CE CE	I	high level, the w When the CE pir	rite pulse (WF n is set to a hig pulse (RD) can	R) or read pulso th level or CE p	e (RD) can be oin is set to a l	and the CE pin is set to a accepted. ow level, the write pulse cannot be communicate				

Pin	Symbol	Туре	Description				
29	BUSY	0	Busy. This pin outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0 to D3 pins. The state of this pin is the same as the contents of the BUSY bit of the status register.				
30	RPM	0	RPM. This pin outputs a high level during recording or playback operation. The state of this pin is the same as the contents of the RPM bit of the status register.				
31	VPM	0	VPM. This pin outputs a high level during standby for voice incoming after the st recording by voice triggered starting or unvoiced-part elimination. Also outputs a level when the record/playback is stopped temporarily by inputting the PAUSE command. The state of this pin is the same as the contents of the VPM bit of the status register.				
71	NAR	0	NAR. This NAR pin indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after verifying that the NAR pin is at high level and input the START command.				
32	ACON	I	Pop Noise Suppression Select. This pin selects whether the pop noise suppression circuit is used. Low level: the pop noise suppression circuit is not used. High level: the pop noise suppression circuit is used. The DC level is shifted by the LEV command.				
37	EXTD	I	EXTD. In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.				
91	XT	I	Oscillator Connect. When an external clock is used, input the clock through this pin. At the power-down state, this pin must be set to the ground level.				
92	ΧT	0	Oscillator Connect. When an external clock is uesd, this pin must be left open.				
72	MON	0	MON. This pin outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.				
36, 37-39, 61, 67-70 33	TEST TEST	I	MSM6789A Test. Input a low level to the TEST pin and a high level to the TEST pin.				
9-12 13-20 21	TMD3-TMD0 TDT7-TDT0 SYNC	1/0	MSM6789A Test. This pin must be left open.				
17-20	TDT3-TDT0 [DQ4]-[DQ1]	1/0	Connect these pins to DQ1 to DQ4 of DRAM at the time of 4-bit × type DRAM selection. Otherwise these pins must be left open as they are MSM6789A test pins.				
22 23 8	TST TCK TMD4	I	MSM6789A Test. Input a low level.				

ABSOLUTE MAXIMUM RATINGS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V _{DD}	Ta=25°C	-0.3 to +7.0	V
Input Voltage	V _{IN}	Ta=25°C	-0.3 ~ V _{DD} +0.3	V
Storage temperature	T _{STG}	_	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V _{DD}	DGND=AGND=0 V	+3.5 to +5.5*3	V
Operating temperature	T _{op}	_	0 to +70	°C
Master clock frequencuy	f _{OSC}	_	6.0 to 8.192	MHz

ELECTRIAL CHARACTERISTICS (for MSM6789A (5 V Version))

DC Characteristics

 $\ensuremath{\mathsf{DV_{DD}}}\xspace = 4.5 \text{ to } 5.5 \ensuremath{\:\mathsf{V^{*3}}}\xspace$ DGND=AGND=0 V $\ensuremath{\:\mathsf{Ta=0}}\xspace$ to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High input voltage	V _{IH}	_	0.8×V _{DD}	_	_	V
Low input voltage	V _{IL}	_	_	_	$0.2 \times V_{DD}$	V
High output voltage	V _{OH}	Ι _{ΟΗ} =–40 μΑ	V _{DD} -0.3	_	_	V
Low output voltage	V _{OL}	I _{OL} =2 mA	_	_	0.45	V
High input current*1	I _{IH1}	V _{IH} =V _{DD}	_	_	10	μΑ
High input current*2	I _{IH2}	V _{IH} =V _{DD}	_	_	20	μΑ
Low input current*1	I _{IL1}	V _{IL} =GND	-10	_	_	μΑ
Low input current*2	I _{IL2}	V _{IL} =GND	-20	_	_	μΑ
Operating current consumption	I _{DD}	f _{OSC} =8 MHz, no load	_	20	35	mA
Power down current	I _{DDS1}	No load		_	10	μΑ
		Serial register connected	_			
	I _{DDS2}	No load		200	_	μА
		DRAM connected				

^{*1} Applies to all inputs excluding the XT pin.

^{*2} Applies to the XT pin.

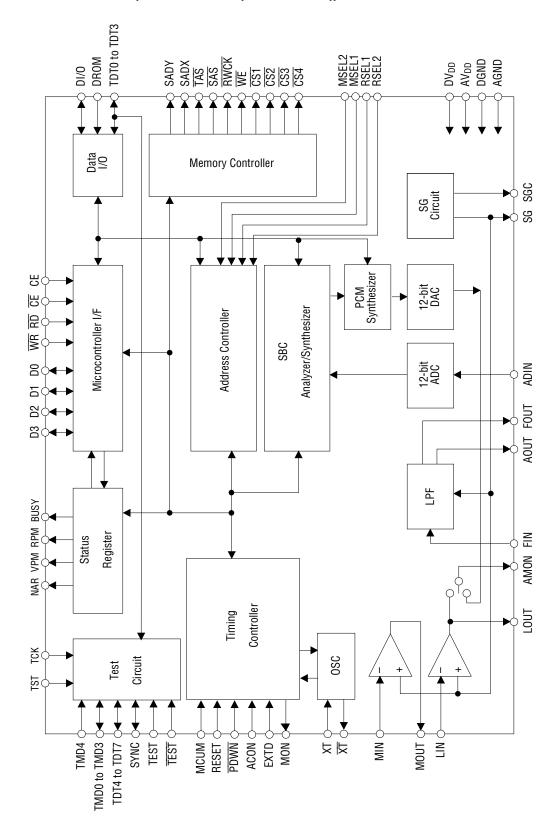
^{*3} The record/playback operation must be performed at the power supply voltage of 4.5 to 5.5 V. The MSM6789A operates at 3.5 to 5.5 V when the serial register is backed up.

Analog Characteristics

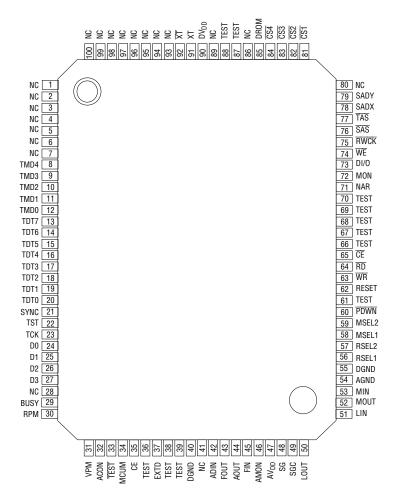
DV_{DD}=AV_{DD}=4.5 to 5.5 V DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DA output relative error	V _{DAE}	No load	_	_	10	mV
FIN admissible input voltage range	V_{FIN}	_	1	_	V _{DD} -1	V
FIN input impedance	R _{FIN}	_	1	_		MΩ
OP-amp open loop gain	G _{OP}	f _{IN} =0 to 4 kHz	40	_		dB
OP-amp input impedance	R _{INA}	_	1	_	_	MΩ
OP-amp load resistance	R _{OUTA}	_	200	_	_	kΩ
AOUT load resistance	R _{AOUT}	_	50	_	_	kΩ
FOUT load resistance	R _{FOUT}	_	50	_	_	kΩ

BLOCK DIAGRAM (for MSM6789L (3.3 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789L (3.3V Version))



100-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version))

Pin	Symbol	Туре	Description
90	DV _{DD}	_	Digital power supply. Insert a bypass capacitor of $0.1\mu F$ or more between this pin and the DGND pin.
47	AV _{DD}	_	Analog power supply. Insert a bypass capacitor of $0.1\mu F$ or more between this pin and the AGND pin.
40, 55	DGND	_	Digital ground.
54	AGND	_	Analog ground.
48, 49	SG, SGC	0	Output for analog circuit reference voltage (signal ground).
53	MIN		Inverting input of the built-in OP amplifier. The non-inverting input pin is
51	LIN	l	internally connected to SG (signal ground).
52 50	MOUT LOUT	0	Output of the built-in OP amplifier for MIN and LIN.
46	AMON	0	Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. This pin connects the built-in LPF input (FIN pin).
45	FIN	I	Input of the built-in LPF.
43	FOUT	0	Output of the built-in LPF. This pin connects the AD converter input (ADIN pin).
42	ADIN	I	Input of the built-in 12-bit AD converter.
44	AOUT	0	Output of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier.
79 78	SADY SADX	0	These pins connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write.
77	TAS	0	This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	SAS	0	This pin connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM. Clock pin to write serial addresses.
75	RWCK	0	This pin connects to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM. Clock pin to read data from and write data into the serial register.
74	WE	0	Write Enable. This pin connects to the WE pin of the serial register and DRAM. This pin selects either read or write mode.
73	DI/O	1/0	Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin is used to output write data and inputs read data.
85	DROM	ı	Data ROM. This pin connects to the DOUT pin of the serial voice ROM.
81	CS1		
82	CS2		Chip Slect. These pins connect $\overline{\text{CS}}$ pin of the serial register and the $\overline{\text{CS}}$ ($\overline{\text{CS1}}$,
83	CS3	0	CS2, CS3) pins of the serial voice ROM.
84	CS4		
58	MSEL1	I	The same of the sa
59	MSEL2	I	These pins select the capacity of the memory to be connected externally.

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

Pin	Symbol	Туре			Descri	ption	
			These pins se externallly.	lect the numb	er of serial reg	isters to be co	onnected
56	RSEL1	1	MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity
57	RSEL2	i	L	L	L	L	4M ×1
0.	110222		L	L	L	Н	4M × 2
			L	L	Н	L	4M × 3
			L	L	Н	Н	4M × 4
			Mode Selecti				
34	MCUM	I	Low level : Stan				
62	RESET	I	High level : Mic A high input lev down state.			be initialized	and to go into the power
60	PDWN	I	state. Unlike the When an Low le is halted, and wi	RESET pin, this vel is applied t Il be maintaine	s pin does not to this pin dur d in the power	force the MSN ing recording down state w	poes to the power down 16789L to be reset. operation, the MSM6789L hile PDWN is low level. for recording will be
24	D0						
25	D1	1.00	Bidirectional da	ta bus to trans	sfer command	ls and data to	and from an external
26	D2	1/0	microcontroller				
27	D3						
63	WR	I	Write Pulse Into be input via [-	ig a low pulse	to WR pin ca	uses a command or data
64	RD	I	Read Pulse II be output via Do	-	ig a low pulse	to RD pin ca	uses status bits or data to
65 35	CE CE	I	high level, the w	vrite pulse (Win is set to a hin pulse (RD) can	R) or read pul	se (RD) can be pin is set to	el and the CE pin is set to a be accepted. a low level, the write pulse ata cannot be communicated
29	BUSY	0	•	, do not apply	any data to D	0 to D3 pins.	being executed. When this The state of this pin is the ter.
30	RPM	0			ū	· ·	playback operation. The bit of the status register.

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

Pin	Symbol	Туре	Description
31	VPM	0	VPM. This pin outputs a high level during standby for voice incoming after the start of recording by voice triggered starting or unvoiced-part elimination. Also outputs a high level when the record/playback is stopped temporarily by inputting the PAUSE command. The state of this pin is the same as the contents of the VPM bit of the status register.
71	NAR	0	NAR. This NAR pin indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after verifying that the NAR pin is at high level and input the START command.
32	ACON	I	Pop Noise Suppression Select. This pin selects whether the pop noise suppression circuit is used. Low level: the pop noise suppression circuit is not used. High level: the pop noise suppression circuit is used. The DC level is shifted by the LEV command.
37	EXTD	I	EXTD. In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.
91	XT	I	Oscillator Connect. When an external clock is used, input the clock through this pin. At the power-down state, this pin must be set to the ground level.
92	XT	0	Oscillator Connect. When an external clock is uesd, this pin must be left open.
72	MON	0	MON. This pin outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
36, 37-39, 61, 67-70 33	TEST TEST	I	MSM6789L Test. Input a low level to the TEST pin and a high level to the TEST pin.
9-12	TMD3-TMD0		
13-20	TDT7-TDT0	I/O	MSM6789L Test. This pin must be left open.
21	SYNC		
17-20	TDT3-TDT0	I/O	These pins must be left open as they are MSM6789L test pins.
22	TST		
23	TCK	ı	MSM6789L Test. Input a low level.
8	TMD4		

ABSOLUTE MAXIMUM RATINGS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V _{DD}	Ta=25°C	-0.3 to +7.0	V
Input Voltage	V _{IN}	Ta=25°C	-0.3 ~ V _{DD} +0.3	V
Storage temperature	T _{STG}	_	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V _{DD}	DGND=AGND=0 V	+3.0 to +3.6	V
Operating temperature	T _{op}	_	0 to +70	°C
Master clock frequencuy	f _{OSC}	_	6.0 to 8.192	MHz

ELECTRIAL CHARACTERISTICS (for MSM6789L (3.3 V Version))

DC Characteristics

 $\ensuremath{\mathsf{DV_{DD}}}\xspace = AV_{DD}\xspace = 3.0$ to 3.6 V DGND=AGND=0 V $\ensuremath{\mathsf{Ta=0}}\xspace$ to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High input voltage	V _{IH}	_	0.85×V _{DD}	_	_	V
Low input voltage	V _{IL}	_	_	_	0.15×V _{DD}	V
High output voltage	V _{OH}	Ι _{ΟΗ} =-40 μΑ	V _{DD} -0.3	_	_	V
Low output voltage	V_{OL}	I _{OL} =2 mA	_	_	0.45	V
High input current*1	I _{IH1}	V _{IH} =V _{DD}	_	_	10	μΑ
High input current*2	I _{IH2}	$V_{IH}=V_{DD}$	_	_	20	μΑ
Low input current*1	I _{IL1}	V _{IL} =GND	-10	_	_	μΑ
Low input current*2	I _{IL2}	V _{IL} =GND	-20	_	_	μΑ
Operating current consumption	I _{DD}	f _{OSC} =8 MHz, no load	_	20	35	mA
Power down current	I _{DDS1}	No load Serial register connected	_	_	10	μА
	I _{DDS2}	No load DRAM connected	_	200	_	μА

^{*1} Applies to all inputs excluding the XT pin.

^{*2} Applies to the XT pin.

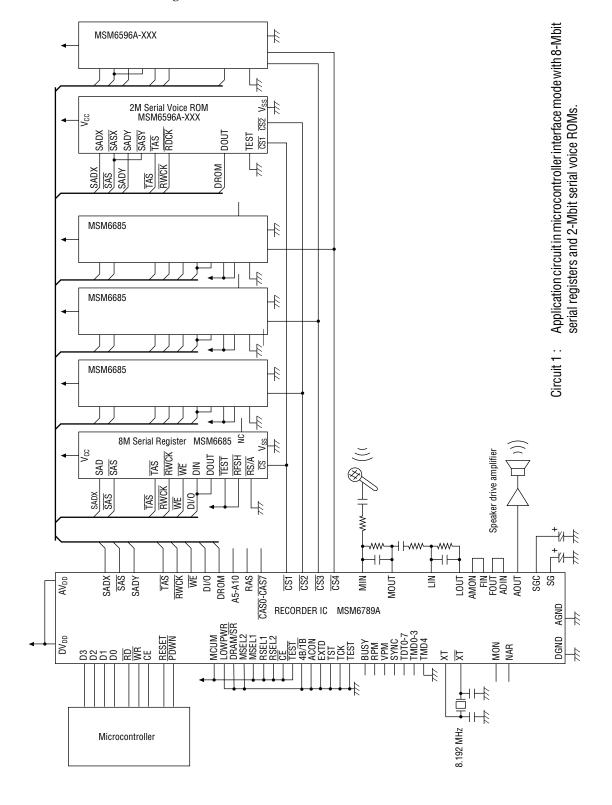
Analog Characteristics

DV_{DD}=AV_{DD}=3.0 to 3.6 V DGND=AGND=0 V Ta=0 to 70°C

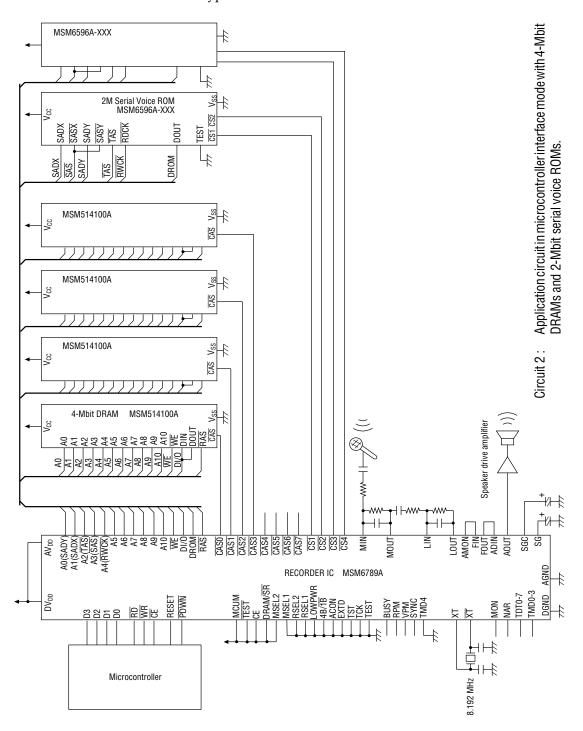
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DA output relative error	V _{DAE}	No load	_	_	20	mV
FIN admissible input voltage range	V_{FIN}	_	1	_	V _{DD} -1	V
FIN input impedance	R _{FIN}	_	1	_	_	MΩ
OP-amp open loop gain	G _{OP}	f _{IN} =0 to 4 kHz	40	_		dB
OP-amp input impedance	R _{INA}	_	1	_	_	MΩ
OP-amp load resistance	R _{OUTA}	_	400	_	_	kΩ
AOUT load resistance	R _{AOUT}	_	100	_	_	kΩ
FOUT load resistance	R _{FOUT}	_	100	_	_	kΩ

APPLICATION CIRCUITS (for MSM6789A (5 V Version))

This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 8-Mbit serial registers and two 2-Mbit serial voice ROMs.

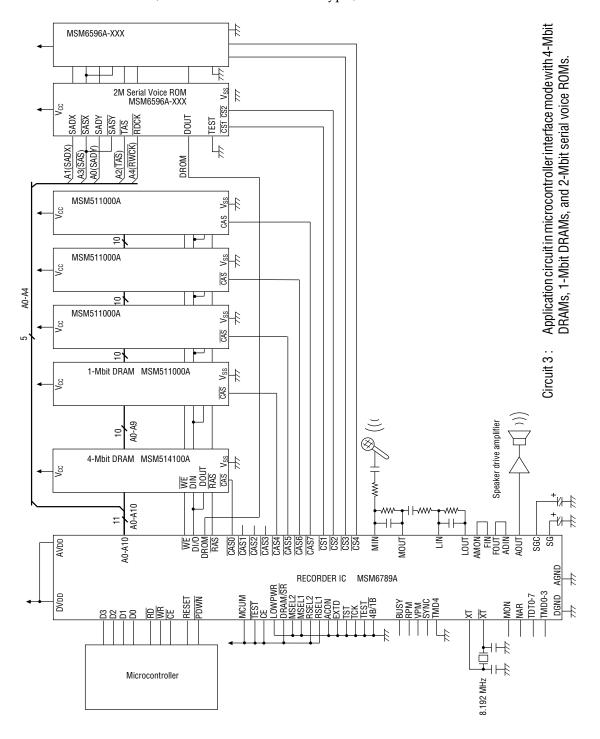


This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 4-Mbit DRAMs (1-bit \times type) and two 2-Mbit serial voice ROMs.

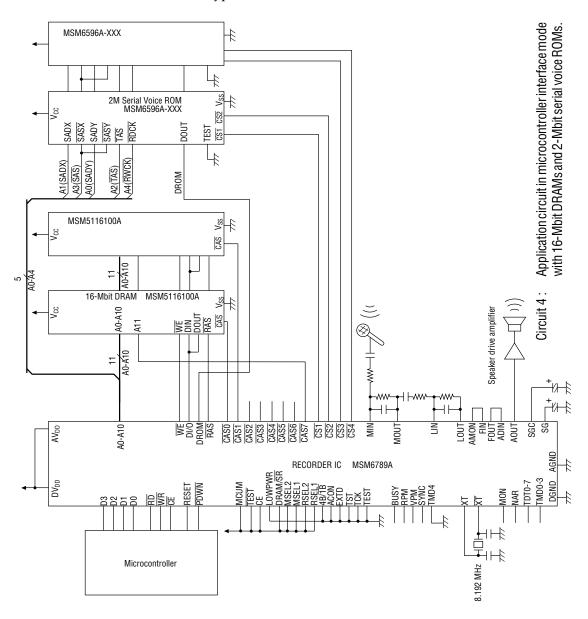


APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

This is an application circuit example when the MSM6789A is used in microcontroller interface mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (1-bit \times type), and two 2-Mbit serial voice ROMs.

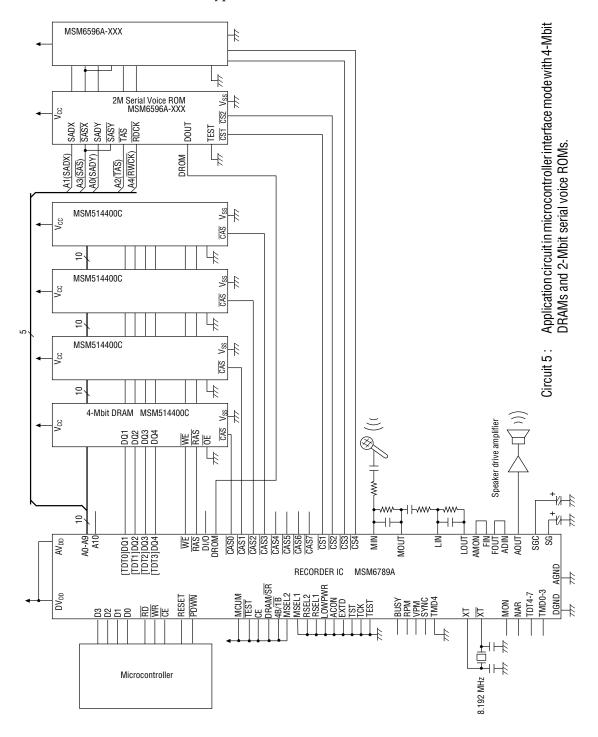


This is an application circuit example when the MSM6789A is used in microcontroller interface mode with two 16-Mbit DRAMs (1-bit \times type) and two 2-Mbit serial voice ROMs.

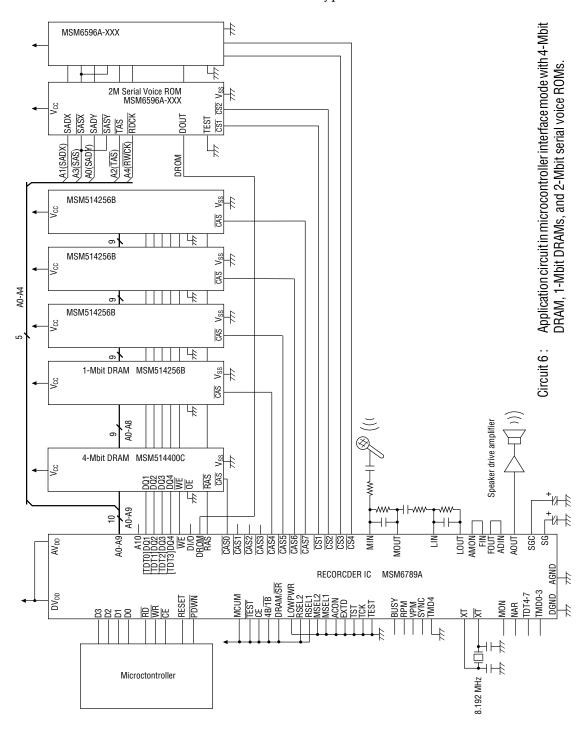


APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

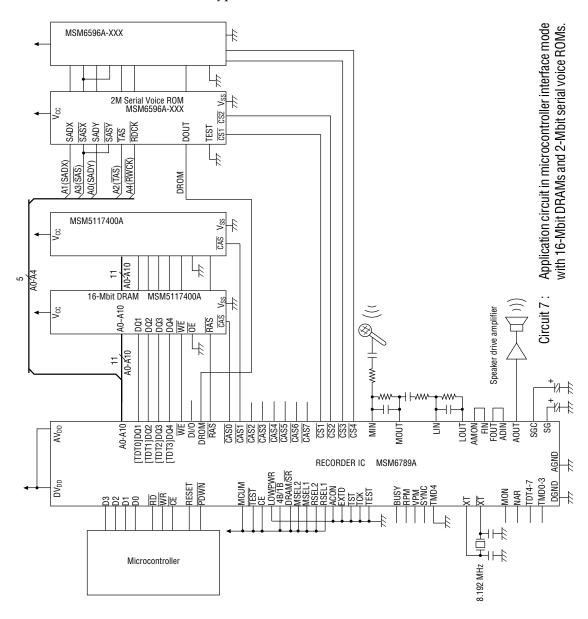
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 4-Mbit DRAMs (4-bit \times type) and two 2-Mbit serial voice ROMs.



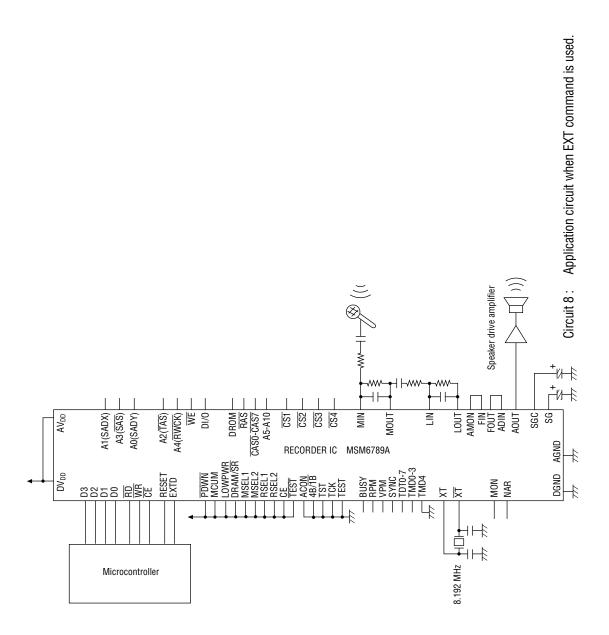
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (4-bit \times type), and two 2-Mbit serial voice ROMs.



This is an application circuit example when the MSM6789A is used in microcontroller interface mode with two 16-Mbit DRAMs (4-bit \times type) and two 2-Mbit serial voice ROMs.



This is an application circuit example when the EXT command is used for recording/playback.



APPLICATION CIRCUITS (for MSM6789L (3.3 V Version))

This is an application circuit example when the MSM6789L is used in microcontroller interface mode with four 4-Mbit serial registers and two 2-Mbit serial voice ROMs.

