PROGRAMMABLE CLOCK GENERATOR

IDT5V925

FEATURES:

- **3V to 3.6V operating voltage**
- **3.125 MHz to 160MHz output frequency range**
- **4 programmable frequency outputs**
- **Input from fundamental crystal oscillator or external source**
- **Balanced Drive Outputs ±12mA**
- **PLL disable mode for low frequency testing**
- **Select inputs ($S_{[1:0]}$) for divide selection (multiply ratio of 2, 3, 4, 5, 6, 7, and 8)**
- **5V tolerant inputs**
- **Low output skew/jitter**
- **External PLL feedback, internal loop filter**
- **Available in 16-pin QSOP package**

APPLICATIONS:

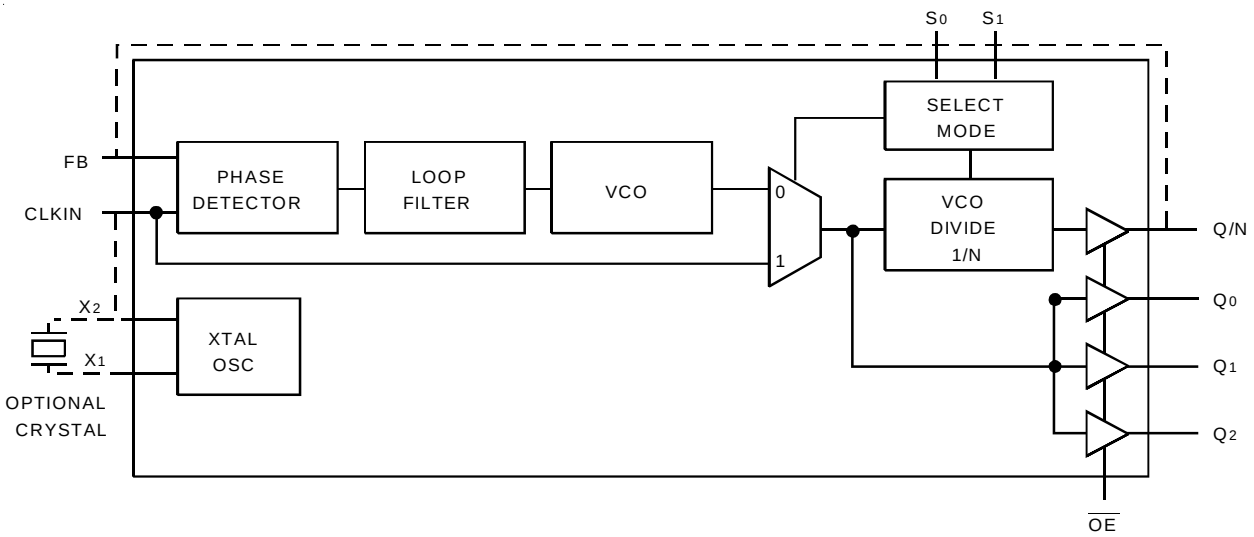
- **Ethernet/fast ethernet**
- **Router**
- **Network switches**
- **SAN**
- **Instrumentation**

DESCRIPTION:

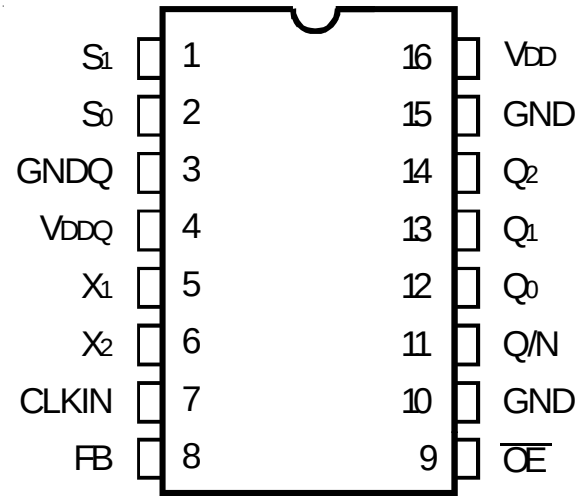
The IDT5V925 is a high-performance, low skew, low jitter phase-locked loop (PLL) clock driver. It provides precise phase and frequency alignment of its clock outputs to an externally applied clock input or internal crystal oscillator. The IDT5V925 has been specially designed to interface with Gigabit Ethernet and Fast Ethernet applications by providing a 125MHz clock from 25MHz input. It can also be programmed to provide output frequencies ranging from 3.125MHz to 160MHz with input frequencies ranging from 3.125MHz to 80MHz.

The IDT5V925 includes an internal RC filter that provides excellent jitter characteristics and eliminates the need for external components. When using the optional crystal input, the chip accepts a 10-30MHz fundamental mode crystal with a maximum equivalent series resistance of 50Ω. The on-chip crystal oscillator includes the feedback resistor and crystal capacitors (nominal load capacitance is 15pF).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM	Supply Voltage to Ground	–0.5 to +7	V
	DC Output Voltage VOUT	–0.5 to VCC +0.5	V
	DC Input Voltage VIN	–0.5 to +7	V
TA = 85°C	Maximum Power Dissipation	.55	W
TSTG	Storage Temperature	–65 to +150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CRYSTAL SPECIFICATION

The crystal oscillators should be fundamental mode quartz crystals: overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance.

PIN DESCRIPTION

Pin Names	I/O	Description
CLKIN	I	Input clock
X1(1)	I	Crystal oscillator input. Connected to GND if oscillator not required.
X2 (1)	O	Crystal oscillator output. Leave unconnected for clock input.
FB	I	PLL feedback input which should be connected to Q/N output pin only. PLL locks onto positive edge of FB signal.
S[1:0]	I	Three level divider/mode select pins. Float to MID.
Q[2:0]	O	Output at N*CLKIN frequency
Q/N	O	Programmable divide-by-N clock output
$\overline{OE}$	I	Tri-state output enable. When asserted HIGH, clock outputs are high impedance.
VDD	PWR	Power supply for output buffers
GND	PWR	Ground supply for output buffers
VDDQ	PWR	Power supply for PLL
GNDQ	PWR	Ground supply for PLL

NOTE:
1. For best accuracy, use parallel resonant crystal specified for a load capacitance of 15pF.

FUNCTION TABLE

Output Used for	Allowable CLKIN Range (MHz)(1,2)		Output Frequency Relationships	
Feedback	Minimum	Maximum	Q/N	Q[2:0]
Q/N	25/N	160/N	CLKIN	CLKIN x N

NOTES:
1. Operation in the specified CLKIN frequency range guarantees that the VCO will operate in the optimal range of 25MHz to 160MHz. Operation with CLKIN outside specified frequency ranges may result in invalid or out-of-lock outputs.
2. Q[2:0] is not allowed to be used as feedback.

DIVIDE SELECTION TABLE (1)

S1	S0	Divide-by-N Value	Mode
L	L	FACTORY TEST (2)	
L	M	2	PLL
L	H	3	PLL
M	L	4	PLL
M	M	5(3)	PLL
M	H	6	PLL
H	L	7	PLL
H	M	8	PLL
H	H	16	TEST(4)

NOTES:
1. H = HIGH
   M = MEDIUM
   L = LOW
2. Factory Test Mode: operation not specified,
3. Ethernet mode (use a 25MHz input frequency and Q/N as feedback).
4. Test mode for low frequency testing. In this mode, CLKIN bypasses the VCO (VCO powered down). Frequency must be > 1MHz due to dynamic circuits in the frequency dividers. $Q_{[2:0]}$ outputs are divided by 2 in test mode.

OPERATING CONDITIONS

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}/V_{DDQ}	Power Supply Voltage	3	3.3	3.6	V
T_A	Operating Temperature	–40	+25	+85	°C
C_L	Output Load Capacitance	—	—	15	pF
C_{IN}	Input Capacitance, CLKIN, FB, $\overline{OE}$, F = 1MHz, V_{IN} = 0V, T_A = 25°C	—	5	7	pF

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions		Min.	Typ.(7)	Max	Unit
V_{IL}	Input LOW Voltage			—	—	0.8	V
V_{IH}	Input HIGH Voltage			2	—	—	V
V_{IHH}(1)	Input HIGH Voltage	3-level input only		V_{DD} - 0.6	—	—	V
V_{IMM}(1)	Input MID Voltage	3-level input only		V_{DD}/2 - 0.3	—	V_{DD}/2 + 0.3	V
V_{ILL}(1)	Input LOW Voltage	3-level input only		—	—	0.6	V
I_{IN}	Input Leakage Current (CLKIN, FB Inputs only)	V_{IN} = V_{DD} or GND, V_{DD} = Max		- 5	—	+5	µA
I_3	3-Level Input DC Current, $S_{[1:0]}$	V_{IN} = V_{DD}	HIGH Level	—	—	+200	µA
		V_{IN} = V_{DD}/2	MID Level	- 50	—	+50	
		V_{IN} = GND	LOW Level	- 200	—	—	
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		- 5	0.07	+5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 12mA		—	0.15	0.55	V
V_{OH}	Output HIGH Voltage	I_{OH} = -12mA		2.4	2.8	—	V

NOTE:
1. These inputs are normally wired to V_{CC}, GND, or unconnected. If the inputs are switched in real time, the function and timing of the outputs may glitch, and the PLL may require an additional lock time before all the datasheet limits are achieved.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min.	Typ.	Max	Unit
I_{DDQ}	Quiescent Supply Current	V_{DD} = Max. CLKIN = FB = X_1 = GND $S_{[1:0]}$ = HH $\overline{OE}$ = H All outputs unloaded	—	0.7	2	mA
ΔI_{DD}	Supply Current per Input	V_{DD} = Max., V_{IN} = 3V	—	1	30	µA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.6V $S_{[1:0]}$ =LM $\overline{OE}$ = GND F_{OUT} = 60MHz All outputs unloaded	—	77	130	mA

NOTE:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_R, t_F	Rise Time, Fall Time (1)	0.8V to 2V	—	0.7	1.5	ns
d_T	Output/Duty Cycle (1)	V_T = V_{DD}/2	45	—	55	%
t_{PD}	CLKIN to FB (1)	V_T = V_{DD}/2	-300	—	300	ps
t_{SK}	Output to Output Skew (1)	V_T = V_{DD}/2; $Q_{[2:0]}$	—	—	100	ps
		V_T = V_{DD}/2; Q/N - $Q_{[2:0]}$	—	—	300	
t_J	Cycle - Cycle Jitter (1)		—	—	200	ps
f_{OUT}	Output Frequency		25	—	160	MHz

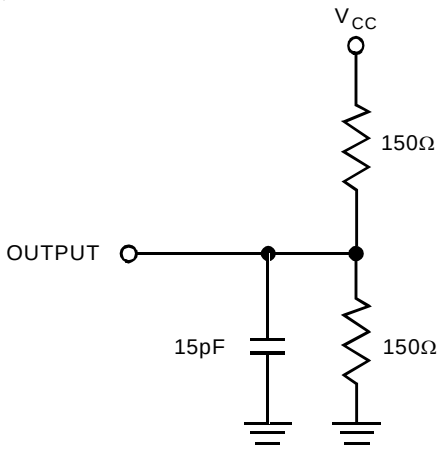
NOTE:
1. This parameter is guaranteed by design but not tested.

INPUT TIMING REQUIREMENTS

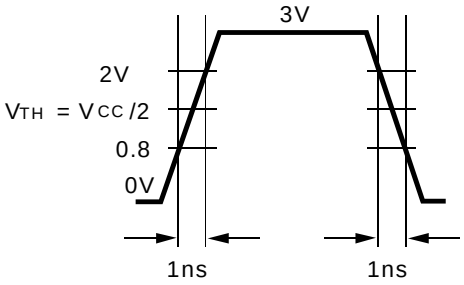
Symbol	Description	Min.	Max.	Unit
t_R, t_F	Maximum Input Rise and Fall Time, 0.8V to 2V (1)	—	2	ns
D_H	Input Duty Cycle (1)	25	75	%
f_{OSC}	XTAL Oscillator Frequency	—	30	MHz
f_{IN}	Input Frequency	25/N	160/N	MHz

NOTE:
1. This parameter is guaranteed by design but not tested.

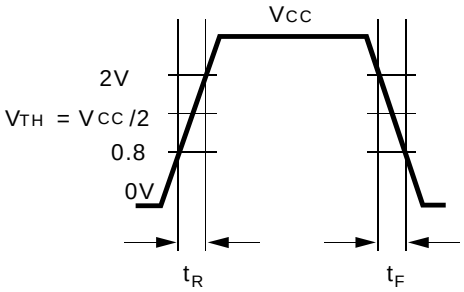
TEST LOADS AND WAVEFORMS



AC Test Load



Input Test Waveform



Output Waveform

HOW TO USE THE 5V925

The 5V925 is a general-purpose phase-locked loop (PLL) that can be used as a zero delay buffer or a clock multiplier. It generates three outputs at the VCO frequency and one output at the VCO frequency divided by n, where n is determined by the Mode/Frequency Select input pins S_0 and S_1. The PLL will adjust the VCO frequency (within the limits of the Function Table) to ensure that the input frequency equals the Q/N frequency.

The 5V925 can accept two types of input signal. The first is a reference clock generated by another device on the board which needs to be reproduced with a minimal delay between the incoming clock and output. The second is an external crystal. When used in the first mode, the crystal input (X_1) should be tied to ground and the crystal output (X_2) should be left unconnected.

By connecting Q/N to FB (see Figure 1), the 5V925 not only becomes a zero delay buffer, but also a clock multiplier. With proper selection of S_0 and S_1, the Q_0–Q_2 outputs will generate two, three, up to eight times the input clock frequency. Make sure that the input and output frequency specifications are not violated (refer to Function Table). There are some applications where higher fan-out is required. These kinds of applications could be addressed by using the 5V925 in conjunction with a clock buffer such as the 49FCT3805. Figure 2 shows how higher fan-out with different clock rates can be generated.

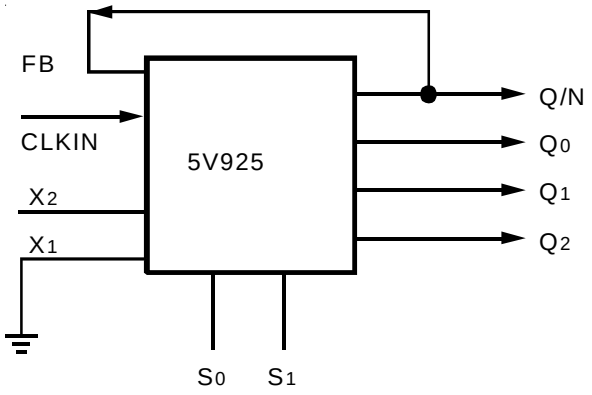


Figure 1

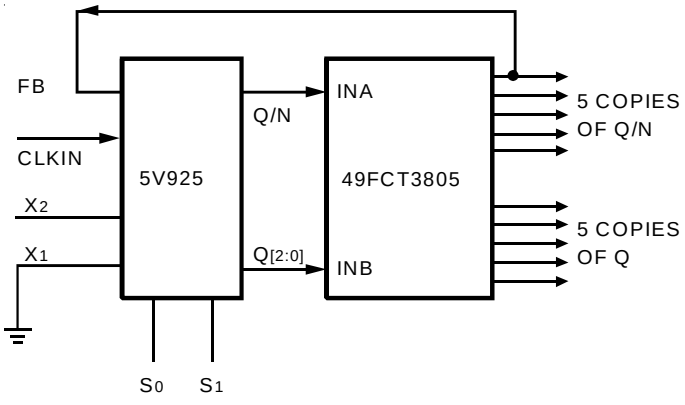


Figure 2

By connecting one of the 49FCT3505 outputs to the FB input of the 5V925 , the propagation delay from CLKIN to the output of the 49FCT3505 will be nearly zero. To ensure PLL stability, only one 49FCT3505 should be included between Q/N and FB.

The second way to drive the input of the 5V925 is via an external crystal. When connecting an external crystal to pins 5 and 6, the X_2 pin must be shorted to the CLKIN (pin 7) as shown in Figure 3. For best accuracy, a parallel resonant crystal with a crystal load capacitance rating of 15pF should be used. To reduce the parasitic between the external crystal and the 5V925 , it is recommended to connect the crystal as close as possible to the X_1 and X_2 pins.

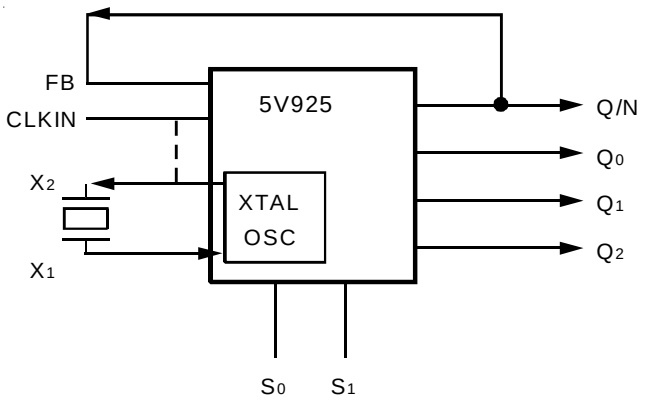


Figure 3

One of the questions often asked is what is the accuracy of our clock generators? In applications where clock synthesizers are used, the terms frequency accuracy and frequency error are used interchangeably. Here, frequency accuracy (or error) is based on two factors. One is the input frequency and the other is the multiplication factor. Clock multipliers (or synthesizers) are governed by the equation:

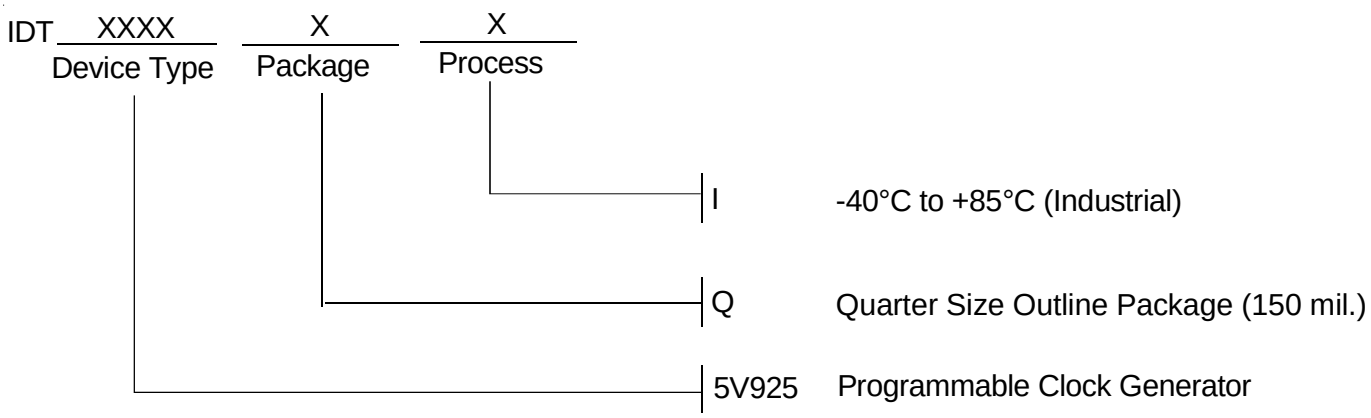
$$\text{Output Frequency} = \frac{(M)}{N} * \text{Input Frequency}$$

where "M" is the feedback divide and "N" is the reference divide. If the ratio of M/N is not an integer, then the output frequency will not be an exact multiple of the input. On the other hand, if the ratio were a whole number, the output clock would be an exact multiple of the input. In the case of 5V925, since the reference divide ("N") is "1", the equation is a strong function of the feedback divide ("M"). In addition, since the feedback is an integer, the output frequency error (or accuracy) is merely a function of how accurate the input is. For instance, 5V925 could accept two forms of input, one from a crystal oscillator (see Figure 1) and the other from a crystal (see Figure 3). By using a 20MHz clock with a multiplication factor of 5 (with an accuracy of ±30 parts per million), one can easily have three copies of 100MHz of clock with ±30PPM of accuracy. Frequency accuracy is defined by the following equation:

$$\text{Accuracy} = \frac{(\text{Measured Freq.} - \text{Nominal Freq.})}{\text{Nominal Frequency}}$$

where measured frequency is the average frequency over certain number of cycles (typically 10,000) and the nominal frequency is the desired frequency.

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459