JMicron Technology Corporation

JMF612

SATAII To Flash Controller Datasheet

Document No.: 61X-00002 / Revision: 1.04 / Issue Date: 09-12-2009

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Printed in Taiwan 2009

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Revision History

Revision	Effect Date	Description of Revision		Author
		Reference	Description of the Change	
1.01	06-26-2009		Draft release.	M
1.02	06-29-2009		Electrical Characteristics modified.	M
1.03	08-31-2009		10.4\10.5 modify.	M
1.04	09-12-2009		Delete Flash 2K page.	

This document is valid until ☐ the date dd-mm-yyyy ☒ the next revision has been effective.

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1 General Description

JMF612 is a single chip, supports external SDRAM, SATA II to NAND flash interface. It is native design to provide higher bandwidth for flash memory access.

JMF612 can support the maximum read and write speed to drive the limit of flash memory. JMF612 has the best supporting to the latest NAND flash memory, including Samsung, Toshiba, Hynix, Micron and IM Flash. It also provides the embedded hardware error correction code (ECC), wear leveling, and bad block management technology in this chip. In order to resolve compatibility issue, JMF612 provides the on line firmware upgrade ability.

JMF612 provides embedded processor, internal masked ROM, data SRAM, SATA link/transport layer, SATA PHY. Data swap between different interfaces can be done very efficiency by DMA without CPU involvement. Based on the efficient architecture, the JMF612 can provide the best performance.

2 Features

2.1 Compliance

- Compliant with Universal Serial Bus Specification Revision 2.0.
- Compliant with USB Mass Storage Class specification version 1.0.
- Compliant with Serial ATA International Organization: Serial ATA Revision 2.6.

2.2 SATAI\II

- Supports 1-port 1.5/3.0Gbps SATA I/II interface.

2.3 CPU

- Embedded data buffer.
- 32bits Embedded processor.
- 32 KBytes Embedded masked program ROM.
- 128 KBytes Embedded system RAM.

2.4 Flash

- Support maximum 16CE's Flash per channel.
- Support 5x/4x/3x nm Flash.
- Enhanced endurance by dynamic/static wear-leveling.

- Supports 4K/8K bytes page size.
- Supports dynamic power management.
- SMART (Self-Monitoring, Analysis and Reporting Technology).
- Data integrity under power-cycling.
- Supports online SATA/USB firmware update.
- Supports 8 bits Flash interface.
- Supports BCH 16/24 bits ECC.

2.5 SDRAM

- Supports DDR/DDR2
- Support 128Mbits to 2Gbits

2.6 SYSTEM

- Integrated 1-USB2.0 port, 1-SATA II port and 8-channels Flash controller.
- LED indicator for USB2.0 and SATA read/write access.
- LED indicator for USB2.0 and SATA PHY link up.
- Provides 14 GPIO pins for customer.
- Provides UART and JTAG for S/W debugging.
- Built-in power-up self-test (BIST).
- Manual and automatic self-diagnostics.
- Provides voltage low detect interrupt.
- 281-ball TFBGA package

2.7 Firmware

- Support NCQ on this controller.
- Support LBA24 & LBA48 on this controller.
- Support 1 to 8 banks selected free.
- Support 2 to 8 channels selected free.

3 Block Diagram

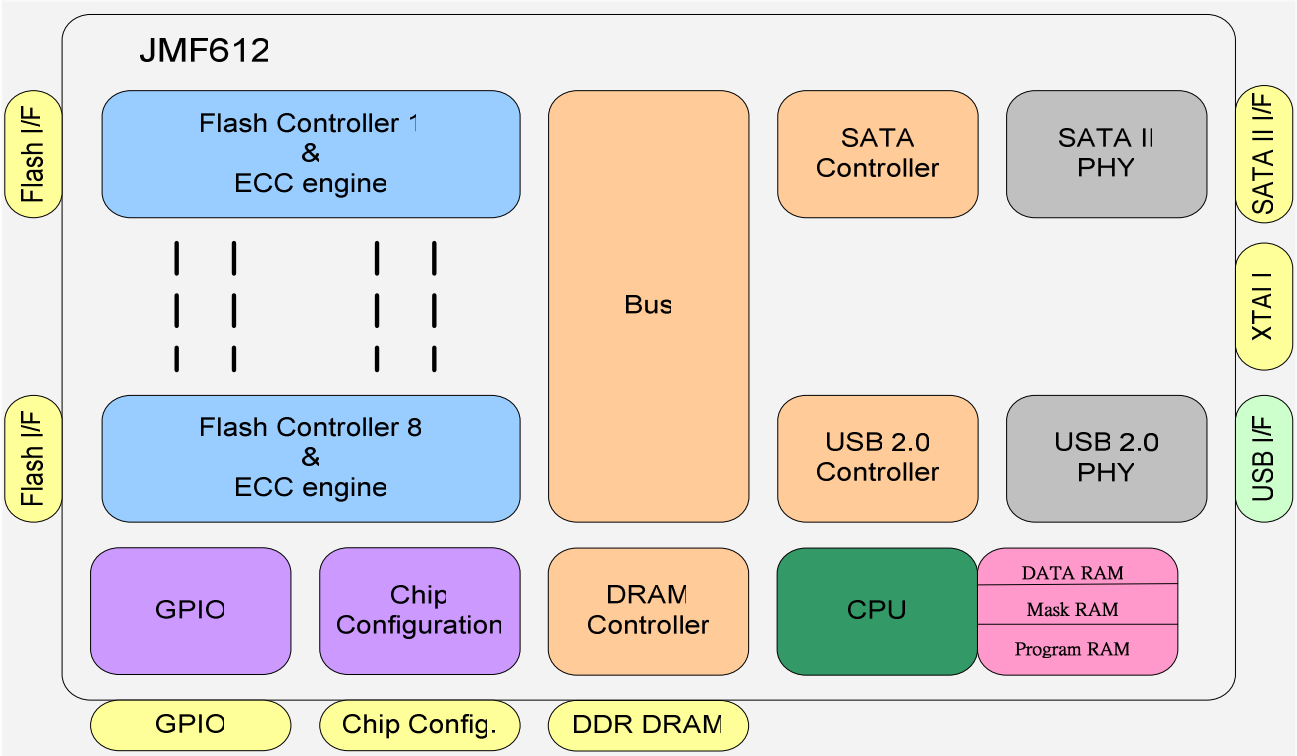

Figure 1 *Block diagram of JMF612*

4 Total Capacity

Table 1 Total capacity table

density/per flash	Support CE pins/per flash	maximum flash number	Total capacity
1G x 8 Bits (8Gb)	1 CE pin	32	32G Bytes
2G x 8 Bits (16Gb)	1 CE/ 2 CE pin	32	64G Bytes
4G x 8 Bits (32Gb)	1 CE/ 2 CE pin	32	128G Bytes
8G x 8 Bits (64Gb)	2 CE pin	32	256G Bytes
16G x 8 Bits (128Gb)	4 CE pin	32	512G Bytes

5 Package Pin Out (TFBGA 281 ball)

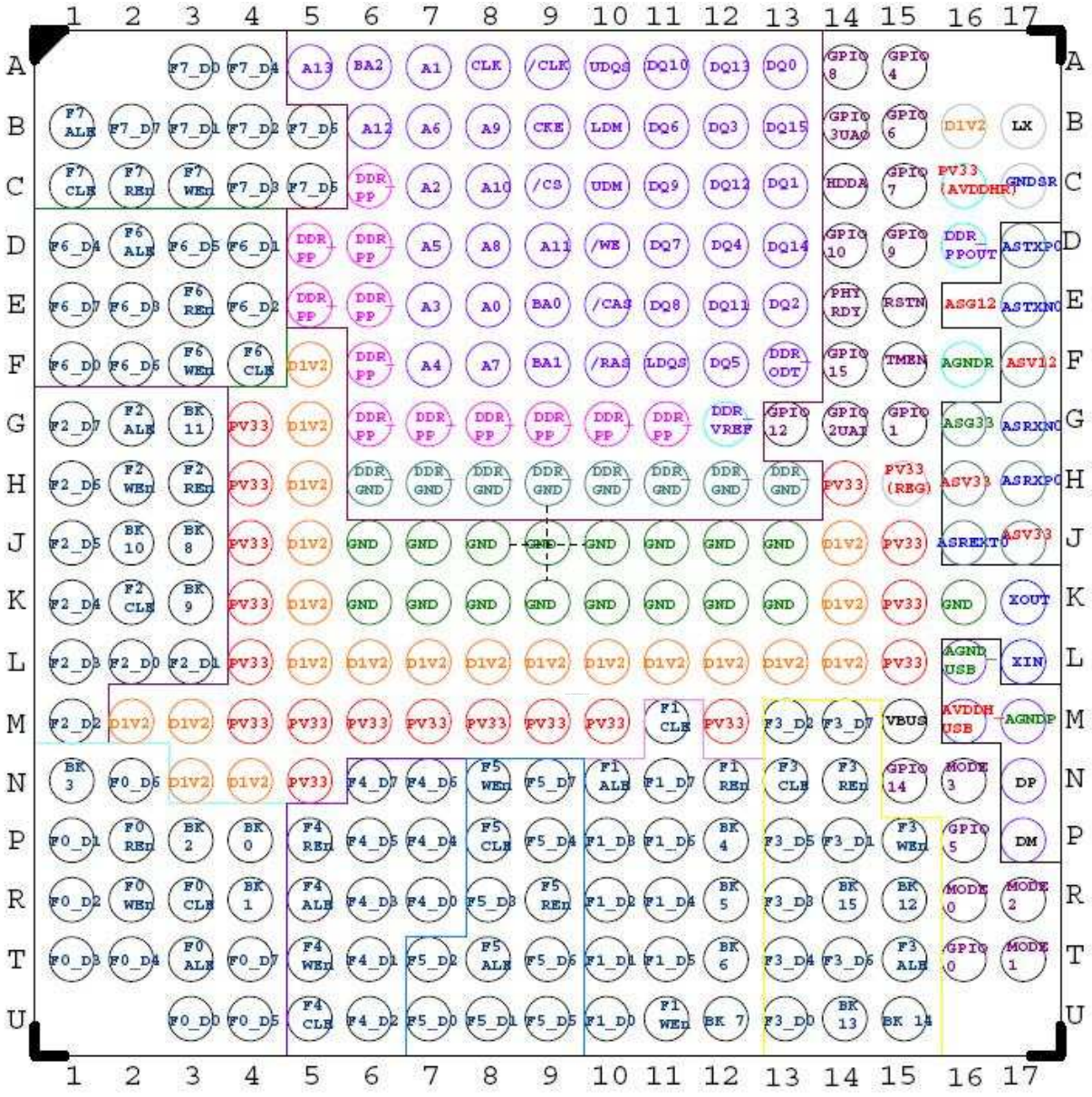

Figure 2 *Package ball assignment of JMF612*

6 Package Outline Drawing (TFBGA 281 ball)

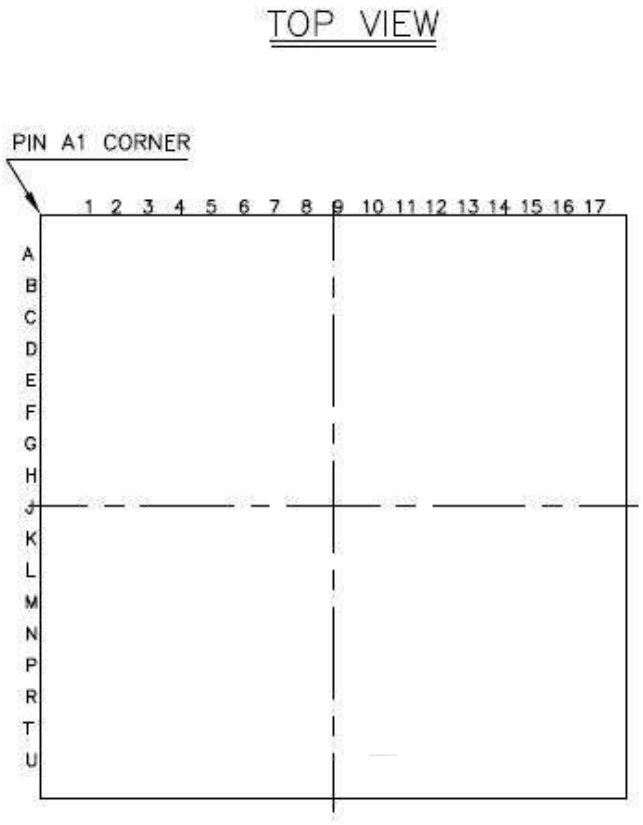

Figure 3 *Outline drawing_ Top view*

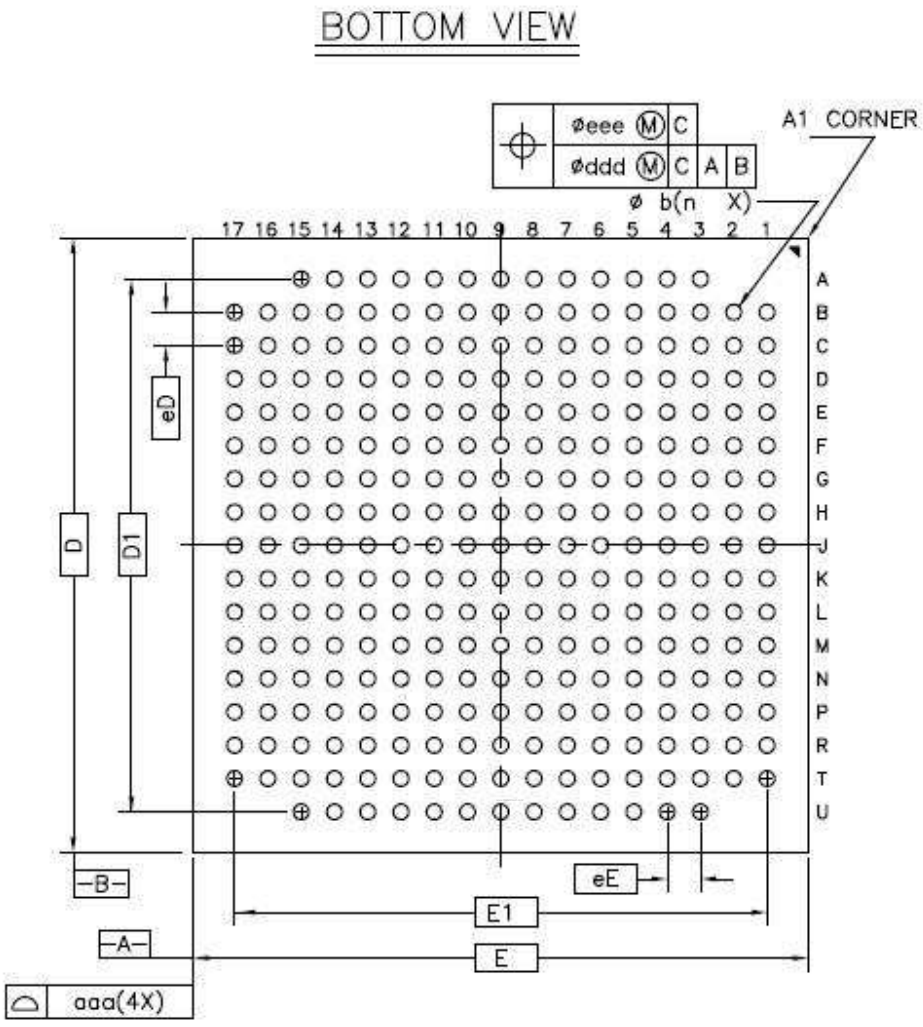

Figure 4 *Outline drawing_ Bottom view*

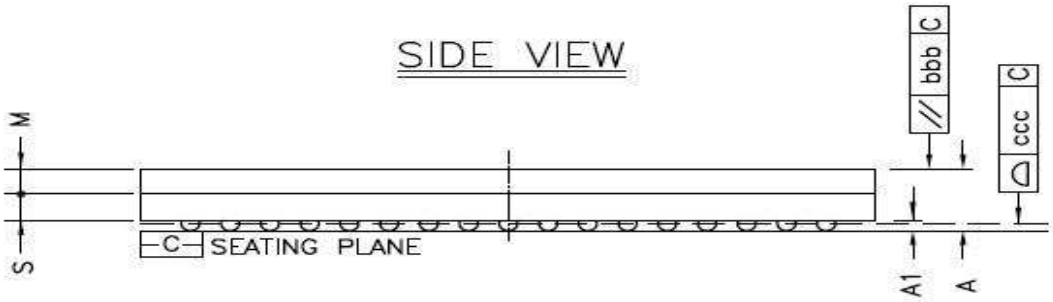

Figure 5 *Outline drawing_ Side view*

		Symbol	Common Dimensions
Package :			LFBGA
Body Size:	X	E	12.000
	Y	D	12.000
Ball Pitch :	X	eE	0.650
	Y	eD	0.650
Total Thickness :		A	1.400 MAX.
Mold Thickness :		M	0.530 Ref.
Substrate Thickness :		S	0.560 Ref.
Ball Diameter :			0.300
Stand Off :		A1	0.160 ~ 0.260
Ball Width :		b	0.270 ~ 0.370
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ccc	0.080
Ball Offset (Package) :		ddd	0.150
Ball Offset (Ball) :		eee	0.080
Ball Count :		n	281
Edge Ball Center to Center :	X	E1	10.400
	Y	D1	10.400

Figure 6 *Outline drawing_ symbol*

7 Pin Descriptions

7.1 Pin type definition

Table 2 Pin type definition table

Pin Type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
IL	Internal week pull-low (Typical 75KΩ)
IH	Internal week pull-high (Typical 75KΩ)

7.2 Pin definition

Table 3 Pin definition table

Signal Name	Ball No.	Type	Description
F0_[D0~D7]	U3,P1,R1,T1,T2,U4N2,T4	IO	**Flash data input/output** The I/O pins are used to output command, address, data and to input data during read operations.
F1_[D0~D7]	U10,T10,R10,P10,R11,T11,P11,N11	IO	**Flash data input/output** The I/O pins are used to output command, address, data and to input data during read operations.
F2_[D0~D7]	L2,L3,M1,L1,K1,J1H1,G1	IO	**Flash data input/output** The I/O pins are used to output command, address, data and to input data during read operations.
F3_[D0~D7]	U13,P14,M13,R13,T13,P13,T14,M14	IO	**Flash data input/output** The I/O pins are used to output command, address, data and to input data during read operations.
F4_[D0~D7]	R7,T6,U6,R6,P7,P6,N7,N6	IO	**Flash data input/output** The I/O pins are used to output command, address, data and to input data during read operations.
F5_[D0~D7]	U7,U8,T7,R8,P9,U9,T9,N9	IO	**Flash data input/output** The I/O pins are used to output command, address, data and to input data during read operations.

Signal Name	Ball No.	Type	Description
F6_[D0~D7]	F1,D4,E4,E2,D1,D3F2,E1	IO	**Flash data input/output** The I/O pins are used to output command, address, data and to input data during read operations.
F7_[D0~D7]	A3,B3,B4,C4,A4,C5B5,B2	IO	**Flash data input/output** The I/O pins are used to output command, address, data and to input data during read operations.
[F0~F7]_WEn	R2,U11,H2,P15,T5,N8,F3,C3	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WEn pulse
[F0~F7]_ALE	T3,N10,G2,T15,R5,T8,D2,B1	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
[F0~F7]_CLE	R3,M11,K2,N13,U5,P8,F4,C1	O	**Command Latch Enable** The CLE output controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
[F0~F7]_REn	P2,N12,H3,N14,P5,R9,E3,C2	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.
BK_[0n~15n]	P4,R4,P3,N1,P12,R12,T12,U12,J3,K3,J2,G3,R15,U14,U15,R14	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
GPIO0	T16	DIO	**General purpose I/O,** For normal function can be configured by customer.
GPIO1	G15	DIO	**General purpose I/O,** For normal function can be configured by customer.
GPIO2/UAI	G14	DIO	**General purpose I/O,** RS232 debug port.
GPIO3/UAO	B14	DIO	**General purpose I/O,** RS232 debug port.
GPIO4	A15	DIO	**General purpose I/O,(F/W setting)** 0: Run SATA 1.5Gbps. 1: Run SATA 3.0Gbps.

Signal Name	Ball No.	Type	Description
GPIO5	P16	DIO	**General purpose I/O,** 0: Load firmware code from flash to program memory. 1: Load firmware code from host to program memory.
GPIO6	B15	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO7	C15	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO8	A14	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO9	D15	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO10	D14	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO12	G13	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO14	N15	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO15	F14	DIO	**General purpose I/O,** Can be configured by customer firmware.
DM	P17	AIO	**USB Bus D- Signal.**
DP	N17	AIO	**USB Bus D+ Signal.**
VBUS	M15	I	**USB Cable Power Detector.** The 51K and 100K resistances should be connected to divide the 5V cable power into 3.3V.
AGND_USB	L16	AI	**USB Analog Ground.**
AGNDP	M17	AI	**USB Analog Ground.**
AVDDH_USB	M16	AI	**USB Analog 3.3V Power Supply.**
TMEn	F15	DIH	**Test Mode Enable, (internal pull-H)** This pin is reserved for IC mass production testing. Always Keep this pin to logic “1” in normal operation.
MODE[3:0]	N16,R17,T17,R16	IL	**Chip Operation Mode Selection.(internal 0000)** Ball B4 A3 B5 A4 0 0 0 0
RSTn	E15	DIH	**System Global Reset Input.** Active-low to reset the entire chip. An external 10msec RC should be connected to this pin.
HDDA	C14	DO	**SATA Hard Disk Active.(GPIO21)** Can be configured by customer firmware.
PHYRDY	E14	DO	**PHYRDY of SATA/USB output.**
XTALI	L17	AI	**Crystal input pad** It is connected to a 30MHz crystal.

Signal Name	Ball No.	Type	Description
XTALO	K17	AO	**Crystal output pad** It is connected to a crystal.
ASV33	H16,J17	AI	**SATA Analog 3.3V Power Supply.**
ASG33	G16	AI	**SATA Analog Ground.**
ASREXT0	J16	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.
ASRXP0	H17	AI	**Serial ATA RX+ signal.** A 10nF CAP. should be connected between this pin and SATA connector.
ASRXN0	G17	AI	**Serial ATA RX- signal.** A 10nF CAP. should be connected between this pin and SATA connector.
ASV12	F17	AI	**SATA Analog 1.2V Power Supply.** This power could be sourced from internal 1.2V voltage regulator through AVREG pin.
ASG12	E16	AI	**SATA Analog Ground.**
ASTXN0	E17	AO	**Serial ATA TX- signal.** A 10nF CAP. should be connected between this pin and SATA connector.
ASTXP0	D17	AO	**Serial ATA TX+ signal.** A 10nF CAP. should be connected between this pin and SATA connector.
LX	B17	AO	**Switching Regulator output.**
GNDSR	C17	AI	**Switching regulator ground**
PV33(REG)	H15	AI	**Switching regulator 3.3V power supply**
DDR_PPOUT	D16	AO	**DDR regulator output**
AGNDR	F16	AI	**DDR regulator ground**
PV33(AVDDHR)	C16	AI	**DDR regulator 3.3v power supply**
A0	E8	O	**Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.**
A1	A7		
A2	C7		
A3	E7		
A4	F7		
A5	D7		
A6	B7		
A7	F8		
A8	D8		
A9	B8		
A10	C8		
A11	D9		
A12	B6		
A13	A5		
BA0	E9	O	**Bank address inputs: BA[2:0] define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being**
BA1	F9		

Signal Name	Ball No.	Type	Description
BA2	A6		**applied. BA[2:0] define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.**
CK	A8	O	**Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.**
CK#	A9		
CKE	B9	O	**Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge powerdown and SELF REFRESH operation (all banks idle), or ACTIVATE power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for self refresh entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once Vdd is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation, Vref must be maintained.**
CS#	C9	O	**Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered high. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.**
LDM	B10	O	**Input data mask: DM is an input mask signal for write data. Input data is masked when DM is concurrently sampled HIGH during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.**
UDM	C10		

Signal Name	Ball No.	Type	Description
ODT	F13		On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#	F10	O	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
CAS#	E10		
WE#	D10		
DQ0	A13	IO	Data input/output: Bidirectional data bus for x16.
DQ1	C13		Data input/output: Bidirectional data bus for x16.
DQ2	E13		Data input/output: Bidirectional data bus for x16.
DQ3	B12		Data input/output: Bidirectional data bus for x16.
DQ4	D12		Data input/output: Bidirectional data bus for x16.
DQ5	F12		Data input/output: Bidirectional data bus for x16.
DQ6	B11		Data input/output: Bidirectional data bus for x16.
DQ7	D11		Data input/output: Bidirectional data bus for x16.
DQ8	E11		Data input/output: Bidirectional data bus for x16.
DQ9	C11		Data input/output: Bidirectional data bus for x16.
DQ10	A11		Data input/output: Bidirectional data bus for x16.
DQ11	E12		Data input/output: Bidirectional data bus for x16.
DQ12	C12		Data input/output: Bidirectional data bus for x16.
DQ13	A12		Data input/output: Bidirectional data bus for x16.
DQ14	D13		Data input/output: Bidirectional data bus for x16.
DQ15	B13		Data input/output: Bidirectional data bus for x16.
LDQS	F11	IO	Data strobe for lower byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
UDQS	A10	IO	Data strobe for upper byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
PV33	G4	DI	I/O Pad 3.3V Power Supply.
PV33	H4	DI	I/O Pad 3.3V Power Supply.
PV33	H14	DI	I/O Pad 3.3V Power Supply.
PV33	J4	DI	I/O Pad 3.3V Power Supply.
PV33	J15	DI	I/O Pad 3.3V Power Supply.
PV33	K4	DI	I/O Pad 3.3V Power Supply.
PV33	K15	DI	I/O Pad 3.3V Power Supply.

Signal Name	Ball No.	Type	Description
PV33	L4	DI	**I/O Pad 3.3V Power Supply.**
PV33	L15	DI	**I/O Pad 3.3V Power Supply.**
PV33	M4	DI	**I/O Pad 3.3V Power Supply.**
PV33	M5	DI	**I/O Pad 3.3V Power Supply.**
PV33	M6	DI	**I/O Pad 3.3V Power Supply.**
PV33	M7	DI	**I/O Pad 3.3V Power Supply.**
PV33	M8	DI	**I/O Pad 3.3V Power Supply.**
PV33	M9	DI	**I/O Pad 3.3V Power Supply.**
PV33	M10	DI	**I/O Pad 3.3V Power Supply.**
PV33	M12	DI	**I/O Pad 3.3V Power Supply.**
PV33	N5	DI	**I/O Pad 3.3V Power Supply.**
GND	J6	DI	**Ground.**
GND	J7	DI	**Ground.**
GND	J8	DI	**Ground.**
GND	J9	DI	**Ground.**
GND	J10	DI	**Ground.**
GND	J11	DI	**Ground.**
GND	J12	DI	**Ground.**
GND	J13	DI	**Ground.**
GND	K6	DI	**Ground.**
GND	K7	DI	**Ground.**
GND	K8	DI	**Ground.**
GND	K9	DI	**Ground.**
GND	K10	DI	**Ground.**
GND	K11	DI	**Ground.**
GND	K12	DI	**Ground.**
GND	K13	DI	**Ground.**
GND	K16	DI	**Ground.**
DV12	F5	DI	**1.2V Power Supply.**
DV12	G5	DI	**1.2V Power Supply.**
DV12	H5	DI	**1.2V Power Supply.**
DV12	J5	DI	**1.2V Power Supply.**
DV12	J14	DI	**1.2V Power Supply.**
DV12	K5	DI	**1.2V Power Supply.**
DV12	K14	DI	**1.2V Power Supply.**
DV12	L5	DI	**1.2V Power Supply.**
DV12	L6	DI	**1.2V Power Supply.**
DV12	L7	DI	**1.2V Power Supply.**
DV12	L8	DI	**1.2V Power Supply.**
DV12	L9	DI	**1.2V Power Supply.**
DV12	L10	DI	**1.2V Power Supply.**
DV12	L11	DI	**1.2V Power Supply.**
DV12	L12	DI	**1.2V Power Supply.**
DV12	L13	DI	**1.2V Power Supply.**

Signal Name	Ball No.	Type	Description
DV12	L14	DI	**1.2V Power Supply.**
DV12	M2	DI	**1.2V Power Supply.**
DV12	M3	DI	**1.2V Power Supply.**
DV12	N3	DI	**1.2V Power Supply.**
DV12	N4	DI	**1.2V Power Supply.**
DV12	B16	DI	**1.2V Power Supply.**
DDR_PP	C6	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	D5	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	D6	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	E5	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	E6	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	F6	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	G6	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	G7	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	G8	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	G9	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	G10	DI	**DDR PAD 1.8V Power Supply**
DDR_PP	G11	DI	**DDR PAD 1.8V Power Supply**
DDR_VREF	G12	DI	**DDR PAD 0.9V reference voltage**
DDR_GND	H6	DI	**Ground for DDR PAD**
DDR_GND	H7	DI	**Ground for DDR PAD**
DDR_GND	H8	DI	**Ground for DDR PAD**
DDR_GND	H9	DI	**Ground for DDR PAD**
DDR_GND	H10	DI	**Ground for DDR PAD**
DDR_GND	H11	DI	**Ground for DDR PAD**
DDR_GND	H12	DI	**Ground for DDR PAD**
DDR_GND	H13	DI	**Ground for DDR PAD**

8 ECC Descriptions

Please refer to FIG. 4 that is a diagram illustrating an allocating method of a spare area in each page of a NAND flash memory, where in the specific ECC algorithm utilizes a Bose, Chaudhuri and Hocquengham (BCH) ECC algorithm. When a BCH 16 ECC algorithm encodes the data in the NAND flash memory, the parity code generated in the encoding process may occupy 28 bytes of the spare area in each page. When a BCH 24 ECC algorithm encodes the data in the NAND flash memory, the parity code generated in the encoding process may occupy 42 bytes of the spare area in each page.

When a BCH 16 algorithm decodes the data in the NAND flash memory, the data can be decoded correctly if the error bit happened in two sector (1024Bytes) is 16. When a BCH 24 algorithm decodes the

data in the NAND flash memory, the data can be decoded correctly if the error bit happened in two sector is 24.

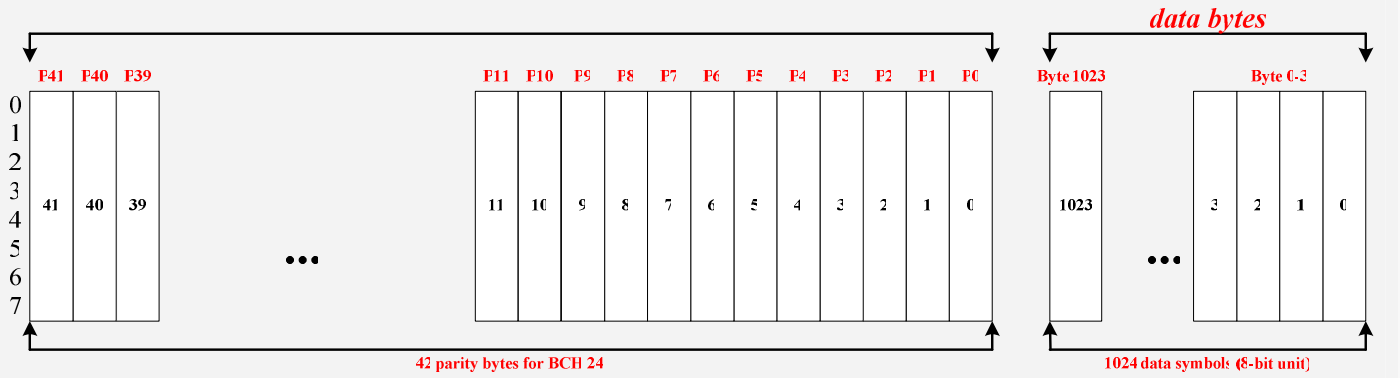

Figure 7 *Allocation for ECC algorithm BCH in NAND Flash*

9 SATA Interface

9.1 Out of bank signaling

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 $ALIGN_P$ primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having duration of 160 UI_{OOB}. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 5 and Table 2.

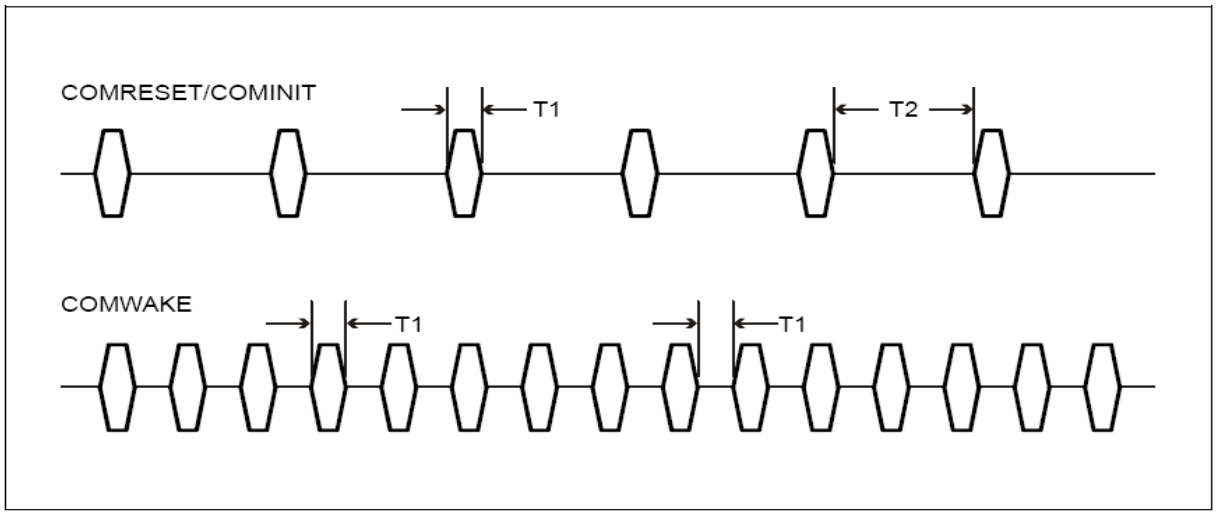

Figure 8 *OOB signals*

Table 4 OOB signal times

Time	Value
T1	160 UI_{oob} (106.7 ns nominal)
T2	480 UI_{oob} (320 ns nominal)

9.2 COMRESET

COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing.

The COMRESET signal shall be:

1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or 2) Started during the system hardware reset and ended some time after the negation of system hardware reset, or 3) Transmitted immediately following the negation of the system hardware reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hardware reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector looksfor four consecutive bursts with 320 ns spacing (nominal). Any spacing less than 175 ns or greater

than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the Phy layer shall initiate the Reset sequence shown in Figure 6 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly.

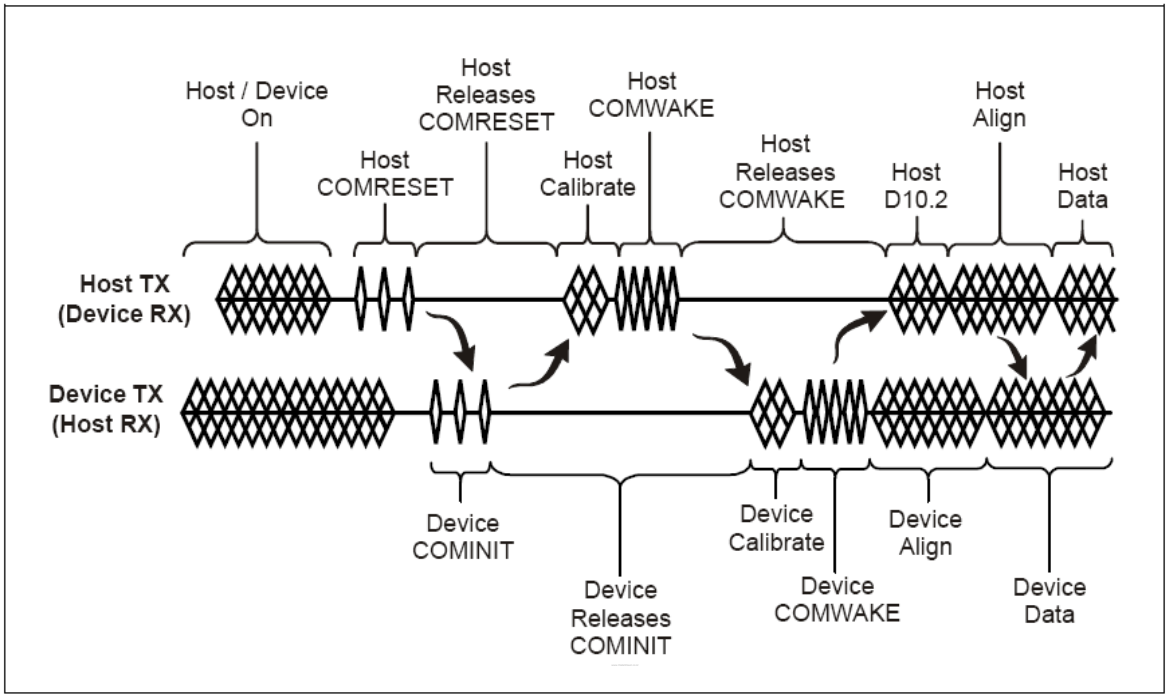

Figure 9 *Comreset sequence*

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the host causes the host to issue COMRESET
3. Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
4. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
5. Host calibrates and issues a COMWAKE.

6. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

7. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.

8. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.

9. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

9.3 COMINI

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 7, below:

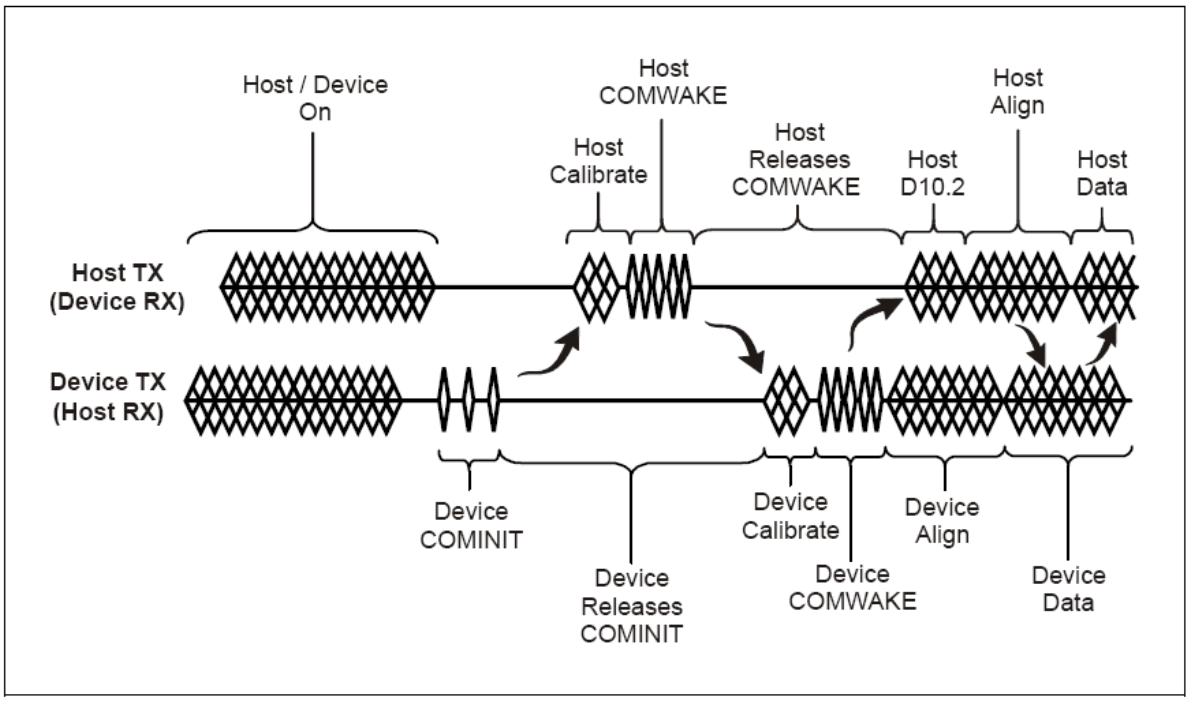

Figure 10 *Cominit sequence*

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the device causes the device to issues a COMINIT
3. Host calibrates and issues a COMWAKE.
4. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.
5. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see

section 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.

6. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.
7. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

9.4 Power on sequence timing diagram

The following timing diagrams and descriptions are provided for clarity and are informative. The state diagrams provided in section 8.4 comprise the normative behavior specification and is the ultimate reference

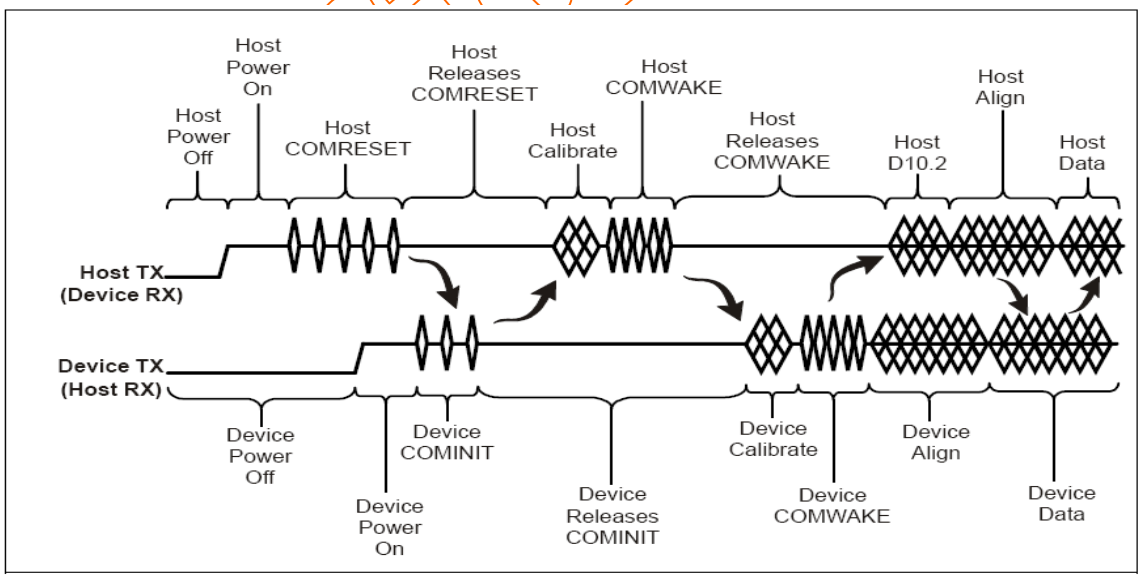

Figure 11 *Power on sequence*

Description:

1. Host/device power-off - Host and device power-off.
2. Power is applied - Host side signal conditioning pulls TX and RX pairs to neutral state (common mode voltage).
3. Host issues COMRESET
4. Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
5. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
6. Host calibrates and issues a COMWAKE.
7. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP primitives have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP primitives at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device shall enter an error state.
8. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This insures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
9. Device locks – the device locks to the ALIGN sequence and, when ready, sends the SYNCP primitive indicating it is ready to start normal operation.
10. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

9.5 ATA command register

This table with the following paragraphs summarizes the ATA command set.

Table 5 Command table

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	X	X	X	O	X	X
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	O	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
READ DMA	C8h or C9h	O	O	O	O	O	X
READ MULTIPLE	C4h	O	O	O	O	O	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6h	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3h	X	X	X	O	X	X
SECURITY ERASE UNIT	F4h	X	X	X	O	X	X
SECURITY FREEZE LOCK	F5h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2h	X	X	X	O	X	X
SEEK	7xh	X	X	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X
SMART	B0h	X	X	O	O	X	O
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE DMA	CAh or CBh	O	O	O	O	O	X

WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X

Note:

O = Valid, X = Don't care

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Low/High Register

DR = DEVICE SELECT Bit (DEVICE/HEAD Register Bit 4)

HD = HEAD SELECT Bit (DEVICE/HEAD Register Bit 3-0)

FT = Features Register

ATA COMMAND SPECIFICATIONS

CHECK POWER MODE (E5h)

The host can use this command to determine the current power management mode.

EXECUTE DIAGNOSITICS (90h)

This command performs the internal diagnostic tests implemented by the drive. See ERROR register for dianostic codes.

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

Table 6 Identify device information default value

Word	Value	F/V	Description
0	0040h		General configuration bit-significant information:
		F	15 0 = ATA device
		X	14-8 Retired
		F	7 1 = removable media device
		X	6 Obsolete

		X	5-3 Retired
		F	2 Reserved
		X	1 Retired
		F	0 Reserved
1	XXXXh	X	Number of logical cylinders

Table 7 Identify device information default value (*continued*)

Word	Value	F/V	Description
2	C837h	V	Specific configuration
3	00XXh	X	Number of logical heads
4-5	XXXXh	X	Retired
6	XXXXh	X	Number of logical sector per logical track
7-8	XXXXh	V	Reserved for assignment by the CompactFlash_ Association
9	000Eh	X	Retired
10-19	XXXXh	F	Serial number (20 ASCII characters)
20-21	XXXXh	X	Retired
22	003Fh	X	Obsolete
23-26	XXXXh	F	Firmware revision (8 ASCII characters)
27-46	XXXXh	F	Model number (40 ASCII characters)
47	8000h	F F F	15-8 80h 7-0 00h = Reserved 01h = Maximum number of 1 sectors on READ/WRITE MULTIPLE commands
48	4000h	F	Reserved
49	2F00h	 F F F F F F X	Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command. 11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired
50	4000h	 F F F X	Capabilities 15 Shall be cleared to zero. 14 Shall be set to one. 13-2 Reserved. 1 Obsolete

		F	0 Shall be set to one to indicate a device specific Standby timer value minimum.
51	0280h	X	15-8 PIO data transfer cycle timing mode 7-0 Reserved
52	0000h	X	Obsolete
53	0007h	F F F X	15-3 Reserved 2 1 = the fields reported in word 88 are valid 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words 70:64 are valid 0 = the fields reported in words 70:64 are not valid 0 1 = the fields reported in words 58:54 are valid 0 = the fields reported in words 58:54 are not valid
54	XXXXh	X	Number of current cylinders
55	00XXh	X	Number of current heads
56	XXXXh	X	Number of current sector per track
57-58	XXXXh	X	Current capacity in sectors
59	0000h	F V V	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	XXXXh	F	Total number of user addressable sectors
62	0000h	X	Obsolete
63	0007h	F V V V F F F F	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported 1 1 = Multiword DMA mode 1 and below are supported 0 1 = Multiword DMA mode 0 is supported
64	0003h	F F	15-8 Reserved 7-0 Advanced PIO modes supported
65	0078h	F	Minimum Multiword DMA transfer cycle time per word
66	0078h	F	Manufacturer's recommended Multiword DMA transfer cycle time
67	0078h	F	Minimum PIO transfer cycle time without flow control
68	0078h	F	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	F	Reserved (for future command overlap and queuing)
80	01FEh	 F F	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14

		F	13	Reserved for ATA/ATAPI-13
		F	12	Reserved for ATA/ATAPI-12
		F	11	Reserved for ATA/ATAPI-11
		F	10	Reserved for ATA/ATAPI-10
		F	9	Reserved for ATA/ATAPI-9
		F	8	Reserved for ATA/ATAPI-8
		F	7	1 = supports ATA/ATAPI-7
		F	6	1 = supports ATA/ATAPI-6
		F	5	1 = supports ATA/ATAPI-5
		F	4	1 = supports ATA/ATAPI-4
		F	3	Obsolete
		X	2	Obsolete
		X	1	Obsolete
		F	0	Reserved
81	0021h	F	Minor version number	
82	0068h		Command set supported.	
		X	15	Obsolete
		F	14	1 = NOP command supported
		F	13	1 = READ BUFFER command supported
		F	12	1 = WRITE BUFFER command supported
		X	11	Obsolete
		F	10	1 = Host Protected Area feature set supported
		F	9	1 = DEVICE RESET command supported
		F	8	1 = SERVICE interrupt supported
		F	7	1 = release interrupt supported
		F	6	1 = look-ahead supported
		F	5	1 = write cache supported
		F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not
		F	supported.	
		F	3	1 = mandatory Power Management feature set supported
		F	2	1 = Removable Media feature set supported
		F	1	1 = Security Mode feature set supported
			0	1 = SMART feature set supported
83	5000h		Command sets supported.	
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13-9	Reserved
		F	8	1 = SET MAX security extension supported
		F	7	Reserved
		F	6	1 = SET FEATURES subcommand required to spinup after power-up
		F	5	1 = Power-Up In Standby feature set supported
		F	4	1 = Removable Media Status Notification feature set supported
		F	3	1 = Advanced Power Management feature set supported
		F	2	1 = CFA feature set supported
		F	1	1 = READ/WRITE DMA QUEUED supported
		F	0	1 = DOWNLOAD MICROCODE command supported
84	4000h		Command set/feature supported extension.	
		F	15	Shall be cleared to zero

		F	14 Shall be set to one
		F	13-2 Reserved
		F	1 1 = SMART self-test supported
		F	0 1 = SMART error logging supported
85	0008h		Command set/feature enabled.
		X	15 Obsolete
		F	14 1 = NOP command enabled
		F	13 1 = READ BUFFER command enabled
		F	12 1 = WRITE BUFFER command enabled
		X	11 Obsolete
		V	10 1 = Host Protected Area feature set enabled
		F	9 1 = DEVICE RESET command enabled
		V	8 1 = SERVICE interrupt enabled
		V	7 1 = release interrupt enabled
		V	6 1 = look-ahead enabled
		V	5 1 = write cache enabled
		F	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not
		F	supported.
		F	3 1 = Power Management feature set enabled
		V	2 1 = Removable Media feature set enabled
		V	1 1 = Security Mode feature set enabled
			0 1 = SMART feature set enabled
86	5000h		Command set/feature enabled.
		F	15-9 Reserved
		F	8 1 = SET MAX security extension enabled by SET MAX SET PASSWORD
		F	7 See Address Offset Reserved Area Boot, INCITS TR27:2001
		F	6 1 = SET FEATURES subcommand required to spin-up after power-up
		V	5 1 = Power-Up In Standby feature set enabled
		V	4 1 = Removable Media Status Notification feature set enabled
		V	3-1 1 = Advanced Power Management feature set enabled
		F	0 1 = DOWNLOAD MICROCODE command supported
87	4000h		Command set/feature default.
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13-2 Reserved
		F	1 1 = SMART self-test supported
		F	0 1 = SMART error logging supported
88	203Fh		15-13 Reserved
		V	12 1 = Ultra DMA mode 4 is selected
			0 = Ultra DMA mode 4 is not selected
		V	11 1 = Ultra DMA mode 3 is selected
			0 = Ultra DMA mode 3 is not selected
		V	10 1 = Ultra DMA mode 2 is selected
			0 = Ultra DMA mode 2 is not selected
		V	9 1 = Ultra DMA mode 1 is selected
			0 = Ultra DMA mode 1 is not selected
		V	8 1 = Ultra DMA mode 0 is selected
			0 = Ultra DMA mode 0 is not selected
		F	7-5 Reserved

		F	4 1 = Ultra DMA mode 4 and below are supported
		F	3 1 = Ultra DMA mode 3 and below are supported
		F	2 1 = Ultra DMA mode 2 and below are supported
		F	1 1 = Ultra DMA mode 1 and below are supported
		F	0 1 = Ultra DMA mode 0 is supported
89	0000h	F	Time required for security erase unit completion
90	0000h	F	Time required for Enhanced security erase completion
91	0000h	V	Current advanced power management value
92	0000h	V	Master Password Revision Code
93	0000h	X	Hardware reset result
94-126	0000h	V	Reserved
127	0000h		Removable Media Status Notification feature set support
		F	15-2 Reserved
		F	1-0 00 = Removable Media Status Notification feature set not supported 01 = Removable Media Status Notification feature supported 10 = Reserved 11 = Reserved
128	0001h		Security status
		F	15-9 Reserved
		V	8 Security level 0 = High, 1 = Maximum
		F	7-6 Reserved
		F	5 1 = Enhanced security erase supported
		V	4 1 = Security count expired
		V	3 1 = Security frozen
		V	2 1 = Security locked
		V	1 1 = Security enabled
		F	0 1 = Security supported
129-159	0000h	X	Vendor specific
160-254	0000h	X	Reserved
255	0000h	X	Integrity word 15-8 Checksum 7-0 Signature

Key:
F/V = Fixed/variable content
F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = the content of the word may be fixed or variable.

IDLE (E3h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is

zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h)

This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

INITIALIZE DEVICE PARAMETERS (91h)

This command enables the host to set the number of sectors per track and the number of tracks per heads.

READ DMA (C8h)

Reads data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h/21h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of the requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

RECALIBRATE (10h)

The current drive performs no processing if it receives this command. It is supported for backward compatibility with previous devices.

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

SECURITY UNLOCK (F2h)

This command disabled LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

SEEK (7xh)

This command is effectively a NOP command to the device although it does perform a range check.

SET FEATURES (EFh)

This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

Table 8 Features register value and settable operating mode

Value	Function
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register.
55h	Disable read look-ahead feature
82h	Disable write cache
AAh	Enable read look-ahead feature

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

SLEEP (E6h)

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

SMART Function Set (B0h)

Performs different processing required for predicting device failures, according to the subcommand specified in the Features register. If the Features register contains an unsupported value, the Aborted Command error is returned. If the SMART function is disabled, any subcommand other than SMART ENABLE OPERATIONS results in the Aborted Command error.

STANDBY (E2h)

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA“Standby” Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h/31h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify “00h” to write 256 sectors.

10 Electrical Characteristics

10.1 Absolute Maximum Rating

Parameter	Symbol	Condition	Min	Max	Unit
Analog power supply	AVDDH		-0.5	6	V
Digital I/O power supply	DVDD		-0.5	6	V
Digital I/O input voltage	$V_{I(D)}$		-0.4	DVDD+0.4	V
Storage temperature	$T_{STORAGE}$		-55	140	^{o}C

10.2 Recommended Power Supply Operation Conditions and Temperature

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Operation digital power supply	PV33		3.0	3.3	3.6	V
	D1V2		-5%	1.2	+5%	V
Operation analog power supply	ASV33		3.0	3.3	3.6	V
	ASV12		-5%	1.2	+5%	V
	AVDDH		3.0	3.3	3.6	V
Operation DDR_PP power supply	DDR_PP		1.7	1.8	1.9	V
Operation DDR_Vref power supply	DDR_VREF	Vref=0.5x DDR_PP	0.85	Vref	0.95	V
Ambient operation temperature	T_A	For commercial spec.	0		70	^{o}C
Ambient operation temperature	T_A	For industry spec.	-40		85	^{o}C
Junction temperature	T_J				125	^{o}C
Case operation temperature	T_c	For commercial spec and base on T_A			85	^{o}C
Case operation temperature	T_c	For industry spec and base on T_A			100	^{o}C

TFBGA ?ball	θJC					°C/W
TFBGA ?ball	θJA					°C/W

10.3 Recommended External Clock Source Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				30		MHz
Clock Duty Cycle			45	50	55	%

10.4 Power Supply DC Characteristics (SATA Idle mode and power saving mode disable)

Power supply: PC's SATA 5V input. (Max=Peak)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital Power Supply	I_{PV33}	3.3V		7	14	mA
	I_{DV12}	1.2V		272	373	mA
USB Analog Power Supply	I_{AVDDH}	3.3V		6	18	mA
SATA Analog Power Supply	I_{ASV33}	3.3V		34	41	mA
SATA Analog Power Supply	I_{ASV12}	1.2V		61	68	mA
DDR PAD and DDRII	I_{DDR_PP}	1.8V		143	162	mA

10.5 Power Supply DC Characteristics (SATA Active mode)

Power supply: PC's SATA 5V input. (Max=Peak)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital Power Supply	I_{PV33}	3.3V		44	103	mA
	I_{DV12}	1.2V		320	442	mA
USB Analog Power Supply	I_{AVDDH}	3.3V		6	18	mA
SATA Analog Power Supply	I_{ASV33}	3.3V		34	41	mA
SATA Analog Power Supply	I_{ASV12}	1.2V		61	67	mA
DDR PAD and DDRII	I_{DDR_PP}	1.8V		135	302	mA

10.6 I/O DC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}		2.4			V

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Output low voltage	V_{OL}		1.5			V
Output high voltage	V_{OH}				3.3	V

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