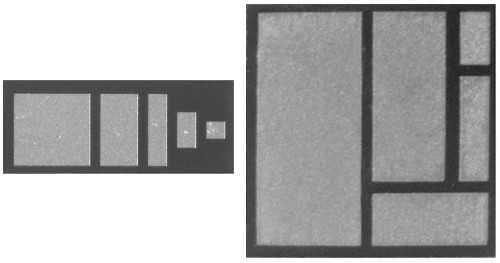
Thin Film Binary MOS Capacitors



Product may not be to scale

The CBB and CBC MOS capacitor chips each contain five different capacitors in binary increments allowing the user many choices in value selection.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CBB and CBCs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- User value selection
- Five capacitors on a 0.019 x 0.048 inches (CBB) or 0.044 inches square (CBC) chip
- Capacitance range: 1.0pF to 93pF in binary increments
- Dielectric: silicon dioxide
- Low dielectric loss
- Substrate: silicon with gold backing

APPLICATIONS

Vishay EFI CBB and CBC binary MOS multi-value capacitor chips are designed to be a useful device for trimming hybrid circuits by adding or subtracting capacitance, using normal wire-bonding techniques.

WV (DC) VALUES AND TOLERANCES

CAPACITOR MODEL	CBB	CBC
Total capacitance	31pF	93pF
Individual capacitance	1pF, 2pF, 4pF, 8pF, 16pF	3pF, 6pF, 12pF, 24pF, 48pF
Tolerance	± 10%	± 10%
DC Working voltage	75V	75V

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Peak voltage at + 25°C	1.5 x working voltage
Dissipation factor 1kHz, $1V_{rms}$, + 25°C	0.1%
Q at 1mHz, $50V_{rms}$, + 25°C	1000 minimum
TCC, - 55°C to + 150°C	+ 15 ± 25ppm/°C
Insulation resistance at working voltage, + 25°C	10^9 minimum
Operating temperature range	- 55°C to + 150°C
Thermal shock	± 0.25% + 0.25pF maximum ΔC/C
Moisture resistance, MIL-STD-202, Method 106	± 1.0% + 0.25pF maximum ΔC/C
Short time overload, + 25°C, 5 seconds: 1.5 x working voltage	± 0.25% + 0.25pF maximum ΔC/C
High temperature exposure: 100 hours at + 150°C ambient	± 0.25% + 0.25pF maximum ΔC/C
Life, MIL-STD-202, Method 108, Condition D, + 125°C ambient, 1000 hours at working voltage	± 2.0%+ 0.25pF maximum ΔC/C

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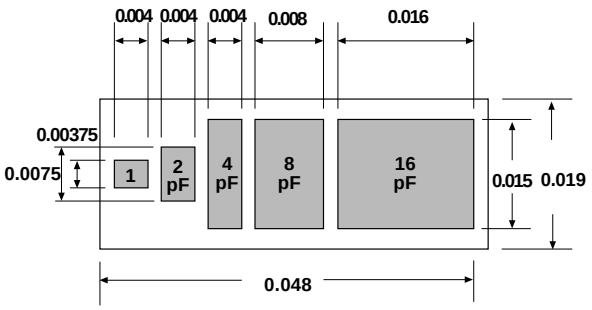
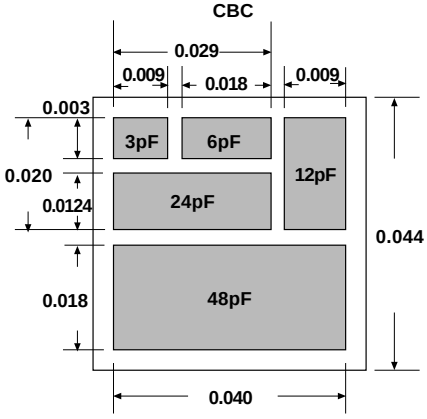
CONFIGURATIONS in inches

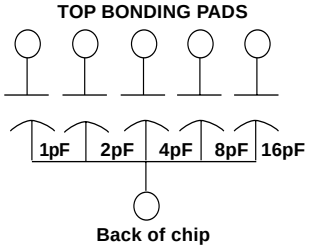
CBB

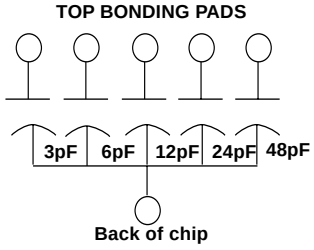


CBC



SCHEMATIC





MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip size, CBB CBC	0.019 x 0.048 ± 0.002 (0.48 x 1.2 ± 0.05mm) 0.044 x 0.044 ± 0.002 (1.1 x 1.1 ± 0.05mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Semiconductor Silicon
Dielectric	Silicon dioxide (MOS)
Bonding pads	10kÅ minimum aluminum
Backing	3kÅ minimum gold

OPTION: Gold bonding pads 15 kÅ minimum
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 93pF, 10%, CBC Capacitor, Aluminum Pads, Class H

P/N:	**W**	**CBC**	**012**	**9300**	**B**	**K**
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	CAPACITANCE VALUE (pF)	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts per MIL-STD-883 **X** = Sample, visually inspected loaded in matrix trays (4% AQL)	CBB CBC	**008** = CBB **012** = CBC	Use first 4 significant digits of the capacitance (C_T)	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1	**J** = 5.0% **K** = 10% **M** = 20% **L** = 25% **N** = 50%

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