REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30				
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Larry T. Gauder	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thanh V. Nguyen	
	APPROVED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, CMOS, RAD HARD MICROCONTROLLER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 99-03-05	
	REVISION LEVEL	SIZE: A; CAGE CODE: **67268**; **5962-98583**
		SHEET 1 OF 30

DSCC FORM 2233
APR 97

5962-E042-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	98583	01	Q	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT80CRH196KD	Radiation hardened Microcontroller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Quad flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

DC supply voltage (V_{DD}) -0.3 V to +6.0 V
Voltage on any pin ($V_{I/O}$) -0.3 V to V_{DD} +0.3 V
DC input current (I_I) - ±10 mA
Storage temperature (T_{STG}) -65°C to +150°C
Maximum power dissipation (P_D) - - - - - - - - - - - - - - - - 4W
Maximum junction temperature (T_J) - - - - - - - - - - - - - - - +175°C
Thermal resistance, junction-to-case (θ_{JC}) - - - - - - - - - 2°C/W per MIL-STD-883, Method 1012

1.4 Recommended operating conditions.

DC supply voltage (V_{DD}) - 4.5 V to 5.5 V
Temperature range (T_C) -55°C to +125°C
DC input voltage (V_{IN}) - 0 V to V_{DD}
High level input voltage (XTAL1) (V_{IH}) - - - - - - - - - - - - - - $0.7V_{DD}$
Low level input voltage (XTAL1) (V_{IL}) - - - - - - - - - - - - - - $0.3V_{DD}$
Min high level input voltage (V_{IH}) - - - - - - - - - - - - - - - 2.2 V 2/
Max low level input voltage (V_{IL}) - - - - - - - - - - - - - - - 0.8 V 2/

1.5 Radiation features.

Total dose (dose rate = 50 to 300 rad(Si)/s) - - - - - - 100 Krads (Si)
Single event phenomenon effective linear
energy threshold, (LET) no upset - - - - - - - - - - - - - 25 MeV-cm^2/mg
Neutron fluence - 1.0E14 n/cm^2

1.6 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) - - - - - - - - 95 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Except XTAL1 and $\overline{\text{RESET}}$.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Load circuit and waveforms. The Load circuit and waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input voltage (except XTAL1, $\overline{RESET}$)	V_{IL}		1, 2, 3	All		0.8	V
High level input voltage (except XTAL1, $\overline{RESET}$)	V_{IH}		1, 2, 3	All	2.2		V
High level input voltage (XTAL1)	V_{IH1}		1, 2, 3	All	$.7V_{DD}$		V
Low level input voltage (XTAL1)	V_{IL1}		1, 2, 3	All		$.3V_{DD}$	V
High level output voltage (Standard outputs)	V_{OH}	I_{OH} = -200 µA 13/ (CMOS) I_{OH} = -4.0 mA (TTL)	1, 2, 3	All	V_{DD}-.3 3.8		V
High level output current (Open drain outputs 2/ with pullups)	I_{OH1}	$V_{OH} = V_{DD}$ -.3 13/ $V_{OH} = V_{DD}$ -.9	1, 2, 3	All	-20 -60		µA
Low level output voltage	V_{OL}	I_{OL} = 200 µA (CMOS) 13/ I_{OL} = 4.0 mA (TTL)	1, 2, 3	All		0.3 0.4	V
Positive going threshold $\overline{RESET}$	V_{T+}		1, 2, 3	All	$.5V_{DD}$	$.7V_{DD}$	V
Negative going threshold $\overline{RESET}$	V_{T-}		1, 2, 3	All	$.2V_{DD}$	$.4V_{DD}$	V
Typical range of Hysteresis $\overline{RESET}$ 13/	V_H		1, 2, 3	All	.9		V
Pullups on $\overline{ADV}$, $\overline{RD}$, $\overline{RESET}$, Port 1, Port 2.0, 2.6, 2.7, AD0-15, $\overline{WR}$, $\overline{WRL}$, $\overline{BHE}$, ALE, CLKOUT	R_{PU}	V_{CC} = 5.5 V, $V_{IN} = V_{SS}$	1, 2, 3	All	6.9	36.7	KΩ
Pulldown on INST, NMI, HSO.0-HSO.3, P2.5	R_{PD}	V_{CC} = 5.5 V, $V_{IN} = V_{DD}$	1, 2, 3	All	3.7	27.5	KΩ
Logical 0 input current (Test mode entry) 3/	I_{IL}	$V_{IN} = V_{IH}$	1, 2, 3	All	-550	-120	µA
I/O leakage current, Standard inputs and Outputs	I_{LI}	$V_{IN} = V_{SS}$ or V_{DD}	1, 2, 3	All	-5	+5	µA
I/O leakage current, with pullups 4/	I_{LI1}	$V_{IN} = V_{SS}$	1, 2, 3	All	-800	-150	µA
I/O leakage current, with pulldowns 5/	I_{LI2}	$V_{IN} = V_{DD}$	1, 2, 3	All	200	1500	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤+125°C unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
Power supply current in Reset	$I_{DDRESET}$	CLK @ 20 MHz, $\overline{RESET}$ ≤ V_{IL}	1, 2, 3	All		65	mA
Active power supply current	AI_{DD}	CLK @ 20 MHz, typical Program flow	1, 2, 3	All		110	mA
Quiescent power supply Current	QI_{DD}		1, 3	All		20	µA
			2	All		1000	µA
		M,D,P,L, and R	1	All		1000	µA
Power supply current in Power down	I_{DDPD}	CLK @ 20MHz, no active I/O	1, 2, 3	All		6	mA
Power supply current in Idle mode	I_{DDIDLE}	CLK @ 20 MHz, no active I/O	1, 2, 3	All		55	mA
Pin capacitance	C_{IO}	@ 1 MHz, 25°C 13/	4	All		15	pF
Short circuit output current, Except for pins noted in Note 12	I_{OS}	V_{DD} = 5.5 V 11/ 13/	1, 2, 3	All	-100	130	mA
Short circuit output current, For pins noted in Note 12	I_{OS1}	V_{DD} = 5.5 V 11/ 12/ 13/	1, 2, 3	All	-200	250	mA
Functional tests		See 4.4.1c	7, 8	All			
Address VALID to READY Setup 13/	t_{AVYV}	See figure 4	9, 10, 11	All		$2T_{OSC}$ -30	ns
Non-READY time 13/	t_{YLYH}		9, 10, 11	All	No upper limit		ns
READY hold after CLKOUT Low 6/ 13/	t_{CLYX}		9, 10, 11	All	0	$2T_{OSC}$ -20	ns
READY hold after ALE low 6/ 13/	t_{LLYX}		9, 10, 11	All	T_{OSC}	$3T_{OSC}$ -20	ns
Address valid to BUSWIDTH setup 13/	t_{AVGV}		9, 10, 11	All		$2T_{OSC}$ -30	ns
BUSWIDTH hold after CLKOUT low 13/	t_{CLGX}		9, 10, 11	All	0		ns
Address valid to input data Valid 7/ 13/	t_{AVDV}		9, 10, 11	All		$3T_{OSC}$ -29	ns
$\overline{RD}$ Active to input data valid 7/	t_{RLDV}		9, 10, 11	All	5 13/	T_{OSC}-26	ns
CLKOUT low to input data Valid 13/	t_{CLDV}		9, 10, 11	All	5	T_{OSC}-26	ns
End of $\overline{RD}$ to input data float 13/	t_{RHDZ}		9, 10, 11	All	0	T_{OSC}-10	ns
Data hold after $\overline{RD}$ inactive 13/	t_{RXDX}		9, 10, 11	All	0	T_{OSC}-10	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤+125°C unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Frequency on XTAL1 13/	f_{OSC}	See figure 4	9, 10, 11	All	1	20	MHz
XTAL1 period (1/f_{OSC}) 13/	T_{OSC}		9, 10, 11	All	50	1000	ns
XTAL1 high to CLKOUT high or low	t_{XHCH}		9, 10, 11	All	0	25	ns
CLKOUT cycle time	t_{CLCL}		9, 10, 11	All	$2T_{OSC}$		ns
CLKOUT high period 13/	t_{CHCL}		9, 10, 11	All	T_{OSC}-10	T_{OSC} +10	ns
CLKOUT falling edge to ALE rising	t_{CLLH}		9, 10, 11	All	-5	+15	ns
ALE falling edge to CLKOUT rising 13/	t_{LLCH}		9, 10, 11	All	-29	+15	ns
ALE cycle time 7/	t_{LHLH}		9, 10, 11	All	$4T_{OSC}$		ns
ALE high period 13/	t_{LHLL}		9, 10, 11	All	T_{OSC}-10	T_{OSC} +15	ns
Address setup to ALE Falling edge 13/	t_{AVLL}		9, 10, 11	All	T_{OSC}-15		ns
Address hold after ALE Falling edge	t_{LLAX}		9, 10, 11	All	T_{OSC}-20	T_{OSC+}5	ns
ALE falling edge to $\overline{RD}$ Falling edge	t_{LLRL}		9, 10, 11	All	T_{OSC}-5	T_{OSC+}10	ns
$\overline{RD}$ low to CLKOUT falling Edge	t_{RLCL}		9, 10, 11	All	-5	+10	ns
$\overline{RD}$ low period 7/	t_{RLRH}		9, 10, 11	All	T_{OSC}-5		ns
$\overline{RD}$ rising edge to ALE risng Edge 8/ 13/	t_{RHLH}		9, 10, 11	All	T_{OSC} -10	T_{OSC} +10	ns
$\overline{RD}$ low to address float 13/	t_{RLAZ}		9, 10, 11	All	-5	+5	ns
ALE falling edge to $\overline{WR}$ Falling edge 13/	t_{LLWL}		9, 10, 11	All	T_{OSC}-10	T_{OSC} +10	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
CLKOUT low to $\overline{WR}$ falling edge	t_{CLWL}	See figure 4	9, 10, 11	All	-5	+10	ns
Data stable to $\overline{WR}$ rising Edge 7/	t_{QVWH}		9, 10, 11	All	T_{OSC}-10	T_{OSC} +10	ns
CLKOUT high to $\overline{WR}$ rising Edge 13/	t_{CHWH}		9, 10, 11	All	-10	+15	ns
$\overline{WR}$ low period 7/ 13/	t_{WLWH}		9, 10, 11	All	T_{OSC}-10		ns
Data hold after $\overline{WR}$ rising Edge 13/	t_{WHQX}		9, 10, 11	All	T_{OSC}-10	T_{OSC} +10	ns
$\overline{WR}$ rising edge to ALE Rising edge 8/ 13/	t_{WHLH}		9, 10, 11	All	T_{OSC}-10	T_{OSC} +10	ns
$\overline{BHE}$, INST after $\overline{WR}$ rising Edge 13/	t_{WHBX}		9, 10, 11	All	T_{OSC}-10	T_{OSC} +10	ns
AD8-15 HOLD after $\overline{WR}$ Rising 9/ 13/	t_{WHAX}		9, 10, 11	All	T_{OSC}-25		ns
$\overline{BHE}$, INST after $\overline{RD}$ rising Edge 13/	t_{RHBX}		9, 10, 11	All	T_{OSC}-10	T_{OSC} +10	ns
AD8-15 HOLD after $\overline{RD}$ Rising 9/ 13/	t_{RHAX}		9, 10, 11	All	T_{OSC}-25		ns
Address valid to $\overline{EDACEN}$ Valid 13/	t_{AVENV}		9, 10, 11	All		$2T_{OSC}$ -30	ns
$\overline{EDACEN}$ hold after ALE High 13/	t_{LHENX}		9, 10, 11	All	0		ns
Address valid to EDAC Input valid 7/ 13/	t_{AVEV}		9, 10, 11	All		$3T_{OSC}$ -29	ns
EDAC hold after $\overline{RD}$ inactive 13/	t_{RXEX}		9, 10, 11	All	0	T_{OSC} -10	ns
EDAC output stable to $\overline{WR}$ Rising 7/ 13/	t_{EVWH}		9, 10, 11	All	T_{OSC} -10	T_{OSC} +10	ns
EDAC output hold after $\overline{WR}$ Rising 13/	t_{WHEX}		9, 10, 11	All	T_{OSC} -10	T_{OSC} +10	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤+125°C unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
EXTERNAL CLOCK DRIVE TIMING CHARACTERISTICS							
Oscillator Frequency	f_{osc}	See figure 4	9, 10, 11	All	1 13/	20	MHz
Oscillator Period ($1/f_{osc}$)	T_{OSC}		9, 10, 11	All	50	1000 13/	ns
High time 13/	t_{OSCH}		9, 10, 11	All	17		ns
Low time 13/	t_{OSCL}		9, 10, 11	All	17		ns
Rise time 10/	t_{OSCR}		9, 10, 11	All		10	ns
Fall time 10/	t_{OSCF}		9, 10, 11	All		10	ns
$\overline{HOLD}$/$\overline{HLDA}$ TIMINGS							
$\overline{HOLD}$ setup 13/	t_{HVCH}	See figure 4	9, 10, 11	All	25		ns
CLKOUT low to $\overline{HLDA}$ low 13/	t_{CLHAL}		9, 10, 11	All	-15	15	ns
CLKOUT low to $\overline{BREQ}$ low 13/	t_{CLBRL}		9, 10, 11	All	-15	15	ns
$\overline{HLDA}$ low to address float 13/	t_{HALAZ}		9, 10, 11	All		10	ns
$\overline{HLDA}$ low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ driven weakly 13/	t_{HALBZ}		9, 10, 11	All		15	ns
CLKOUT low to $\overline{HLDA}$ high 13/	t_{CLHAH}		9, 10, 11	All	-15	15	ns
CLKOUT low to $\overline{BREQ}$ high 13/	t_{CLBRH}		9, 10, 11	All	-15	15	ns
$\overline{HLDA}$ high to address no Longer float 13/	t_{HAHAX}		9, 10, 11	All	-15		ns
$\overline{HLDA}$ high to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ valid 13/	t_{HAHBV}		9, 10, 11	All	-10		ns
CLKOUT low to ALE high 13/	t_{CLLH}		9, 10, 11	All	-5	15	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
SERIAL PORT TIMING							
Serial port clock period (BRR = 8002H)	t_{XLXL}	See figure 4	9, 10, 11	All	6 T_{OSC}		ns
Serial port clock falling Edge to rising edge (BRR = 8002H) 13/	t_{XLXH}		9, 10, 11	All	4 T_{OSC} -50	4 T_{OSC} +50	ns
Serial port clock period (BRR = 8001H)	t_{XLXL}		9, 10, 11	All	4 T_{OSC}		ns
Serial port clock falling Edge to rising edge (BRR = 8001H) 13/	t_{XLXH}		9, 10, 11	All	2 T_{OSC} -50	2 T_{OSC} +50	ns
Output data valid to clock Rising edge 13/	t_{QVXH}		9, 10, 11	All	2 T_{OSC} -50		ns
Output data hold after clock Rising edge 13/	t_{XHQX}		9, 10, 11	All	2 T_{OSC} -50		ns
Next output data valid after Clock rising edge 13/	t_{XHQV}		9, 10, 11	All		2 T_{OSC} +50	ns
Input data setup to clock Rising edge 13/	t_{DVXH}		9, 10, 11	All	T_{OSC} +50		ns
Input data hold after clock Rising edge 13/	t_{XHDX}		9, 10, 11	All	0		ns
Last clock rising to output Float 13/	t_{XHQZ}		9, 10, 11	All	2 T_{OSC} -10	2 T_{OSC} +10	ns

See footnotes on next page.

TABLE IA. Electrical performance characteristics – Continued.

1/ Devices supplied to this drawing are characterized at all levels M, D, P, L, and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Open-drain outputs include Port 1, P2.6 and P2.7.

3/ Test modes are entered at the $\overline{\text{RESET}}$ rising edge by applying V_{IL} to one or more of the following pins TXD, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{HLDA}}$. To avoid entering a test mode, ensure that these pins remain above V_{IH} during the rising edge of $\overline{\text{RESET}}$.

4/ Inputs/outputs with pullup resistors include: $\overline{\text{RESET}}$, Port 1, Port 2.0, P2.6, P2.7, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, AD0-15, $\overline{\text{RD}}$, ALE, CLKOUT.

5/ Inputs/outputs with pulldown resistors include: NMI, HSO.0- HSO.3, P2.5, INST.

6/ If max exceeded, additional wait state occurs.

7/ If wait states are used, add 2 T_{OSC} *N, where N = number of wait states.

8/ Assuming back-to-back bus cycles.

9/ 8-bit only.

10/ Supplied as a design limit but not guaranteed or tested.

11/ Not more than one output may be shorted at a time for maximum duration of one second.

12/ The I_{OS1} spec applies to pins $\overline{\text{RESET}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{RD}}$, ALE and CLKOUT.

13/ Tested only at initial qualification, and after any design or process changes which may affect this characteristic.

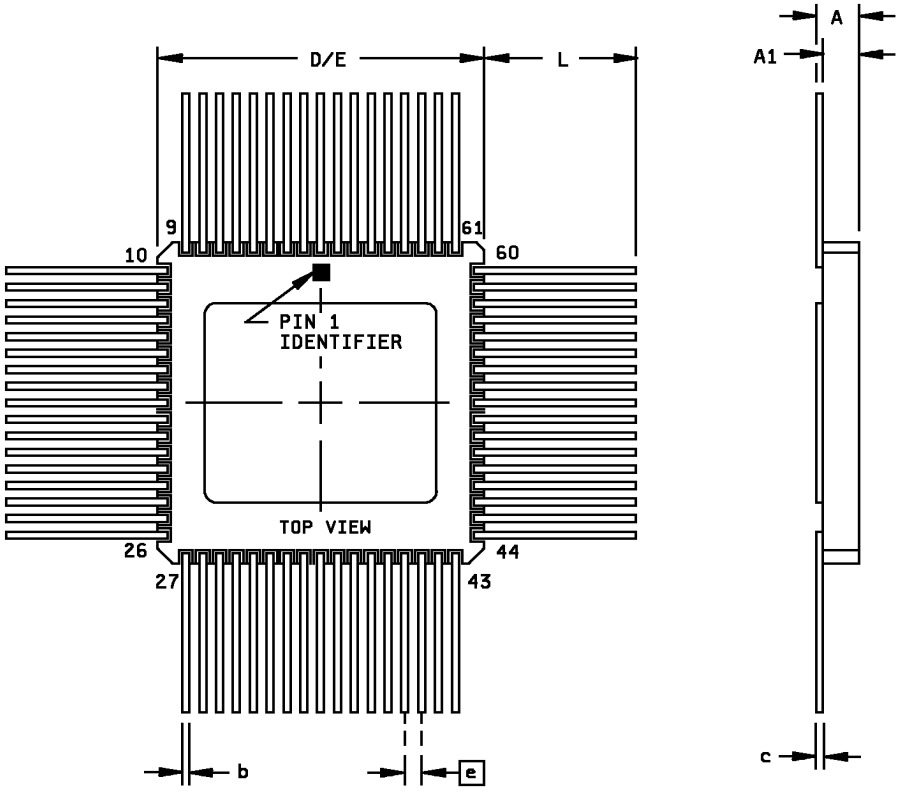
TABLE IB. SEP test limits . 1/ 2/

Device Type	T_A = Temperature ±10°C 3/	V_{CC} = 4.5 V		V_{CC} = 5.5 V
		Effective LET no Upsets [MeV-cm^2/mg)]	Maximum device cross section (Cm^2) (LET = 80)	Effective LET no Latchup 3/ [MeV-cm^2/mg)
All	+25°C	= 25	3.0×10^{-3}	> 128

1/ Devices that contain cross coupled resistance must be tested at the maximum rated T_A . For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature T_A = +125°C.

WELBULL AND DEVICE PARAMETERS FOR ERROR-RATE CALCULATION

SHAPE PARAMETER	WIDTH PARAMETER	STRUCTURAL CROSS-SECTION	ONSET LET	DEPLETION DEPTH	FUNNEL DEPTH
1	14	3.66E-7cm^2/bit	14.4MeV-cm^2/mg	0.8µm	1.45µm



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	---	2.74	---	.108
A1	1.83	2.24	.072	.088
b	0.35	0.46	.014	.018
c	0.18	0.24	.007	.0095
L	6.35	---	.250	---
D	21.6	24.50	.850	.965
E	21.6	24.50	.850	.965
e	1.27 TYP	1.27 TYP	.050 TYP	.050 TYP
N	68	68	68	68

NOTES:

1. The U. S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. All leads increase max limit by 0.003 inches measured at the center of the flat when lead finish A is applied.
3. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

FIGURE 1. Case outline.

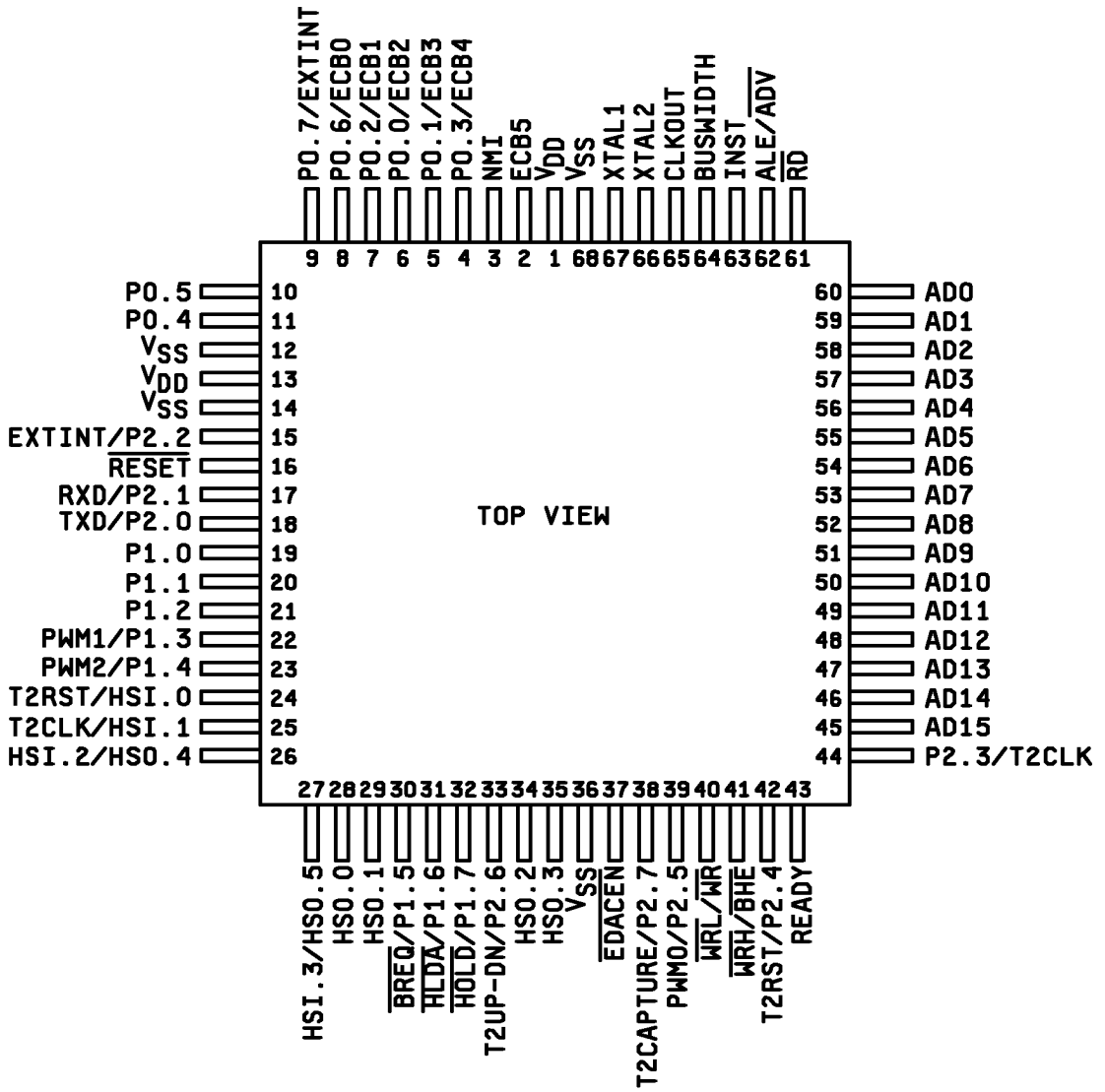


FIGURE 2. Terminal connections.

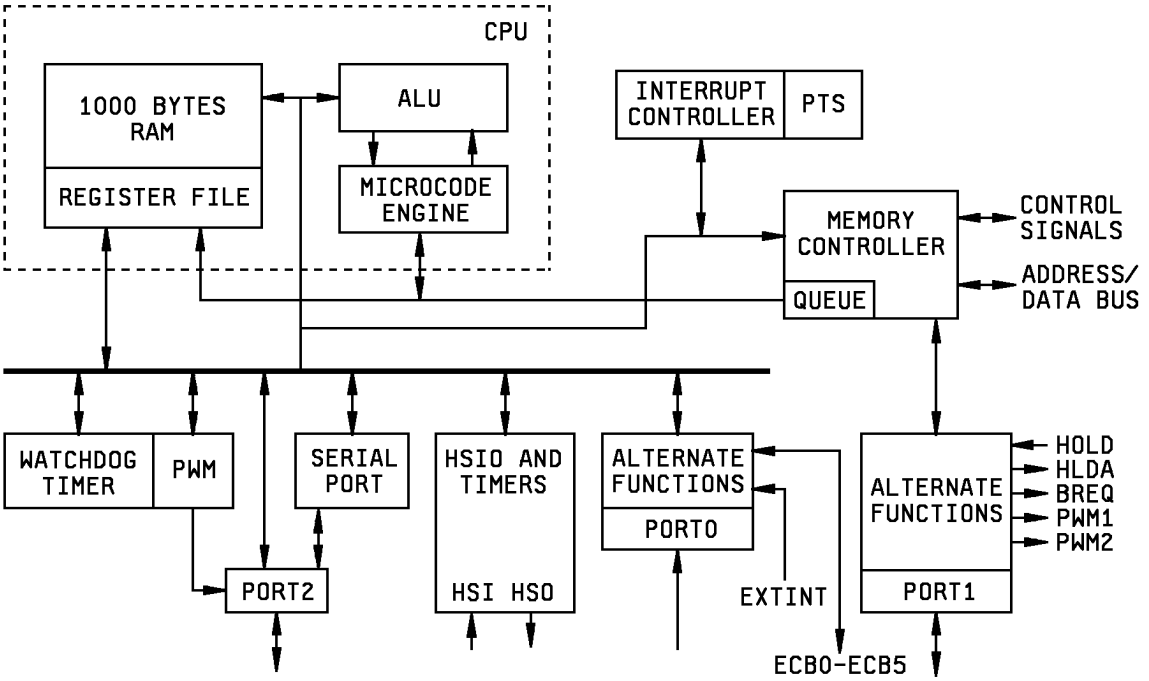


FIGURE 3. Functional Block diagram.

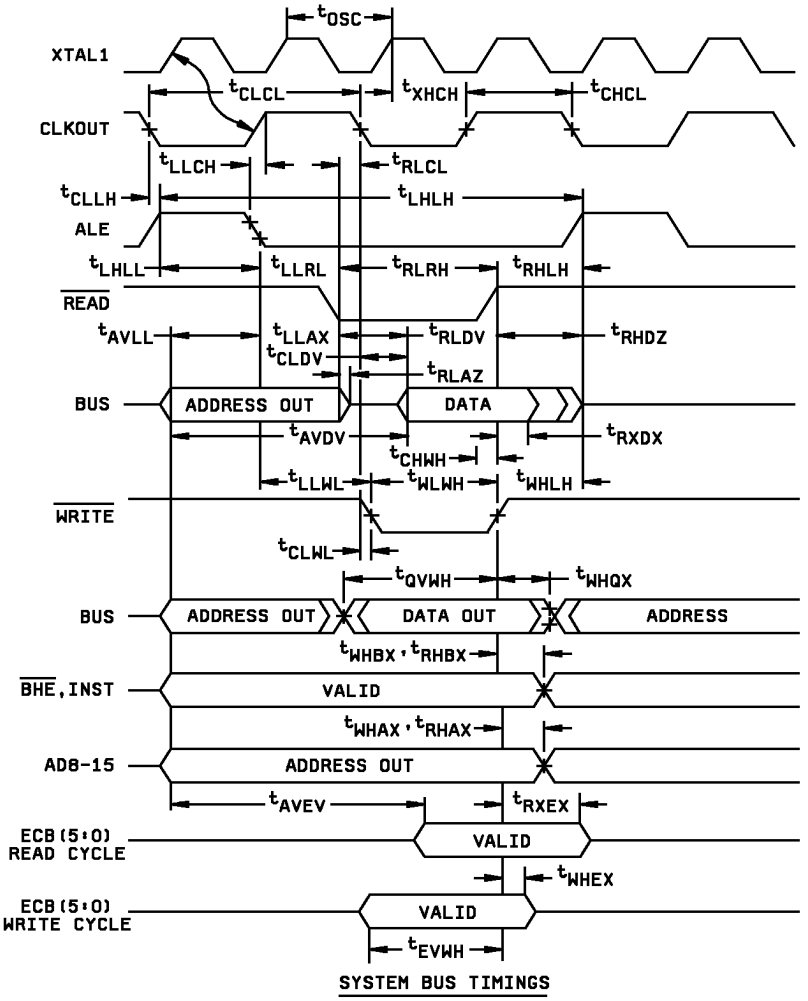


FIGURE 4. Load circuit and waveforms.

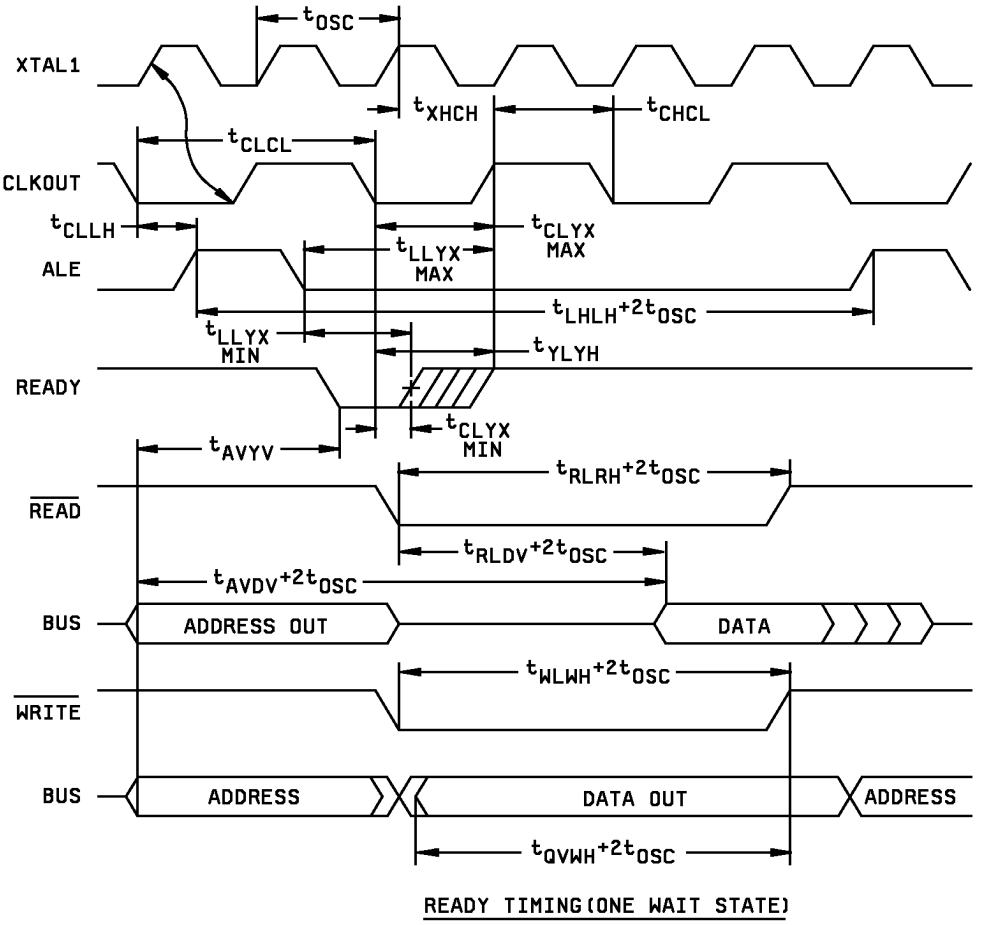
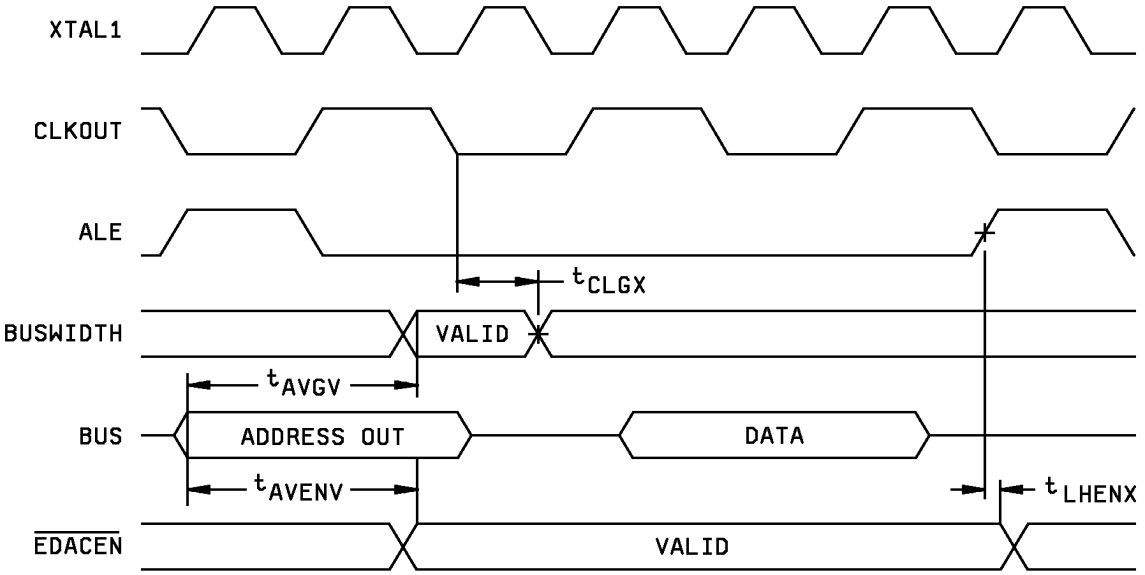
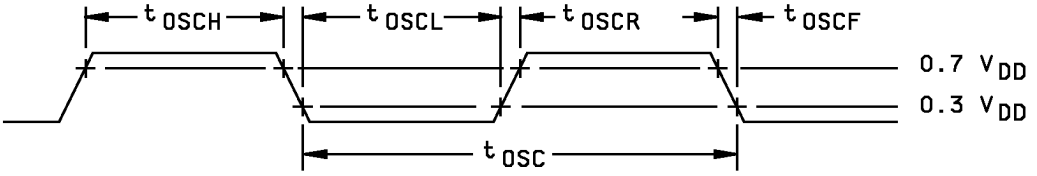


FIGURE 4. Load circuit and waveforms. - Continued



BUSWIDTH AND $\overline{\text{EDACEN}}$ TIMINGS



EXTERNAL CLOCK DRIVE TIMING WAVEFORMS

FIGURE 4. Load circuit and waveforms. - Continued

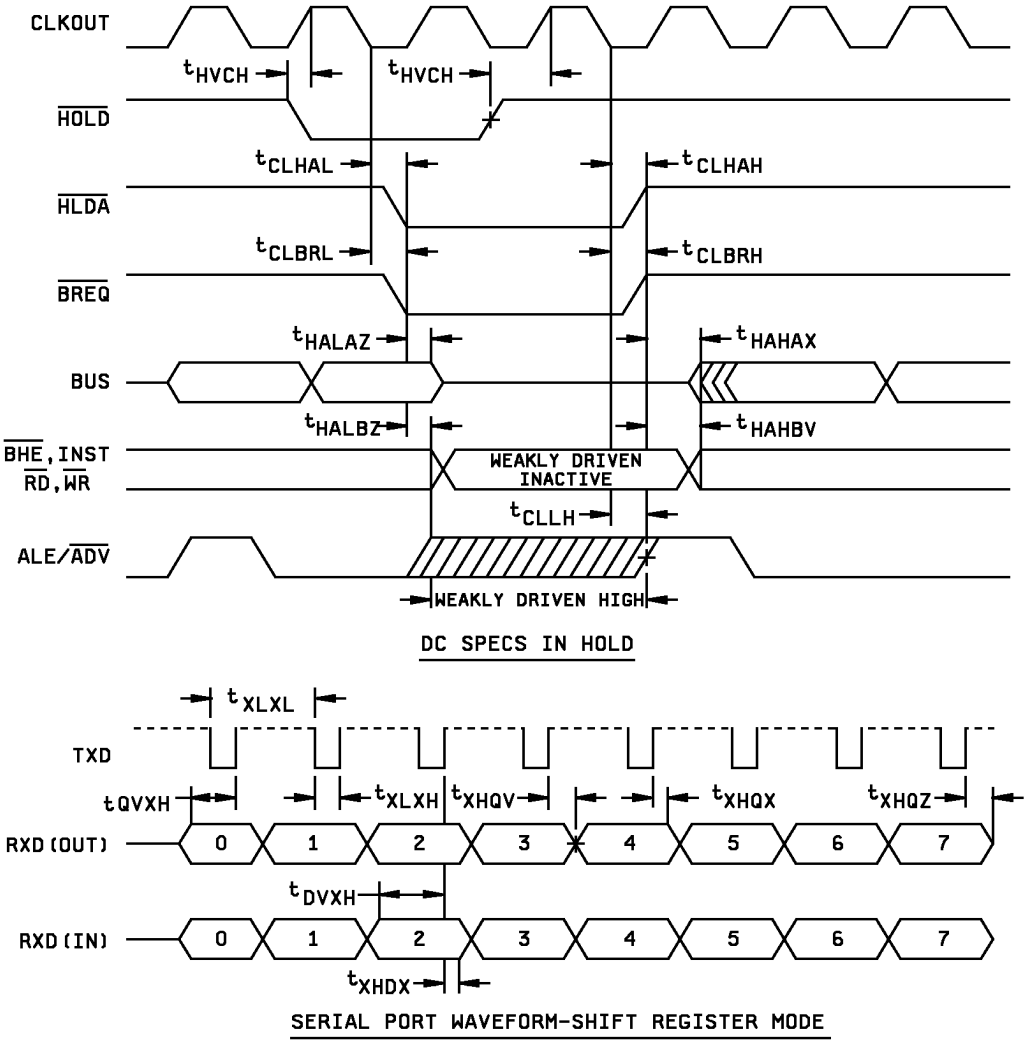
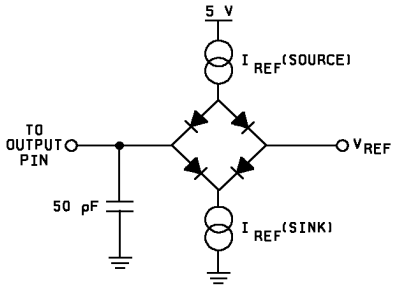
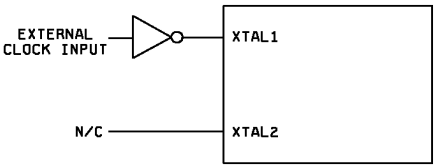


FIGURE 4. Load circuit and waveforms. - Continued

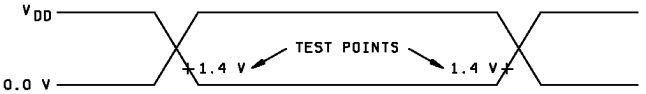


OUTPUT LOADING

NOTE: 50 pF INCLUDES SCOPE PROBE AND TEST SOCKET



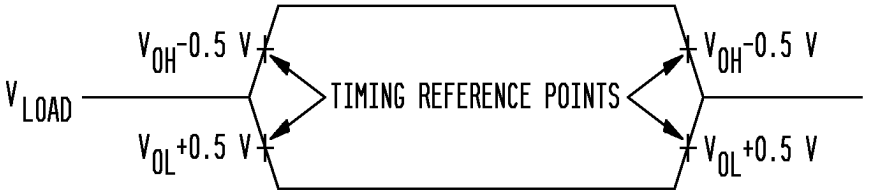
EXTERNAL CLOCK CONNECTIONS



NOTE:
AC Testing inputs are driven at V_{DD} for a Logic "1" and 0.0 V for a Logic "0". Timing measurements on outputs are made at 1.4 V.

AC Testing Input, Output Waveforms.

FIGURE 4. Load circuit and waveforms. - Continued



Float Waveforms

NOTE:
For timing purposes a port pin is no longer floating when it changes to a voltage outside reference points shown, and begins to float when it changes to voltage inside the reference points shown; I_{OL} = 4 mA, I_{OH} = -4 mA .

FIGURE 4. Load circuit and waveforms. - Continued

Open	V_{DD} = 5 V ±0.5V	GND	V_{DD} External Pin	GND External Pin
2,4-8, 17-23, 26-35, 38-41, 45-63, 65,66	9, 11, 16, 24, 37, 43, 64	3, 10, 15, 25, 42, 44, 67	1, 13	12, 14, 36, 68

NOTE: Each pin except those labeled "V_{DD} External Pin" and "GND External Pin" will have a resistor of 2.49KΩ ±5% for irradiation.

FIGURE 5. Radiation exposure circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroup 4 ($C_{I/O}$) shall be measured only for the initial test and after process or design changes which may affect input capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device Class M	Device class Q	Device class V
Interim electrical Parameters (see 4.2)	- - - -	- - - -	- - - -
Final electrical Parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test Requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical Parameters (see 4.4)	1, 2, 7, 8A	1, 2, 7, 8A	1, 2, 7, 8A 3/
Group D end-point electrical Parameters (see 4.4)	1, 2, 7, 8A	1, 2, 7, 8A	1, 2, 7, 8A
Group E end-point electrical Parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in Table IIB herein shall be required when specified and the Delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn-in delta parameters (+25°C).

Parameter	Condition	Limits
Q_{IDD}	T_A = 25°C	±10% of measured value or 20 µA whichever is greater

NOTE: If device is tested at or below 20 µA no deltas are required. Delta's are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125EC, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C " 5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 (condition A) and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accoradance with test method 1021 of MIL-STD-883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 , MIL-HDBK-1331, and Table III herein.

TABLE III. Pin descriptions.

Pin Name	Description
V_{DD}	+5 V Supply voltage
V_{SS}	Circuit ground
PORT 0 (P0.0-P0.7)	Port 0 is an 8-bit input only port when used in its default mode. When configured for their alternate function, five of the bits are bi-directional EDAC check bits as shown in Table A herein.
PORT 1 (P1.0-P1.7)	Port 1 is an 8-bit quasi-bidirectional, I/O port. All pins are quasi-bidirectional unless The alternate function is selected per Table B herein. When the pins are configured for Their alternate functions, they act as standard I/O, not quasi-bidirectional.
PORT 2 (P2.0-P2.7)	Port 2 is an 8-bit, bidirectional, I/O port. These pins are shared with timer 2 Functions, serial data I/O and PWMO output, per Table C herein.
AD0-AD7	The lower 8-bits of the multiplexed address/data bus. The pins on this port are Bidirectional during the data phase of the bus cycle.
AD8-AD15	The upper 8-bits of the multiplexed address/data bus. The pins on this port are Bidirectional during the data phase of the 16 bit bus cycle. When running in 8-bit bus width, these pins are non-multiplexed, dedicated upper address bit outputs.
XTAL1	CMOS level input of the oscillator inverter.
XTAL2	Not used. Driven low by the device.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is one-half the Oscillator frequency.
$\overline{\text{RESET}}$	Active low reset input and open drain output.
BUSWIDTH	Input for the BUSWIDTH selection. If the Chip Configuration Register (CCR) bit 1 Is a logic high, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If the BUSWIDTH is a 0, an 8-bit Cycle occurs. If the CCR bit 1 is a logic low, then the bus is always an 8-bit bus.
NMI	A positive transition causes a non-maskable interrupt vector through 203EH.
INST	Output high during an external memory read indicates the read is a "fetch Instruction". INST is valid throughout the bus cycle. INST is only activated during External memory access and output low for a data fetch.
$\overline{\text{EDACEN}}$	$\overline{\text{EDACEN}}$ is an enable input for the error detection and correction functions.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin Options provide a signal to demultiplex the address from the address /data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive, high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ Is only activated during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is only activated during external Memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. When Selected by the CCR, $\overline{\text{WR}}$ will go low for every external write. However $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is only selected for external memory writes.

TABLE III Pin descriptions – Continued.

Pin Name	Description
$\overline{BHE}/\overline{WRH}$	Byte High Enable or Write High output to external memory, as selected by the CCR. When the $\overline{BHE}$ is selected, a logic low value selects the bank of memory That is connected to the high byte of the data bus, When the $\overline{WRH}$ function Is selected, the pin will go low if the bus cycle is writing to an odd memory location. When the CCR selects 8-bit BUSWIDTH mode, $\overline{WRH}$ is asserted for writes to all External memory locations.
READY	READY is the input used to lengthen external memory cycles for interfacing to Slow memory. A logic low value will place wait states in the memory cycle.
HIS	Inputs to the High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HIS.2 And HIS.3. Two of these pins (HSI.2 and HSI.3) are shared with the HSO Unit. Two of these pins(HSI.0 and HSI.1) have alternate functions for Timer 2.
HSO	Outputs from the High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Pins HSO.4 and HSO.5 are shared With pins HSI.2 and HSI.3 of the HSI Unit respectively.

TABLE A. PORT 0 ALTERNATE FUNCTIONS

Port pin	Alternate Name	Alternate Function
P0.0-P0.3, P0.6	ECB0-ECB4	Error detection and correction check bits.
P0.4, P0.5	P0.4, P0.5	Input port pin.
P0.7	EXTINT	Setting IOC1.1 = 1 will allow P0.7 to be used for EXTINT (INT07).

TABLE B. PORT 1 ALTERNATE FUNCTIONS

P1.0	P1.0	I/O Pin
P1.1	P1.1	I/O Pin
P1.2	P1.2	I/O Pin
P1.3	PWM1	Setting IOC3.2 = 1enables P1.3 as the Pulse Width Modulator (PWM1) output pin.
P1.4	PWM2	Setting IOC3.3 = 1enables P1.4 as the Pulse Width Modulator (PWM2) output pin.
P1.5	$\overline{BREQ}$	Bus Request, output activated when the bus controller has a pending external memory Cycle.
P1.6	$\overline{HLDA}$	Bus Hold Acknowledge, output indicating the release of the bus.
P1.7	$\overline{HOLD}$	Bus Hold, input requesting control of the bus.

TABLE III. Pin descriptions – Continued.

TABLE C. PORT 2 ALTERNATE FUNCTIONS

Port Pin	Alternate Name	Alternate Function
P2.0	TXD	Transmit Serial Data.
P2.1	RXD	Receive Serial Data.
P2.2	EXTINT	External interrupt, Clearing IOC1.1 will allow P2.2 to be used for EXTINT (INT07).
P2.3	T2CLK	Timer 2 clock input and Serial port baud rate generator input.
P2.4	T2RST	Timer 2 Reset.
P2.5	PWMO	Pulse Width Modulator output 0.
P2.6	T2UP-DN	Controls the direction of the Timer 2 counter. Logic High equals count down. Logic Low equals count up.
P2.7	T2CAPTURE	A rising edge on P2.7 causes the value of Timer 2 to be captured into this register, And generates a Timer 2 Capture interrupt (INT11).

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-03-05

Approved sources of supply for SMD 5962-98583 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard Microcircuit drawing PIN 1/	Vendor CAGE Number	Vendor Similar PIN 2/
5962R9858301QXA	65342	UT80CRH196KD-WCA
5962R9858301QXC	65342	UT80CRH196KD-WCC
5962R9858301VXA	65342	UT80CRH196KD-WCA
5962R9858301VXC	65342	UT80CRH196KD-WCC
5962-9858301QXA	65342	UT80C196KD-WCA
5962-9858301QXC	65342	UT80C196KD-WCC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronic Systems Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.