



## M68AR128ML

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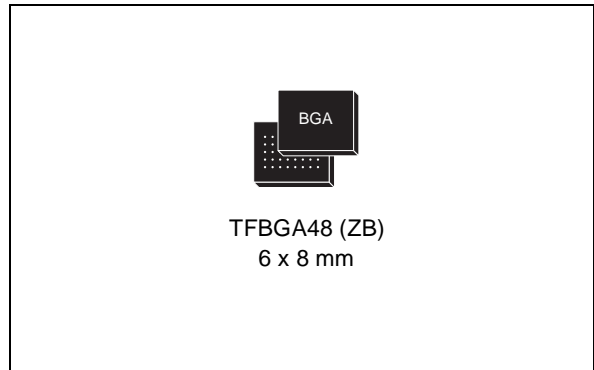
### 2 Mbit (128K x16) 1.8V Asynchronous SRAM

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#### FEATURES SUMMARY

- SUPPLY VOLTAGE: 1.65 to 1.95V
- 128K x 16 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIME: 55ns
- SINGLE BYTE READ/WRITE
- LOW STANDBY CURRENT
- LOW  $V_{CC}$  DATA RETENTION: 1.0V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN

Figure 1. Packages



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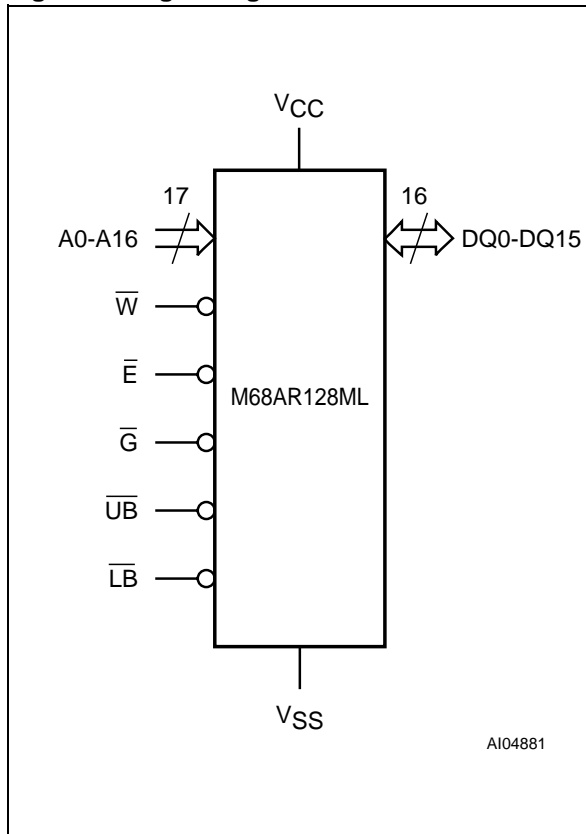
**SUMMARY DESCRIPTION**

The M68AR128ML is a 2 Mbit (2,097,152 bit) CMOS SRAM, organized as 131,072 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 1.8V ( $\pm 150\text{mV}$ ) supply. This device has an

automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AR128ML is available in TFBGA48 (0.75 mm pitch) package.

**Figure 2. Logic Diagram**



**Table 1. Signal Names**

A0-A16	Address Inputs
DQ0-DQ15	Data Input/Output
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{W}$	Write Enable
$\bar{UB}$	Upper Byte Enable Input
$\bar{LB}$	Lower Byte Enable Input
Vcc	Supply Voltage
Vss	Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Figure 3. TFBGA Connections (Top view through package)

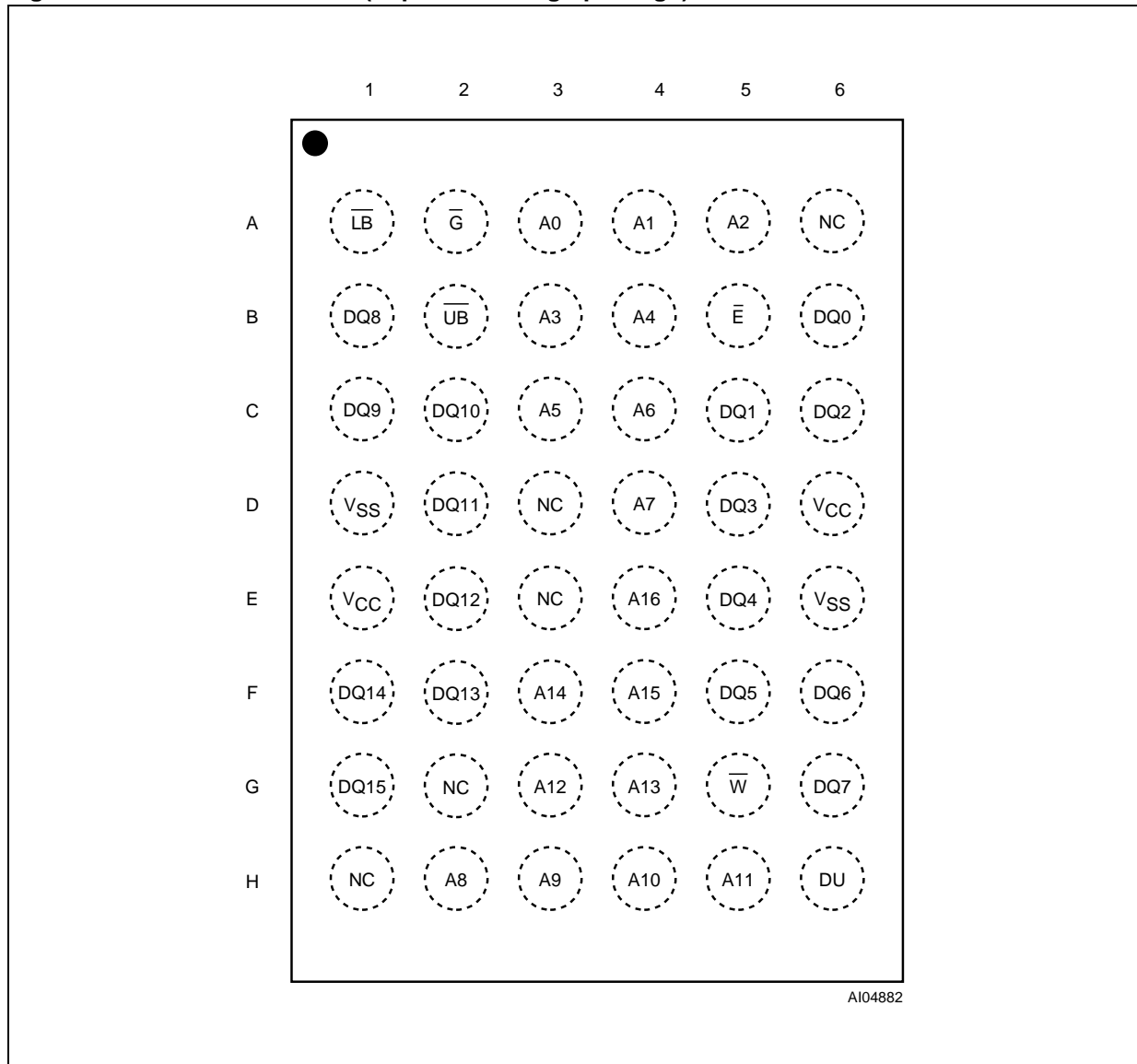
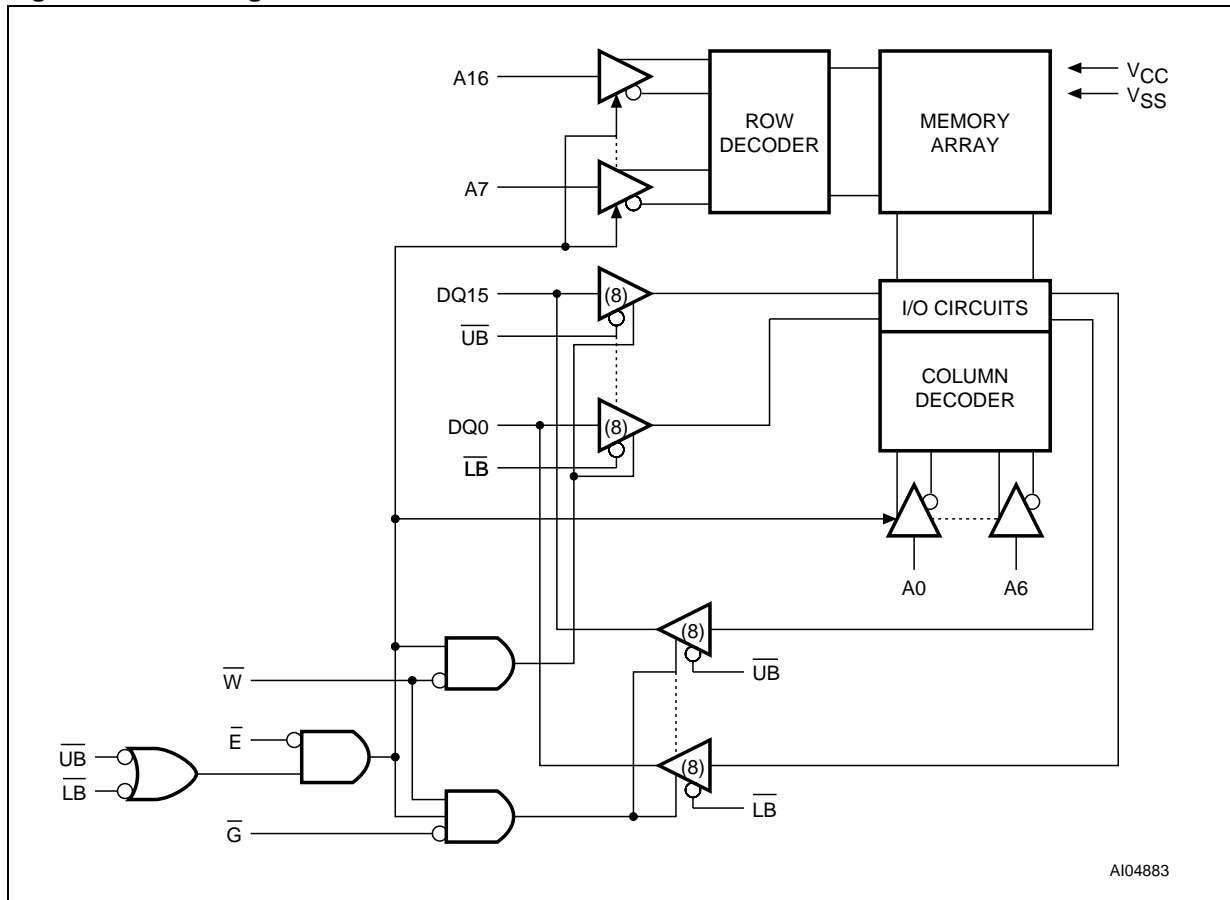


Figure 4. Block Diagram



### MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$I_O^{(1)}$	Output Current	20	mA
$T_A$	Ambient Operating Temperature	-55 to 125	°C
$T_{STG}$	Storage Temperature	-65 to 150	°C
$V_{CC}$	Supply Voltage	-0.5 to 2.5	V
$V_{IO}^{(2)}$	Input or Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$P_D$	Power Dissipation	1	W

Note: 1. One output at a time, not to exceed 1 second duration.

2. Up to a maximum operating  $V_{CC}$  of 1.95V only.

**DC AND AC PARAMETERS**

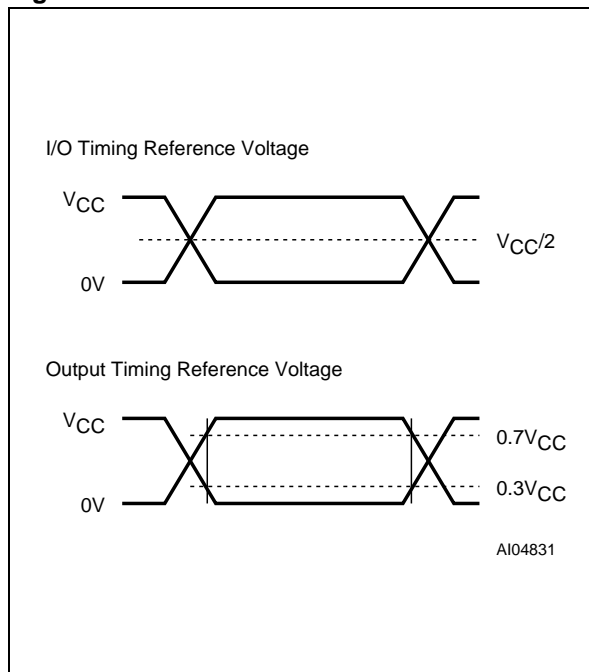
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 3. Operating and AC Measurement Conditions**

Parameter		M68AR128ML
V <sub>CC</sub> Supply Voltage		1.65 to 1.95V
Ambient Operating Temperature	Range 1	0 to 70°C
	Range 6	-40 to 85°C
Load Capacitance (C <sub>L</sub> )		30pF
Output Circuit Protection Resistance (R <sub>1</sub> )		15.3kΩ
Load Resistance (R <sub>2</sub> )		11.3kΩ
Input Rise and Fall Times		1ns/V
Input Pulse Voltages		0 to V <sub>CC</sub>
Input and Output Timing Ref. Voltages		V <sub>CC</sub> /2
Output Transition Timing Ref. Voltages		V <sub>RL</sub> = 0.3V <sub>CC</sub> ; V <sub>RH</sub> = 0.7V <sub>CC</sub>

**Figure 5. AC Measurement I/O Waveform**



**Figure 6. AC Measurement Load Circuit**

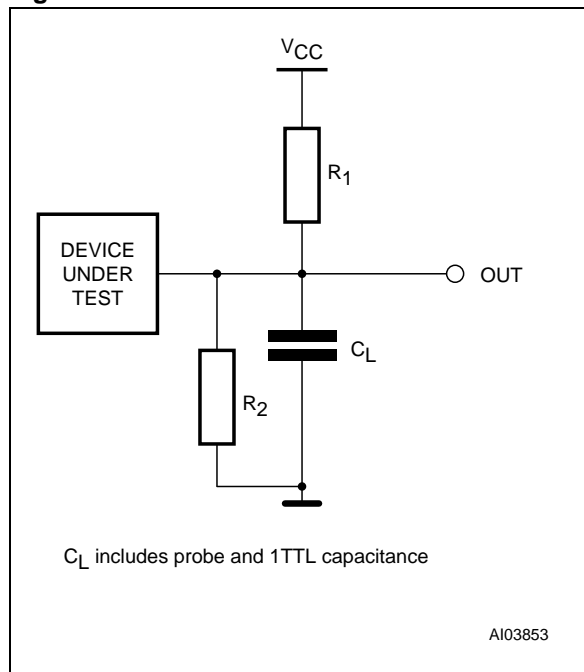


Table 4. Capacitance

Symbol	Parameter <sup>(1,2)</sup>	Test Condition	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance on all pins (except DQ)	V <sub>IN</sub> = 0V		6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V		8	pF

Note: 1. Sampled only, not 100% tested.  
2. At T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 1.8V.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I <sub>CC1</sub> <sup>(1,2)</sup>	Operating Supply Current	V <sub>CC</sub> = 1.95V, f = 1/t <sub>AVAV</sub> , I <sub>OUT</sub> = 0mA		2	6	mA
I <sub>CC2</sub> <sup>(3)</sup>	Operating Supply Current	V <sub>CC</sub> = 1.95V, f = 1MHz, I <sub>OUT</sub> = 0mA		1	2	mA
I <sub>LI</sub>	Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1		1	μA
I <sub>LO</sub> <sup>(4)</sup>	Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> <sup>(3)</sup>	-1		1	μA
I <sub>SB</sub>	Standby Supply Current CMOS	V <sub>CC</sub> = 1.95V, $\overline{E} \geq V_{CC} - 0.2V$ or $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$ , f = 0		0.5	4	μA
V <sub>IH</sub>	Input High Voltage		1.4		V <sub>CC</sub> + 0.4	V
V <sub>IL</sub>	Input Low Voltage		-0.5		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100μA	1.5			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 100μA			0.2	V

Note: 1. Average AC current, cycling at t<sub>AVAV</sub> minimum.  
2.  $\overline{E} = V_{IL}$ ,  $\overline{LB}$  or/and  $\overline{UB} = V_{IL}$ , V<sub>IN</sub> = V<sub>IL</sub> or V<sub>IH</sub>.  
3.  $\overline{E} \leq 0.2V$ ,  $\overline{LB}$  or/and  $\overline{UB} \leq 0.2V$ , V<sub>IN</sub> ≤ 0.2V or V<sub>IN</sub> ≥ V<sub>CC</sub> - 0.2V.  
4. Output disabled.

**OPERATION**

The M68AR128ML has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ( $\overline{E}$  = High) or LB and UB are de-asserted (LB and UB = High). An Output Enable ( $\overline{G}$ ) signal provides

a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs  $\overline{W}$ ,  $\overline{E}$ ,  $\overline{LB}$  and  $\overline{UB}$  as summarized in the Operating Modes table (see Table 6).

**Table 6. Operating Modes**

Operation	$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Deselected	$V_{IH}$	X	X	X	X	Hi-Z	Hi-Z	Standby ( $I_{SB}$ )
Deselected	X	X	X	$V_{IH}$	$V_{IH}$	Hi-Z	Hi-Z	Standby ( $I_{SB}$ )
Lower Byte Read	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	Data Output	Hi-Z	Active ( $I_{CC}$ )
Lower Byte Write	$V_{IL}$	$V_{IL}$	X	$V_{IL}$	$V_{IH}$	Data Input	Hi-Z	Active ( $I_{CC}$ )
Output Disabled	$V_{IL}$	$V_{IH}$	$V_{IH}$	X	X	Hi-Z	Hi-Z	Active ( $I_{CC}$ )
Upper Byte Read	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	Hi-Z	Data Output	Active ( $I_{CC}$ )
Upper Byte Write	$V_{IL}$	$V_{IL}$	X	$V_{IH}$	$V_{IL}$	Hi-Z	Data Input	Active ( $I_{CC}$ )
Word Read	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IL}$	Data Output	Data Output	Active ( $I_{CC}$ )
Word Write	$V_{IL}$	$V_{IL}$	X	$V_{IL}$	$V_{IL}$	Data Input	Data Input	Active ( $I_{CC}$ )

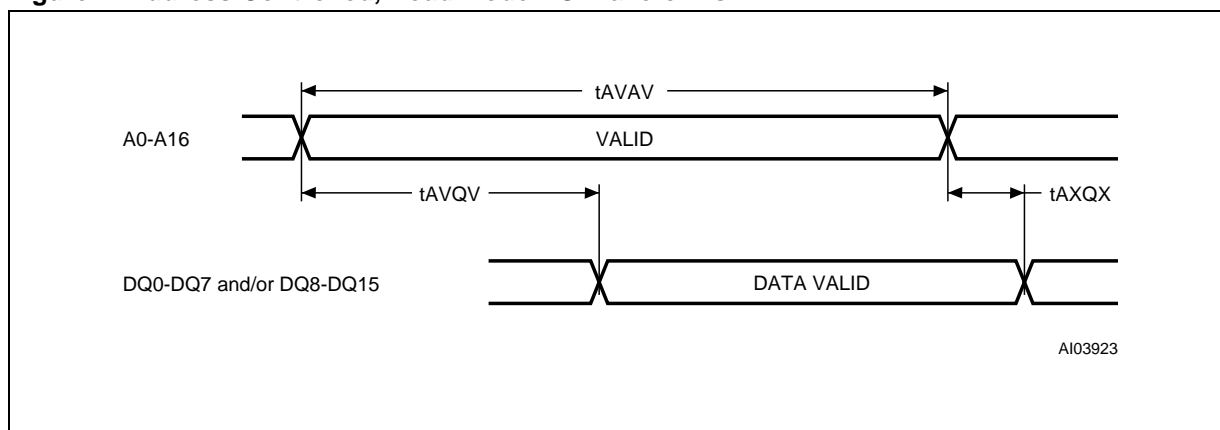
Note: 1. X =  $V_{IH}$  or  $V_{IL}$ .

**Read Mode**

The M68AR128ML is in the Read mode whenever Write Enable ( $\overline{W}$ ) is High with Output Enable ( $\overline{G}$ ) Low, and Chip Enables ( $\overline{E}$ ) is asserted. This provides access to data from eight or sixteen, depending on the status of the signal UB and LB, of the 2,097,152 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight or sixteen output pins

within  $t_{AVQV}$  after the last stable address, providing  $\overline{G}$  is Low and  $\overline{E}$  is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter ( $t_{ELQV}$ ,  $t_{GLQV}$  or  $t_{BLQV}$ ) rather than the address. Data out may be indeterminate at  $t_{ELQX}$ ,  $t_{BLQX}$  and  $t_{GLQX}$ , but data lines will always be valid at  $t_{AVQV}$ .

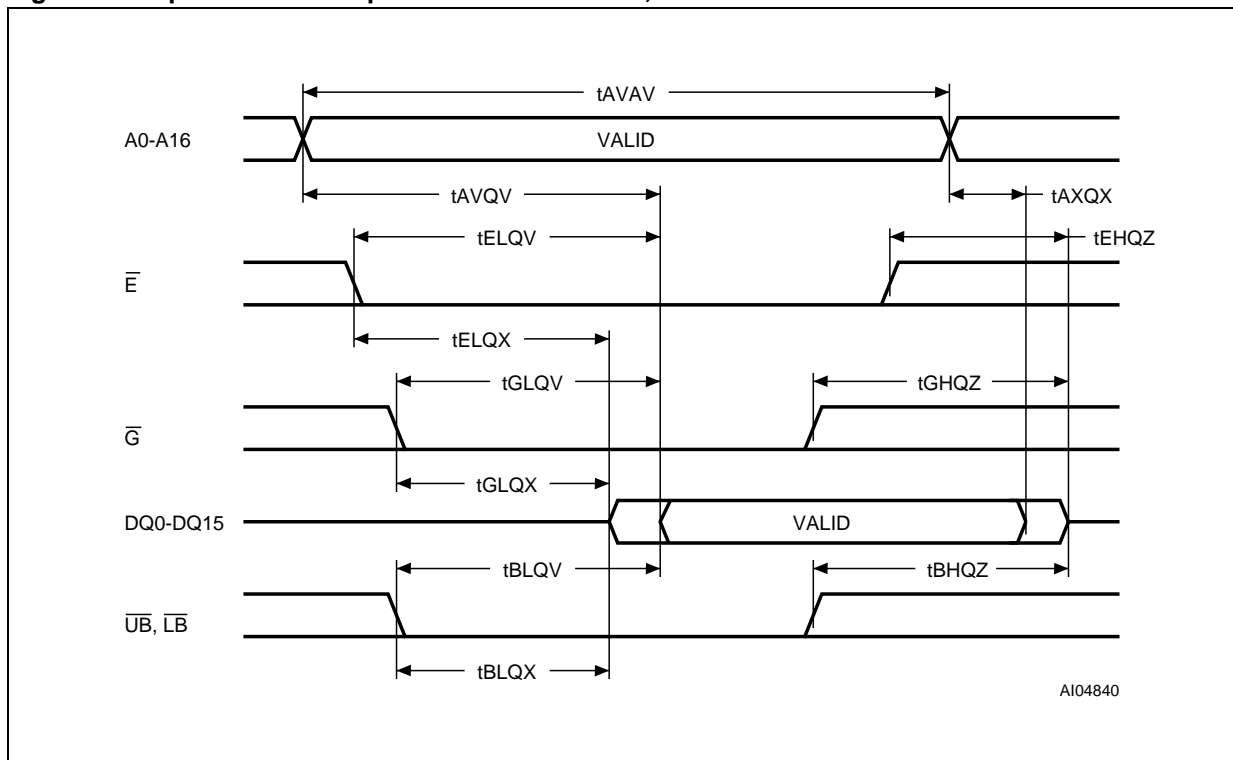
**Figure 7. Address Controlled, Read Mode AC Waveforms**



Note:  $\overline{E}$  = Low,  $\overline{G}$  = Low,  $\overline{W}$  = High,  $\overline{UB}$  = Low and/or  $\overline{LB}$  = Low.

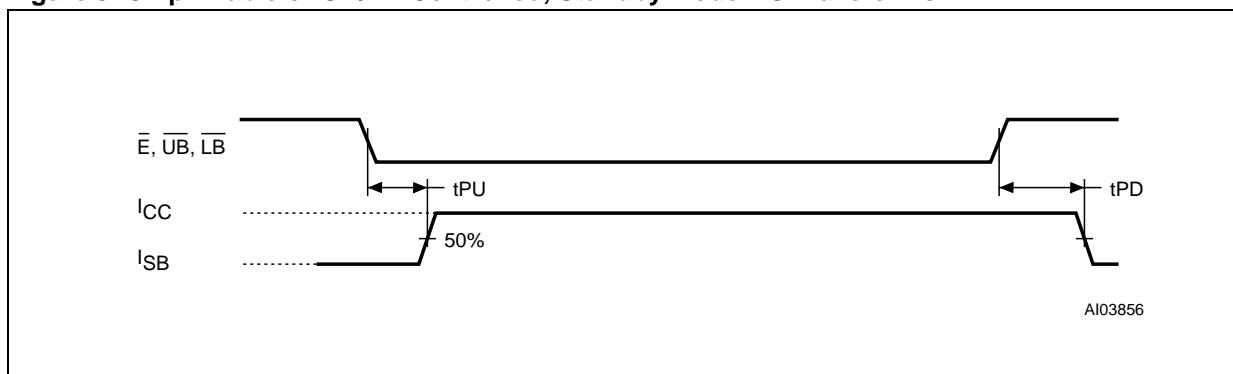


Figure 8. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: Write Enable ( $\bar{W}$ ) = High.

Figure 9. Chip Enable or  $\bar{UB}/\bar{LB}$  Controlled, Standby Mode AC Waveforms



**Table 7. Read and Standby Mode AC Characteristics**

Symbol	Parameter		M68AR128ML		Unit
			55	70	
t <sub>AVAV</sub>	Read Cycle Time	Min	55	70	ns
t <sub>AVQV</sub>	Address Valid to Output Valid	Max	55	70	ns
t <sub>AXQX</sub> <sup>(1)</sup>	Data hold from address change	Min	5	5	ns
t <sub>BHQZ</sub> <sup>(2,3)</sup>	Upper/Lower Byte Enable High to Output Hi-Z	Max	20	25	ns
t <sub>BLQV</sub>	Upper/Lower Byte Enable Low to Output Valid	Max	55	70	ns
t <sub>BLQX</sub> <sup>(1)</sup>	Upper/Lower Byte Enable Low to Output Transition	Min	5	5	ns
t <sub>EHQZ</sub> <sup>(2,3)</sup>	Chip Enable High to Output Hi-Z	Max	20	25	ns
t <sub>ELQV</sub>	Chip Enable Low to Output Valid	Max	55	70	ns
t <sub>ELQX</sub> <sup>(1)</sup>	Chip Enable Low to Output Transition	Min	5	5	ns
t <sub>GHQZ</sub> <sup>(2,3)</sup>	Output Enable High to Output Hi-Z	Max	20	25	ns
t <sub>GLQV</sub>	Output Enable Low to Output Valid	Max	25	35	ns
t <sub>GLQX</sub> <sup>(2)</sup>	Output Enable Low to Output Transition	Min	5	5	ns
t <sub>PD</sub> <sup>(4)</sup>	Chip Enable or $\overline{UB}/\overline{LB}$ High to Power Down	Max	0	0	ns
t <sub>PU</sub> <sup>(4)</sup>	Chip Enable or $\overline{UB}/\overline{LB}$ Low to Power Up	Min	55	70	ns

- Note: 1. Test conditions assume transition timing reference level = 0.3V<sub>CC</sub> or 0.7V<sub>CC</sub>.  
 2. At any given temperature and voltage condition, t<sub>GHQZ</sub> is less than t<sub>GLQX</sub>, t<sub>BHQZ</sub> is less than t<sub>BLQX</sub> and t<sub>EHQZ</sub> is less than t<sub>ELQX</sub> for any given device.  
 3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.  
 4. Tested initially and after any design or process changes that may affect these parameters.

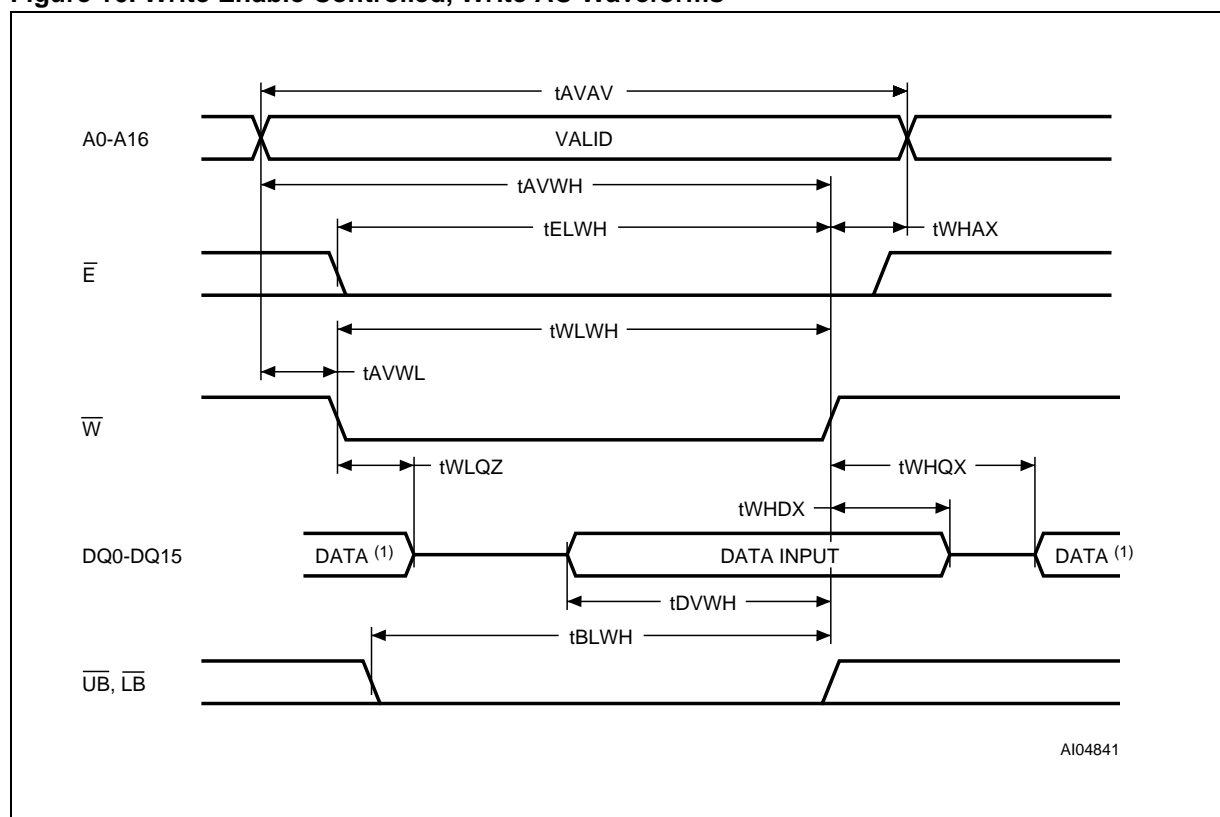
### Write Mode

The M68AR128ML is in the Write mode whenever the  $\overline{W}$  and  $\overline{E}$  are Low. Either the Chip Enable input ( $\overline{E}$ ) or the Write Enable input ( $\overline{W}$ ) must be deasserted during Address transitions for subsequent write cycles. When  $\overline{E}$  ( $\overline{W}$ ) is Low, and  $\overline{UB}$  or  $\overline{LB}$  is Low, write cycle begins on the  $\overline{W}$  ( $\overline{E}$ )'s falling edge. When  $\overline{E}$  and  $\overline{W}$  are Low, and  $\overline{UB} = \overline{LB} = \text{High}$ , write cycle begins on the first falling edge of  $\overline{UB}$  or  $\overline{LB}$ . Therefore, address setup time is referenced to Write Enable, Chip Enable or  $\overline{UB}/\overline{LB}$  as  $t_{AVWL}$ ,  $t_{AVEL}$  and  $t_{AVBL}$  respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of  $\overline{E}$ ,  $\overline{W}$  or  $\overline{UB}/\overline{LB}$ .

If the Output is enabled ( $\overline{E} = \text{Low}$ ,  $\overline{G} = \text{Low}$ ,  $\overline{LB}$  or  $\overline{UB} = \text{Low}$ ), then  $\overline{W}$  will return the outputs to high impedance within  $t_{WLQZ}$  of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for  $t_{DVWH}$  before the rising edge of Write Enable, or for  $t_{DVH}$  before the rising edge of  $\overline{UB}/\overline{LB}$  whichever occurs first, and remain valid for  $t_{WHDX}$ ,  $t_{EHDX}$  and  $t_{BHDX}$  respectively.

Figure 10. Write Enable Controlled, Write AC Waveforms



Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Figure 11. Chip Enable Controlled, Write AC Waveforms

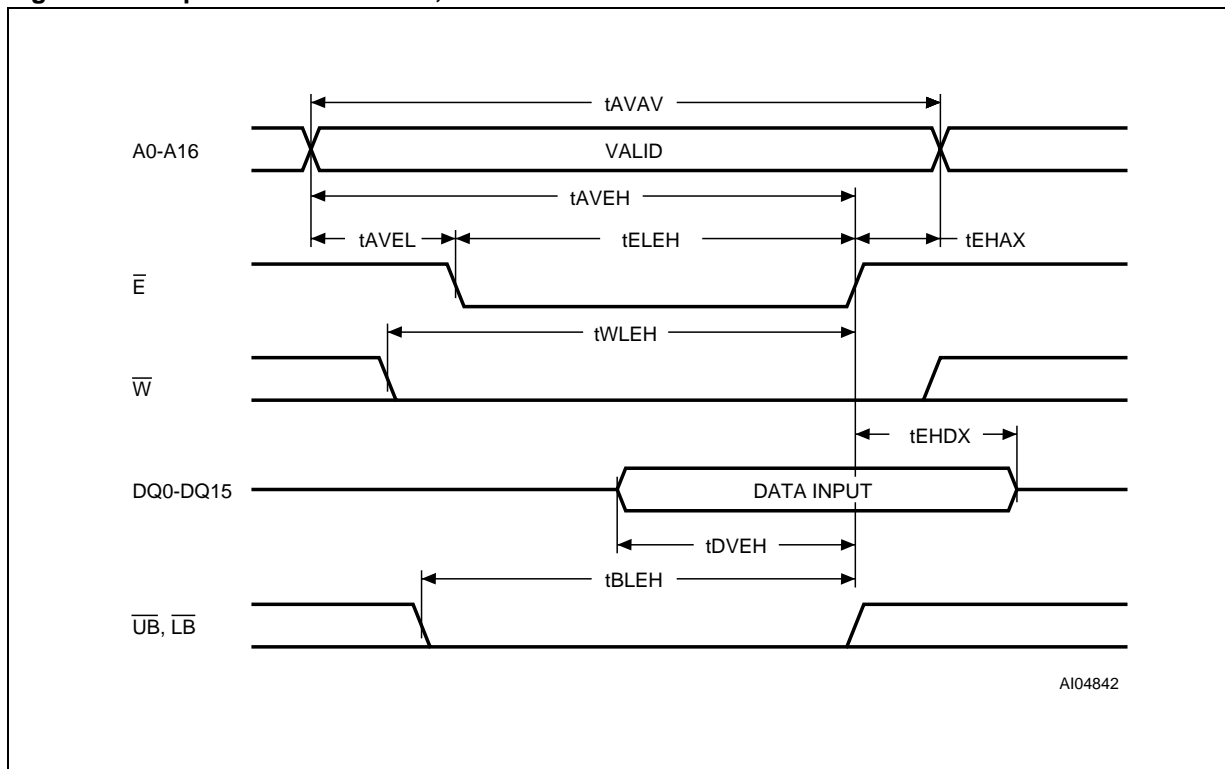
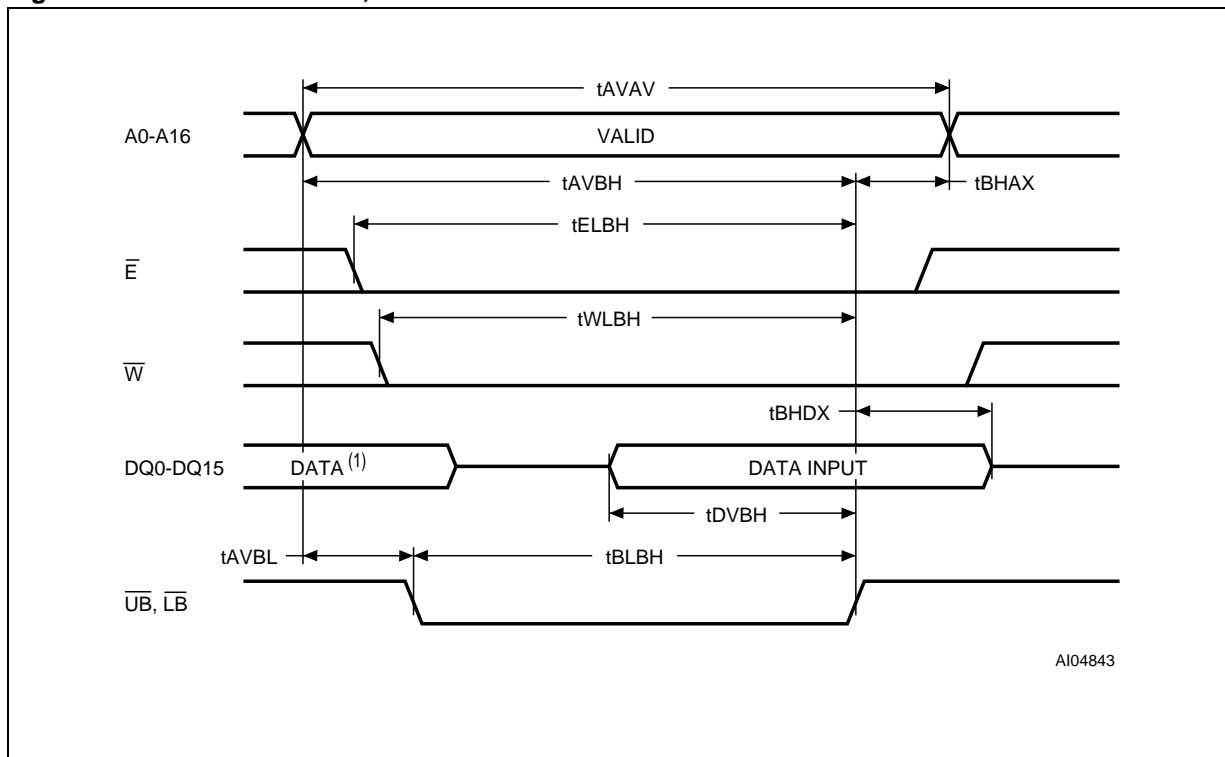


Figure 12.  $\bar{UB}/\bar{LB}$  Controlled, Write AC Waveforms



Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Table 8. Write Mode AC Characteristics

Symbol	Parameter		M68AR128ML		Unit
			55	70	
t <sub>AVAV</sub>	Write Cycle Time	Min	55	70	ns
t <sub>AVBH</sub>	Address Valid to $\overline{LB}$ , $\overline{UB}$ High	Min	45	60	ns
t <sub>AVBL</sub>	Address Valid to $\overline{LB}$ , $\overline{UB}$ Low	Min	0	0	ns
t <sub>AVEH</sub>	Address Valid to Chip Enable High	Min	45	60	ns
t <sub>AVEL</sub>	Address valid to Chip Enable Low	Min	0	0	ns
t <sub>AVWH</sub>	Address Valid to Write Enable High	Min	45	60	ns
t <sub>AVWL</sub>	Address Valid to Write Enable Low	Min	0	0	ns
t <sub>BHAX</sub>	$\overline{LB}$ , $\overline{UB}$ High to Address Transition	Min	0	0	ns
t <sub>BHDX</sub>	$\overline{LB}$ , $\overline{UB}$ High to Input Transition	Min	0	0	ns
t <sub>BLBH</sub>	$\overline{LB}$ , $\overline{UB}$ Low to $\overline{LB}$ , $\overline{UB}$ High	Min	45	60	ns
t <sub>BLEH</sub>	$\overline{LB}$ , $\overline{UB}$ Low to Chip Enable High	Min	45	60	ns
t <sub>BLWH</sub>	$\overline{LB}$ , $\overline{UB}$ Low to Write Enable High	Min	45	60	ns
t <sub>DVBH</sub>	Input Valid to $\overline{LB}$ , $\overline{UB}$ High	Min	25	30	ns
t <sub>DVEH</sub>	Input Valid to Chip Enable High	Min	25	30	ns
t <sub>DVWH</sub>	Input Valid to Write Enable High	Min	25	30	ns
t <sub>EHAX</sub>	Chip Enable High to Address Transition	Min	0	0	ns
t <sub>EHDX</sub>	Chip enable High to Input Transition	Min	0	0	ns
t <sub>ELBH</sub>	Chip Enable Low to $\overline{LB}$ , $\overline{UB}$ High	Min	45	60	ns
t <sub>ELEH</sub>	Chip Enable Low to Chip Enable High	Min	45	60	ns
t <sub>ELWH</sub>	Chip Enable Low to Write Enable High	Min	45	60	ns
t <sub>WHAX</sub>	Write Enable High to Address Transition	Min	0	0	ns
t <sub>WHDX</sub>	Write Enable High to Input Transition	Min	0	0	ns
t <sub>WHQX</sub> <sup>(1)</sup>	Write Enable High to Output Transition	Min	5	5	ns
t <sub>WLBH</sub>	Write Enable Low to $\overline{LB}$ , $\overline{UB}$ High	Min	45	60	ns
t <sub>WLEH</sub>	Write Enable Low to Chip Enable High	Min	45	60	ns
t <sub>WLQZ</sub> <sup>(1,2)</sup>	Write Enable Low to Output Hi-Z	Max	20	20	ns
t <sub>WLWH</sub>	Write Enable Low to Write Enable High	Min	45	60	ns

Note: 1. At any given temperature and voltage condition, t<sub>WLQZ</sub> is less than t<sub>WHQX</sub> for any given device.

2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 13. Low V<sub>CC</sub> Data Retention AC Waveforms

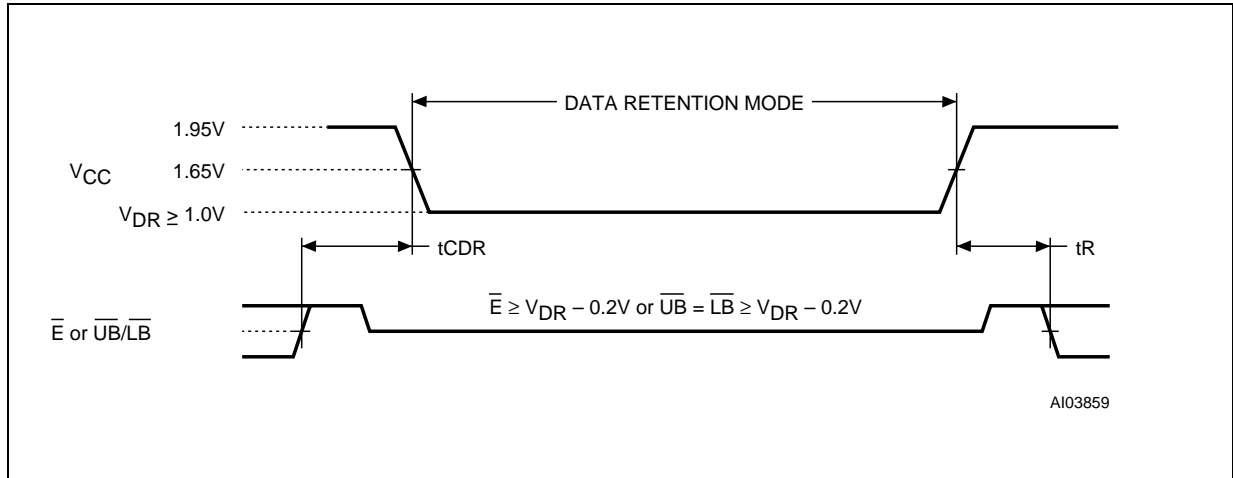


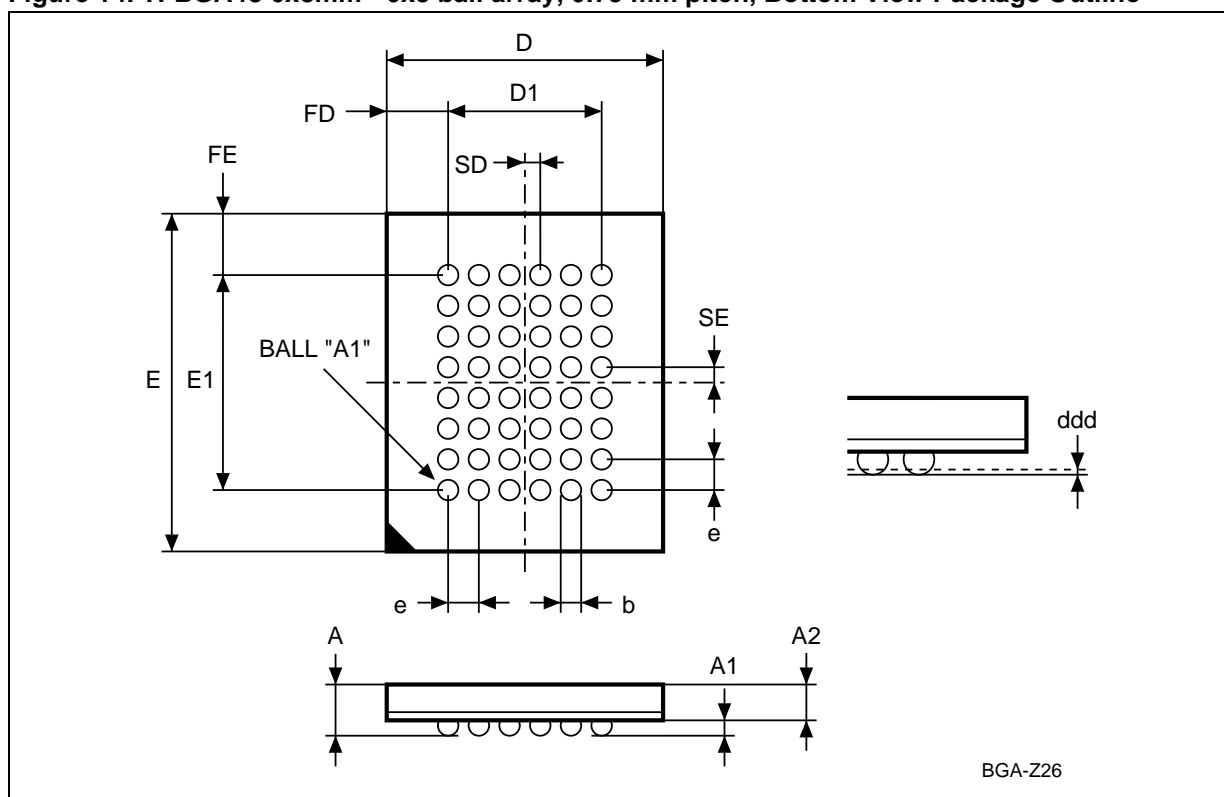
Table 9. Low V<sub>CC</sub> Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I <sub>CCDR</sub> <sup>(1)</sup>	Supply Current (Data Retention)	V <sub>CC</sub> = 1.0V, $\bar{E} \geq V_{CC} - 0.2V$ or $\bar{UB} = \bar{LB} \geq V_{CC} - 0.2V$ , f = 0 <sup>(3)</sup>		0.5	2	μA
t <sub>CDR</sub> <sup>(1,2)</sup>	Chip Deselected to Data Retention Time		0			ns
t <sub>R</sub> <sup>(2)</sup>	Operation Recovery Time		t <sub>AVAV</sub>			ns
V <sub>DR</sub> <sup>(1)</sup>	Supply Voltage (Data Retention)	$\bar{E} \geq V_{CC} - 0.2V$ or $\bar{UB} = \bar{LB} \geq V_{CC} - 0.2V$ , f = 0	1.0			V

Note: 1. All other Inputs at V<sub>IH</sub> ≥ V<sub>CC</sub> - 0.2V or V<sub>IL</sub> ≤ 0.2V.  
 2. Tested initially and after any design or process changes that may affect these parameters. t<sub>AVAV</sub> is Read cycle time.  
 3. No input may exceed V<sub>CC</sub> + 0.2V.

## PACKAGE MECHANICAL

Figure 14. TFBGA48 6x8mm - 6x8 ball array, 0.75 mm pitch, Bottom View Package Outline



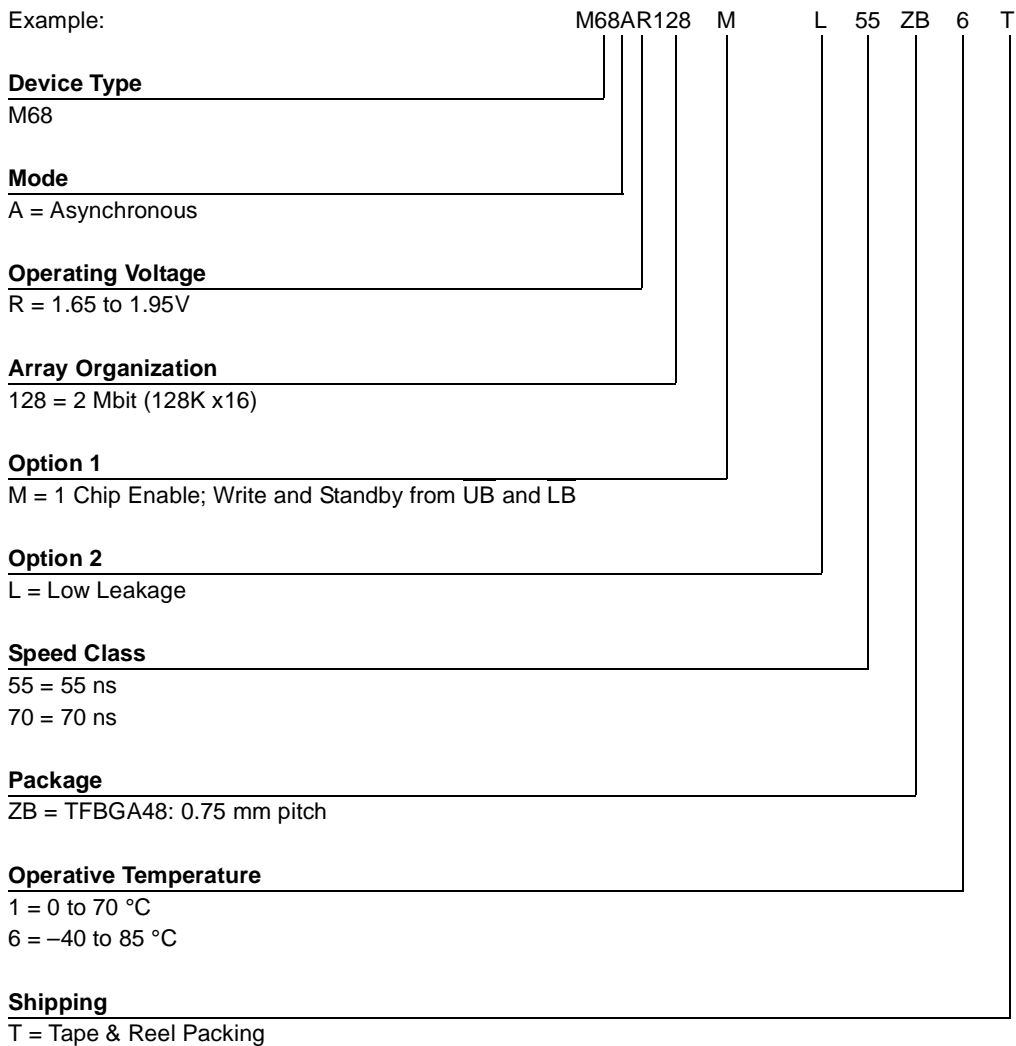
Note: Drawing is not to scale.

Table 10. TFBGA48 6x8mm - 6x8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	1.125	–	–	0.0443	–	–
FE	1.375	–	–	0.0541	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

**PART NUMBERING**

**Table 11. Ordering Information Scheme**



Note: 1. Package option available on request. Please contact STMicroelectronics local Sales Office.

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.



**REVISION HISTORY****Table 12. Document Revision History**

<b>Date</b>	<b>Version</b>	<b>Revision Details</b>
July 2001	-01	First Issue
05-Mar-2002	-02	tAXQX, tBLQX, tELQX clarified in Read and Standby Mode AC Characteristics table (Table 7)
14-May-2002	-03	Document globally revised

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