AKD5702-A
AK5702 Evaluation Board Rev.1

GENERAL DESCRIPTION

AKD5702-A is an evaluation board for the portable digital audio 16bit A/D converter with MIC-AMP, AK5702. AKD5702-A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD5702-A --- AK5702 Evaluation Board
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT with optical output**
- **BNC connector for an external clock input**
- **10pin Header for serial control interface**

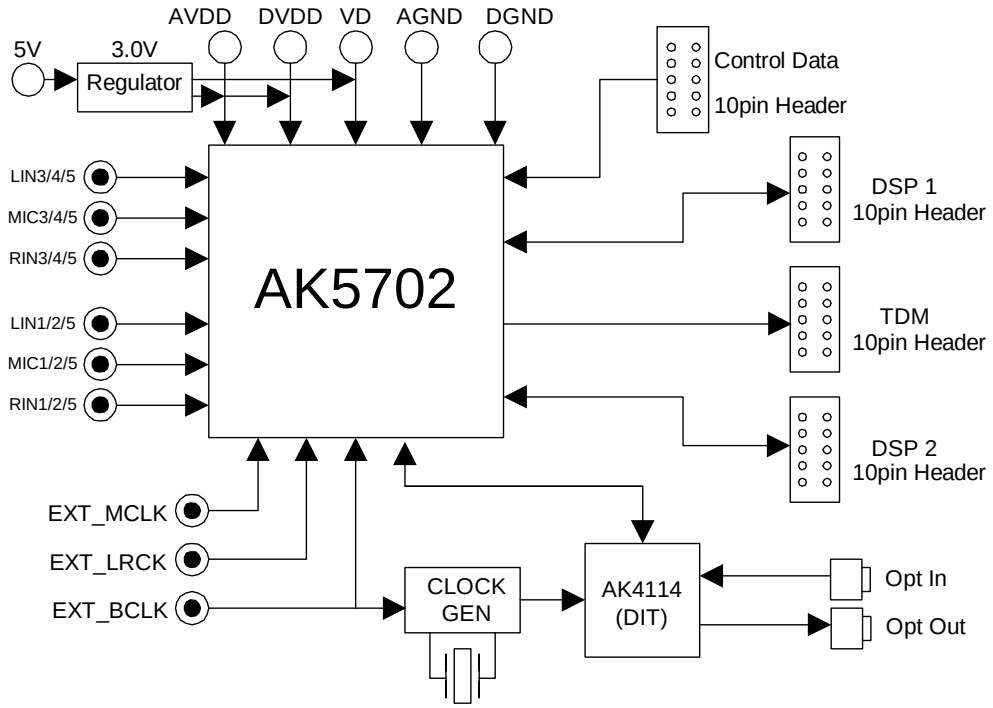


Figure 1. AKD5702-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

1-1) When AVDD, DVDD and VD are supplied from the regulator. (Default)

[REG]	(Red)	= 5V
[AVDD]	(Orange)	= open (3.0V, supply from regulator, for AVDD of AK5702)
[DVDD]	(Orange)	= open (3.0V, supply from regulator, for DVDD of AK5702)
[VD]	(Orange)	= 2.7 ~ 3.6V (typ. 3.0V, for logic of digital part)
[AGND]	(Black)	= 0V (for analog ground)
[DGND]	(Black)	= 0V (for digital ground)

1-2) When AVDD, DVDD and VD are not supplied from the regulator.

[REG]	(Red)	= open
[AVDD]	(Orange)	= 2.4 ~ 3.6V (typ. 3.0V, for AVDD of AK5702)
[DVDD]	(Orange)	= 1.6 ~ 3.6V (typ. 3.0V, for DVDD of AK5702)
[VD]	(Orange)	= 2.7 ~ 3.6V (typ.3.0V, for logic of digital part)
[AGND]	(Black)	= 0V (for analog ground)
[DGND]	(Black)	= 0V (for digital ground)

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK5702 and AK4114 should be reset once by bringing SW1, 2 “L” upon power-up.

■ Evaluation mode

In case of AK5702 evaluation using AK4114, same audio interface format should be set for both AK5702 and AK4114. About AK5702’s audio interface format, refer to datasheet of AK5702. About AK4114’s audio interface format, refer to Table 2 in this manual.

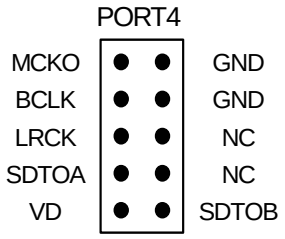
Applicable Evaluation Mode

(1) PLL Master Mode (Default)
(2) PLL Slave Mode 1 (PLL Reference CLOCK: MCKI pin)
(3) PLL Slave Mode 2 (PLL Reference CLOCK: BCLK or LRCK pin)
(4) EXT Slave Mode
(5) EXT Master Mode

(1) PLL Master Mode (Default)

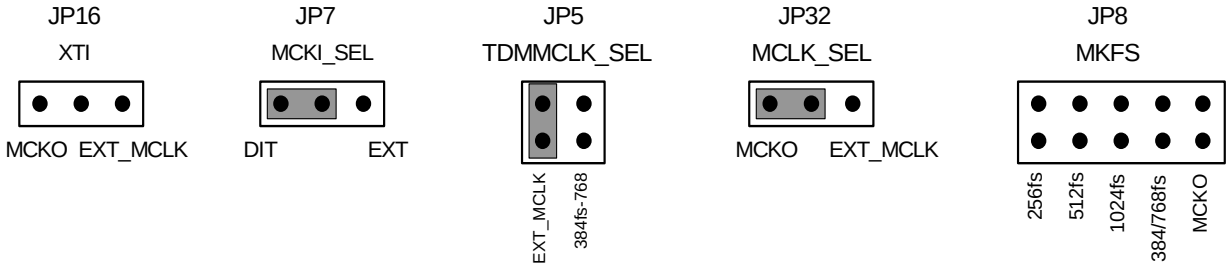
*** Connect PORT4 (DSP1) with DSP.**

Figure below shows PORT4 pin assign.



a) Set up jumper pins of MCKI clock

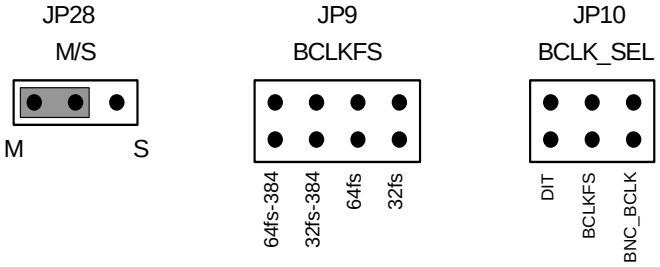
When using X'tal as MCKI clock, X'tal of 11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz can be set to X1. X'tal of 11.2896MHz (Default) is set on the AKD5702-A.
When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz) is supplied through a BNC connector J1 (EXT_MCKI), select EXT_MCLK on JP16 (XTI) and select EXT on JP7 (MCLK_SEL).
JP12 (EXT) and R19 should be properly selected in order to match the output impedance of the clock generator.



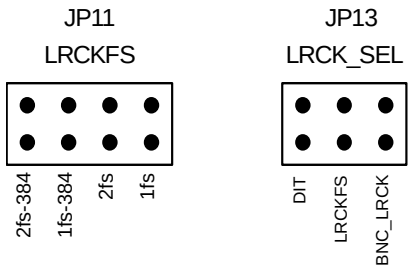
*The setting of JP8(MKFS) is invalid in this mode,but if JP8(MKFS) is open, the input of the buffer will be unstable. So JP8(MKFS) should set up any.

b) Set up jumper pins of BCLK clock

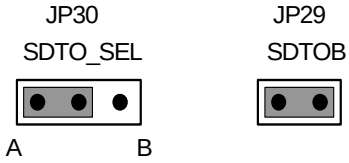
Output frequency (32fs/64fs) of BCLK should be set by "BCKO1-0 bit" in the AK5702.
There is no necessity for set up JP9(BCLKFS).



c) Set up jumper pins of LRCK clock



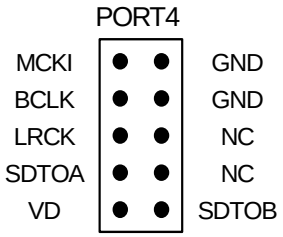
d) Set up jumper pins of SDTO



(2) PLL Slave Mode 1 (PLL Reference CLOCK: MCKI pin)

*** Connect PORT4 (DSP1) with DSP.**

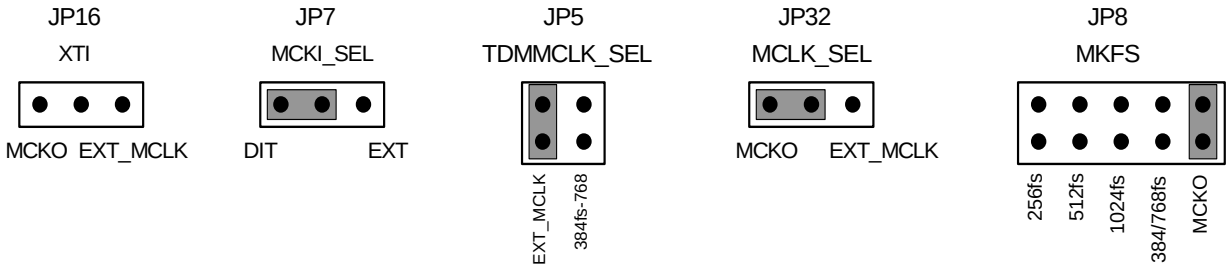
Figure below shows PORT4 pin assign.



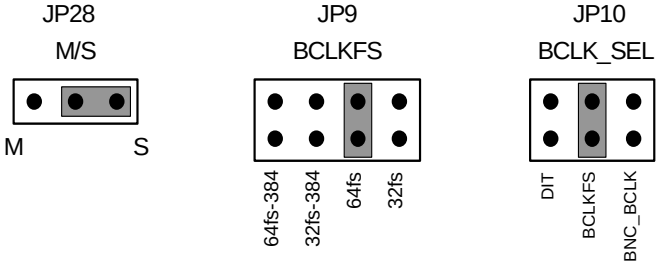
a) Set up jumper pins of MCKI clock

X'tal of 11.2896MHz (Default) is set on the AKD5702-A. In this case, the AK5702 corresponds to PLL reference clock of 11.2896MHz. In this evaluation mode, the output clock from MCKO pin of the AK5702 is supplied to a divider (U3: 74VHC4040), EXT_BCLK and EXT_LRCK clocks are generated by the divider. Then "MCKO bit" in the AK5702 should be set to "1".

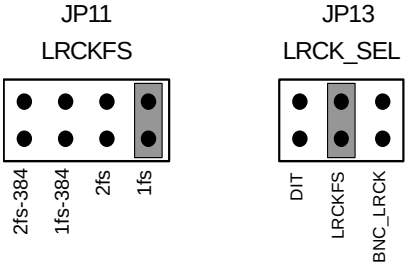
When an external clock is supplied through a BNC connector J1 (EXT_MCKI), select EXT_MCLK on JP16 (XTI) and select EXT on JP7 (MCKI_SEL). JP12 (EXT) and R19 should be properly selected in order too match the output impedance of the clock generator.



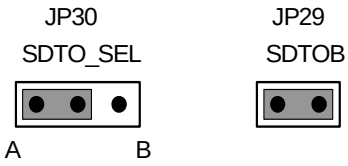
b) Set up jumper pins of BCLK clock



c) Set up jumper pins of LRCK clock



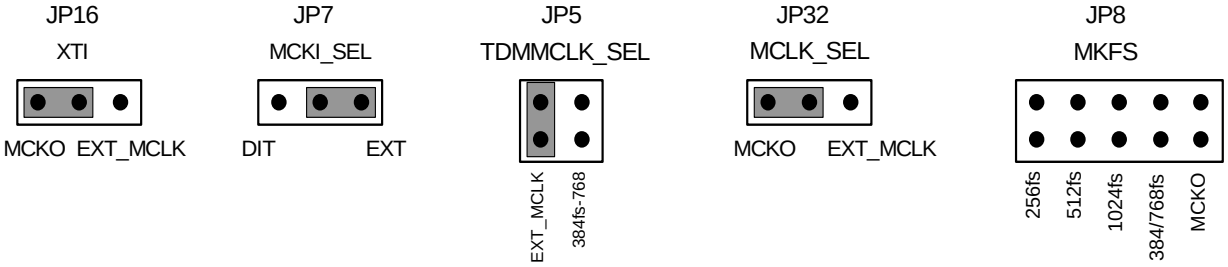
d) Set up jumper pins of SDTO



(2-a) In the case of using AK4114.

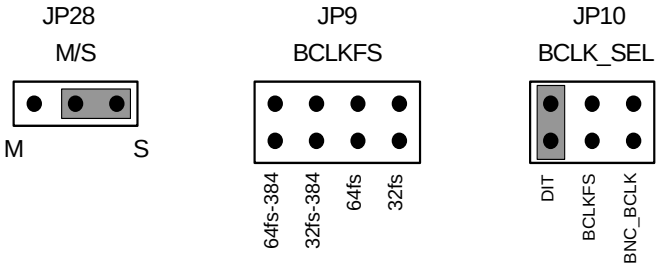
* In this mode, MCLK of AK5702 should be supplied from J1 (EXT_MCKI), and X1 should be open. This mode is BCLK=64fs, LRCK=1fs only.

Set up jumper pins of MCKI clock

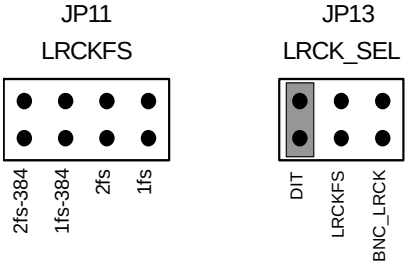


*The setting of JP8(MKFS) is invalid in this mode,but if JP8(MKFS) is open, the input of the buffer will be unstable. So JP8(MKFS) should set up any.

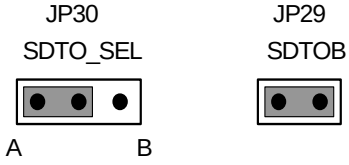
Set up jumper pins of BCLK clock



Set up jumper pins of LRCK clock



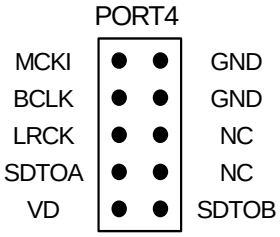
Set up jumper pins of SDTO



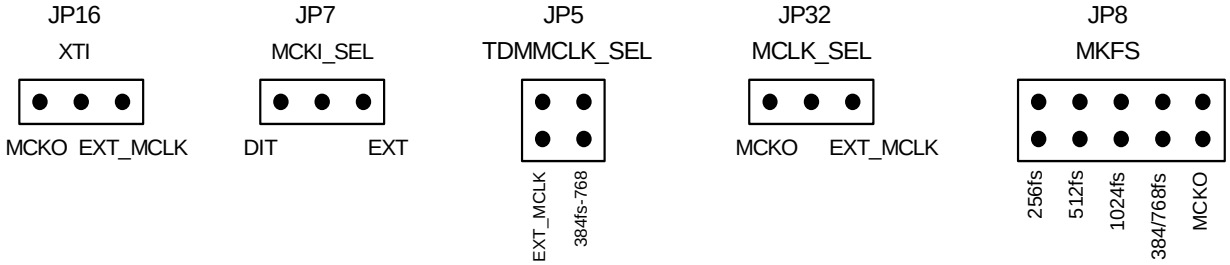
(3) PLL Slave Mode 2 (PLL Reference CLOCK: BCLK or LRCK pin)

*** Connect PORT4 (DSP1) with DSP.**

Figure below shows PORT4 pin assign.

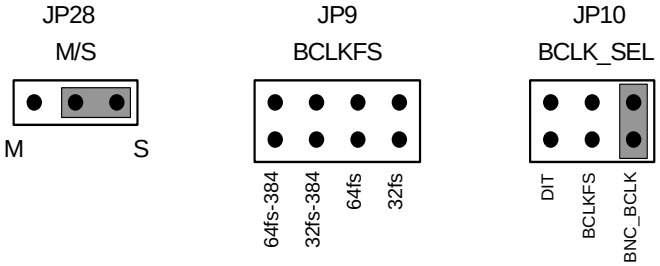


a) Set up jumper pins of MCKI clock

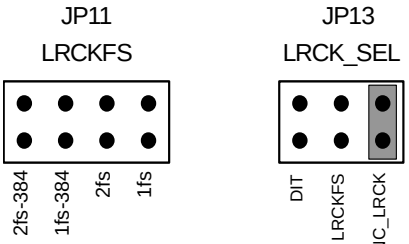


b) Set up jumper pins of BCLK clock

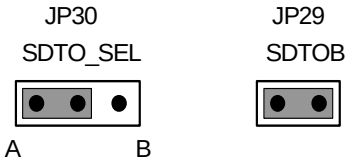
When an external clock is supplied through a BNC connector J2 (EXT/BCLK), J3 (EXT/LRCK), JP14 (EXT1) and R20, JP15 (EXT2) and R21 should be properly selected in order to much the output impedance of the clock generator.



c) Set up jumper pins of LRCK clock



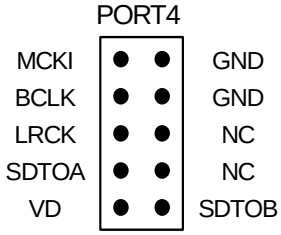
d) Set up jumper pins of SDTO



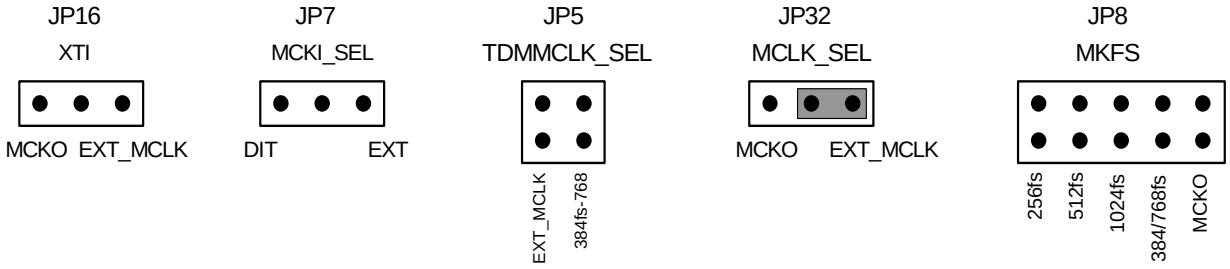
(4) EXT Slave Mode

*** Connect PORT4 (DSP1) with DSP.**

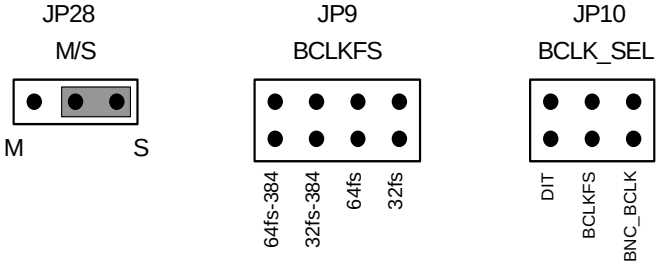
Figure below shows PORT4 pin assign. In this mode, MCKI, BCLK and LRCK should be supplied from PORT4.



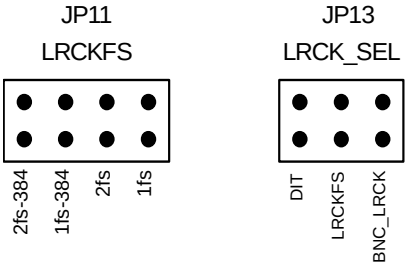
a) Set up jumper pins of MCKI clock



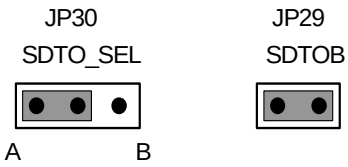
b) Set up jumper pins of BCLK clock



c) Set up jumper pins of LRCK clock



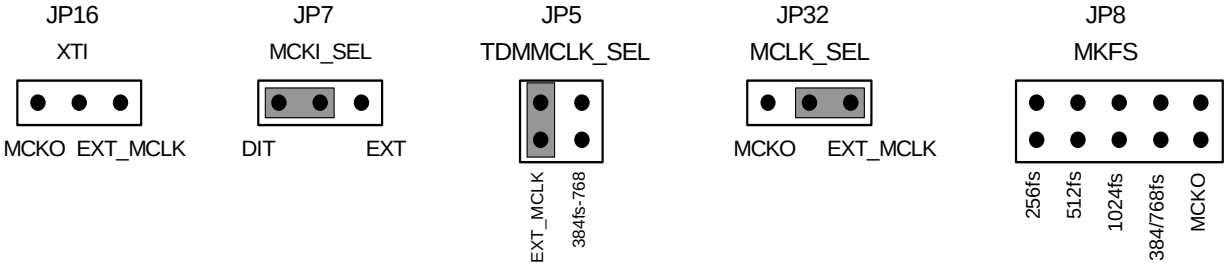
d) Set up jumper pins of SDTO



(4-a) In the case of using AK4114.

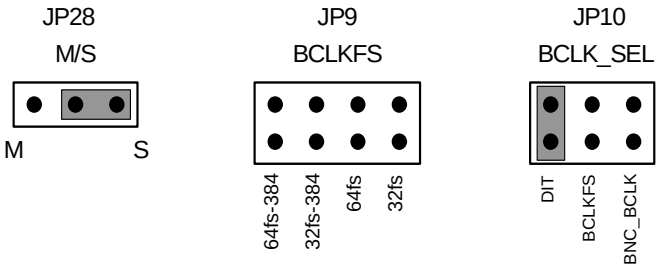
*This mode is BCLK=64fs, LRCK=1fs only. The setting of JP16(XTI) is open, the clock of AK4114 use X'tal of X1. The signal of MCKO, BCLK and LRCK outputted from AK4114 is inputted into AK5702.

Set up jumper pins of MCKI clock

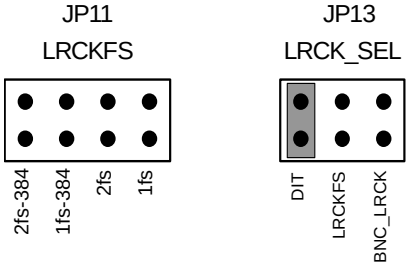


*The setting of JP8(MKFS) is invalid in this mode,but if JP8(MKFS) is open, the input of the buffer will be unstable. So JP8(MKFS) should set up any.

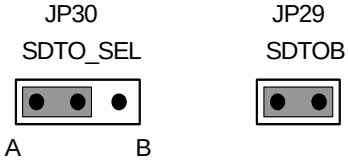
Set up jumper pins of BCLK clock



Set up jumper pins of LRCK clock



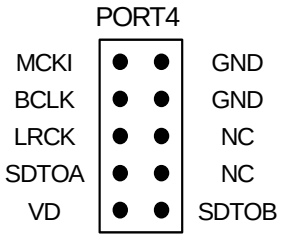
Set up jumper pins of SDTO



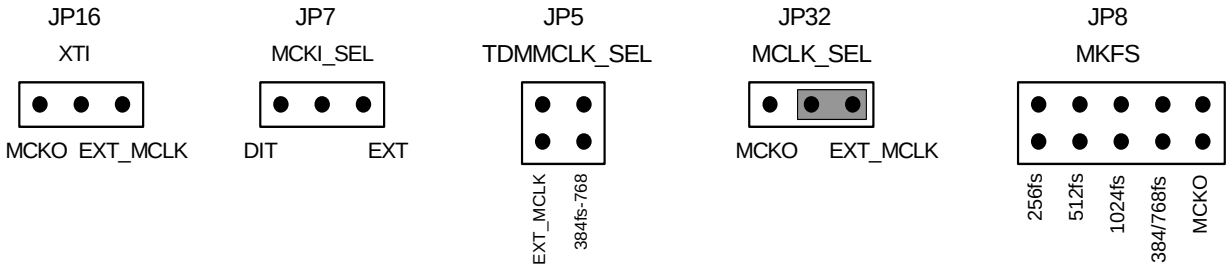
(5) EXT Master Mode

*** Connect PORT4 (DSP1) with DSP.**

Figure below shows PORT4 pin assign. In this mode, MCKI should be supplied from PORT4, but BCLK and LRCK should not be supplied.

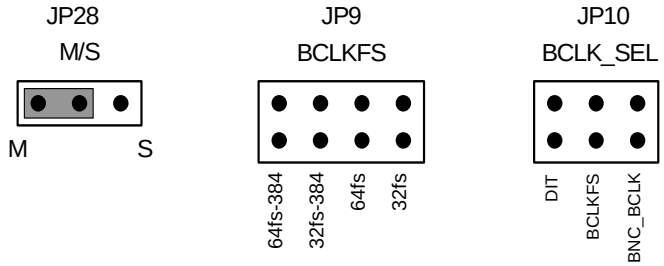


a) Set up jumper pins of MCKI clock

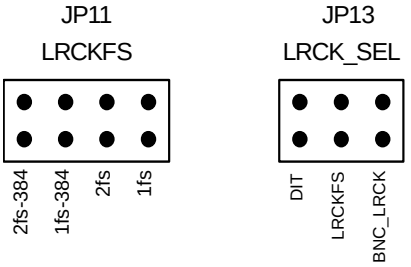


*The setting of JP8(MKFS) is invalid in this mode,but if JP8(MKFS) is open, the input of the buffer will be unstable. So JP8(MKFS) should set up any.

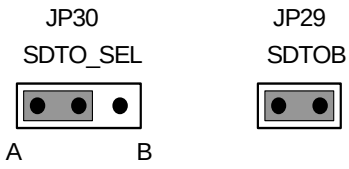
b) Set up jumper pins of BCLK clock



c) Set up jumper pins of LRCK clock



d) Set up jumper pins of SDTO



■ DIP Switch set up

[SW1] (MODE): Mode Setting of AK4114
ON is "H", OFF is "L".

No.	Name	ON ("H")	OFF ("L")
1	I2S	AK4114 Audio Format Setting See Table 2	
2	M/S		
3	OCKS0	Master Clock Frequency Select See Table 3	
4	OCKS1		
5	CAD1	Chip Address pin	
6	CAD0		
7	TEST	"L"	
8	I2C	µp Control Mode Select pin "H": I2C, "L": 3-wire serial	

Table 1. Mode Setting

Resistor for AK5702			Set up for AK4114 SW1			
M/S	DIF1	DIF0	DIF1	DIF0	DAUX	
0	1	0	0	0	24bit, Left justified	Master
0	1	1	0	1	24bit, I^2S	Master
1	1	0	1	0	24bit, Left justified	Slave
1	1	1	1	1	24bit, I^2S	Slave

Default

Table 2. Setting for AK5702 and AK4114 Audio Interface Format

No.	OCKS1	OCKS0	MCKO1	X'tal	
0	0	0	256fs	256fs	Default
2	1	0	512fs	512fs	

Table 3. Master Clock Frequency Select for AK4114 (Stereo mode)

■ Other jumper pins set up

1. JP1, JP3 (MPWRB): Connect to MPWRB
   - OPEN : No connect <Default>
   - SHORT : Connect to MPWRB

2. JP2, JP4 (MPWRA) : Connect to MPWRA
   - OPEN : No connect <Default>
   - SHORT : Connect to MPWRA

3. JP17 (LIN125_SEL) : Select input pin from J4
   - LIN1 : Enable to input to LIN1 from J4 <Default>
   - LIN2 : Enable to input to LIN2 from J4
   - LIN5 : Enable to input to LIN5 from J4

4. JP18 (RIN125_SEL) : Select input pin from J6
   - RIN1 : Enable to input to RIN1 from J6 <Default>
   - RIN2 : Enable to input to RIN2 from J6
   - RIN5 : Enable to input to RIN5 from J6

5. JP19 (LIN5_SEL) : Select input connecter to LIN5
   - LIN125 : Enable to input to LIN5 from J4 <Default>
   - LIN345 : Enable to input to LIN5 from J7

6. JP20 (RIN5_SEL) : Select input connecter to RIN5
   - RIN125 : Enable to input to RIN5 from J6 <Default>
   - RIN345 : Enable to input to RIN5 from J9

7. JP21 (LIN345_SEL) : Select input pin from J7
   - LIN3 : Enable to input to LIN3 from J7 <Default>
   - LIN4 : Enable to input to LIN4 from J7
   - LIN5 : Enable to input to LIN5 from J7

8. JP22 (RIN345_SEL) : Select input pin from J9
   - RIN3 : Enable to input to RIN3 from J9 <Default>
   - RIN4 : Enable to input to RIN4 from J9
   - RIN5 : Enable to input to RIN5 from J9

9. JP35 (SDTOB_SEL) : Select input pin to TDMIN
   - PDOWN : Connect to GND <Default>
   - SDTOB : Connect to SDTOB

10. JP36 (CTRL_SEL) : Select for µp Control Mode
    - 3-WIRE : Select to 3-WIRE <Default>
    - I2C : Select to I2C

11. JP37 (GND) : Analog ground and Digital ground
    - OPEN : Separated. <Default>
    - SHORT : Common. (The connector “DGND” should be open.)

12. JP38 (AVDD_SEL) : AVDD of the AK5702
    - REG : AVDD is supplied from the regulator (“AVDD” jack should be open). < Default >
    - AVDD : AVDD is supplied from “AVDD ” jack.

13. JP39 (DVDD_SEL) : DVDD of the AK5702
AVDD : DVDD is supplied from “AVDD”. < Default >
DVDD : DVDD is supplied from “DVDD ” jack.

14. JP40 (LVC_SEL) : Supply line selection of Logic block of LVC.
DVDD : Logic block of LVC is supplied from “DVDD”. < Default >
VD : Logic block of LVC is supplied from “VD ” jack.

■ The function of the toggle SW

[SW2] (PDN): Power control of AK5702. Keep “H” during normal operation.

[SW3] (DIT): Power control of AK4114. Keep “H” during normal operation.
Keep “L” when AK4114 is not used.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AK5702 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (CTRL) with PC by 10-wire flat cable packed with the AKD5702-A

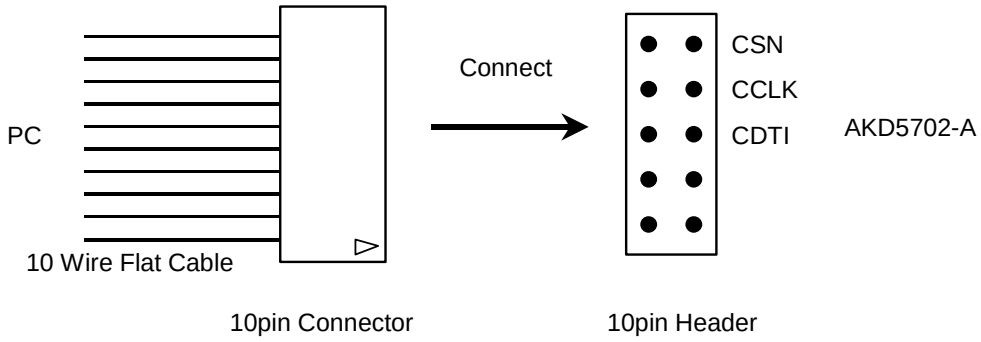


Figure 2. Connect of 10 wire flat cable

■ Analog Input / Output Circuits

(1) Input Circuits

a) LIN, RIN, MIC Input Circuit

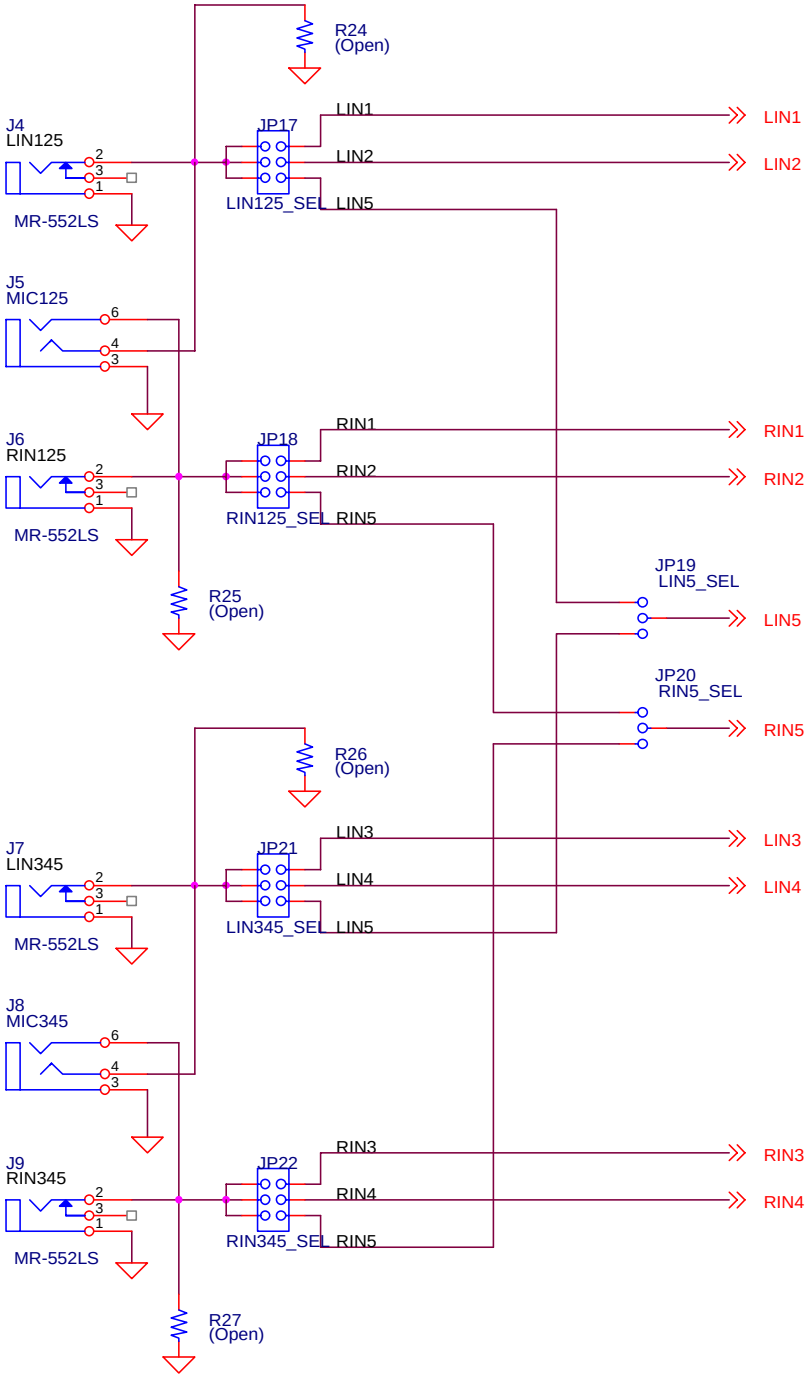


Figure 3. LIN, RIN, MIC Input Circuit

∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

2. Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD5702-A according to previous term.

2. Connect IBM-AT compatible PC with AKD5702-A by 10-line type flat cable (packed with AKD5702-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AK5702 Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “akd5702-a.exe” to set up the control program.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Port Reset” button.
3. Click “Write default” button

■ Explanation of each buttons

1. [Port Reset]: Set up the USB interface board (AKDUSBIF-A) when using the board.
2. [Write default]: Initialize the register of AK5702.
3. [All Write]: Write all registers that is currently displayed.
4. [Function1]: Dialog to write data by keyboard operation.
5. [Function2]: Dialog to write data by keyboard operation.
6. [Function3]: The sequence of register setting can be set and executed.
7. [Function4]: The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE]: Save the current register setting.
10. [OPEN]: Write the saved values to all register.
11. [Write]: Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to AK5702, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK5702, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate IVOL

There are dialogs corresponding to register of 18h and 19h.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK5702 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK5702, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is “akr”.

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is “akr”.

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK5702. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button. The following is displayed.

(2) Set the control sequence.
Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is “aks”.

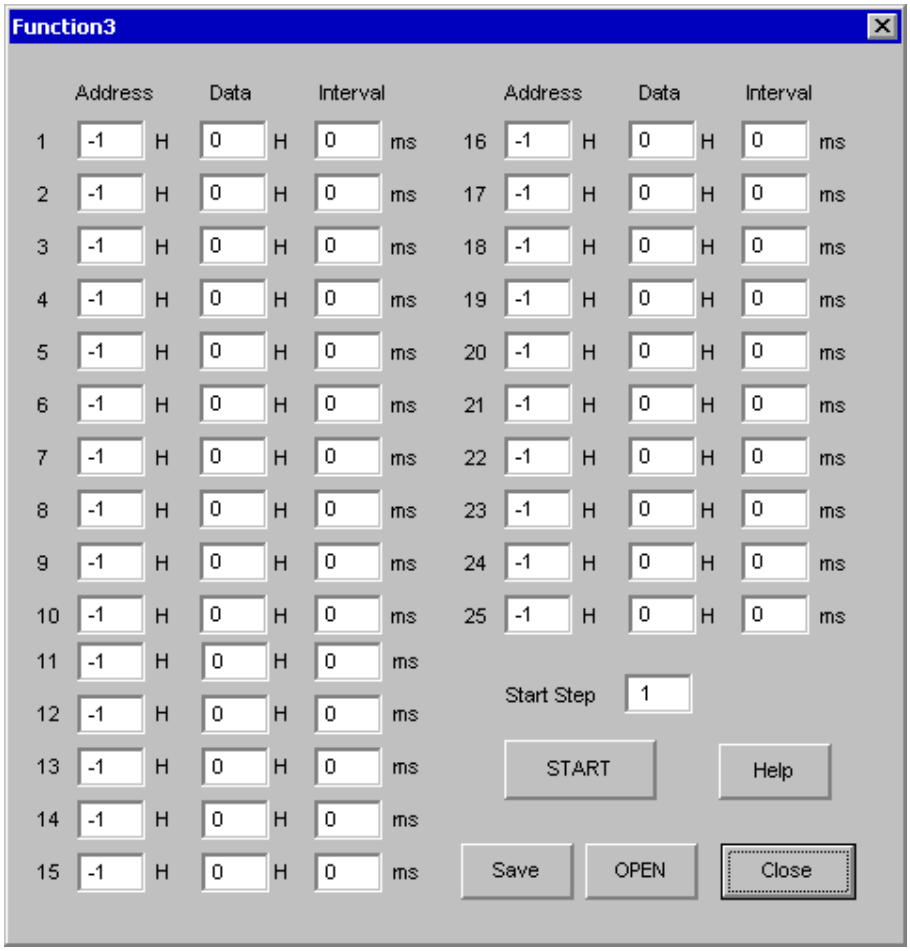


Figure 1. [F3] window

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

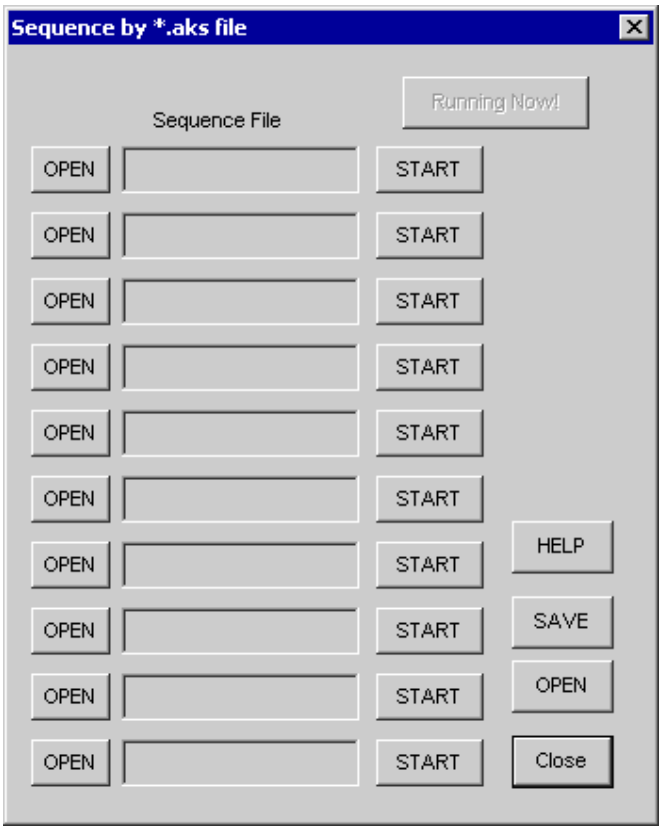


Figure 2. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 3. (In case that the selected sequence file name is "DAC_Stereo_ON.aks")

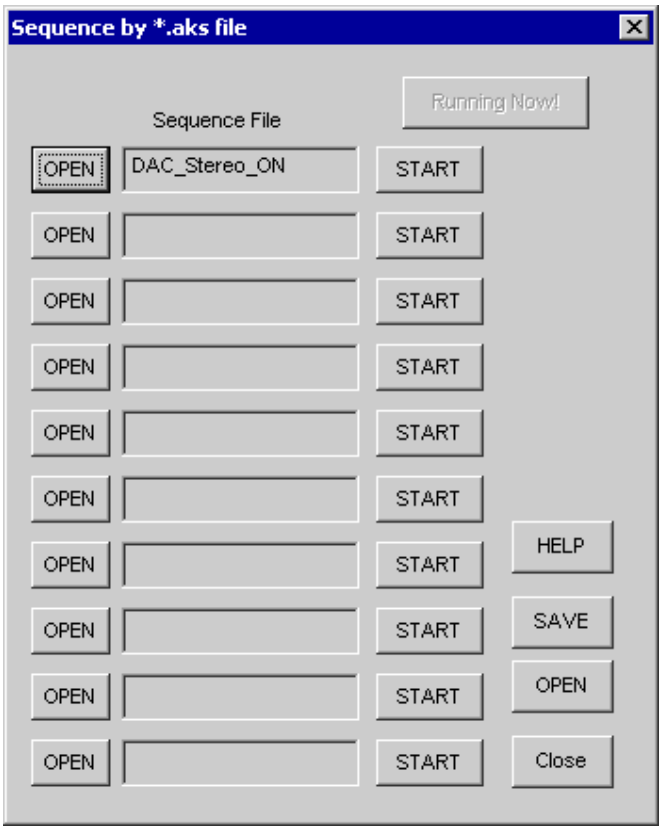


Figure 3. [F4] window (2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is "*.ak4".

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 4 opens.

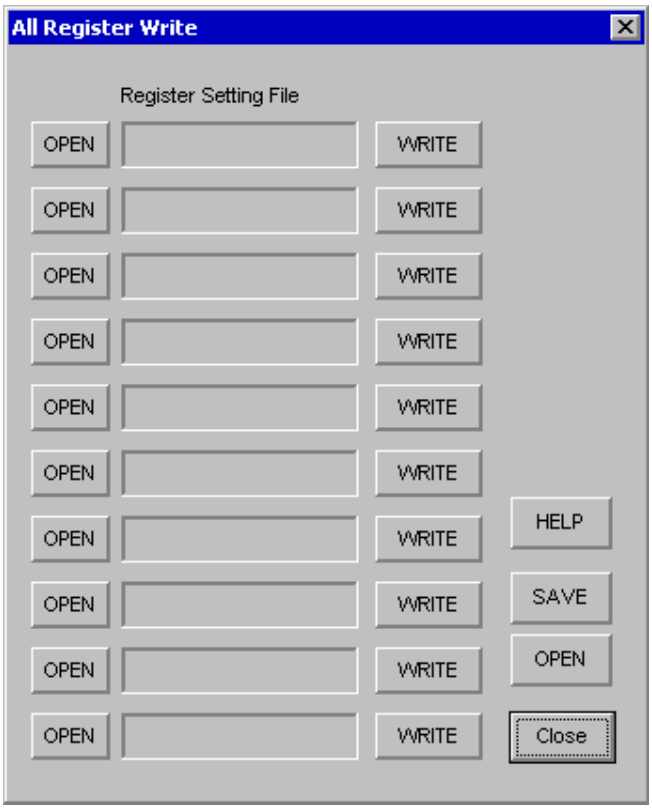


Figure 4. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 5. (In case that the selected file name is "DAC_Output.akr")

(2) Click [WRITE] button, then the register setting is executed.

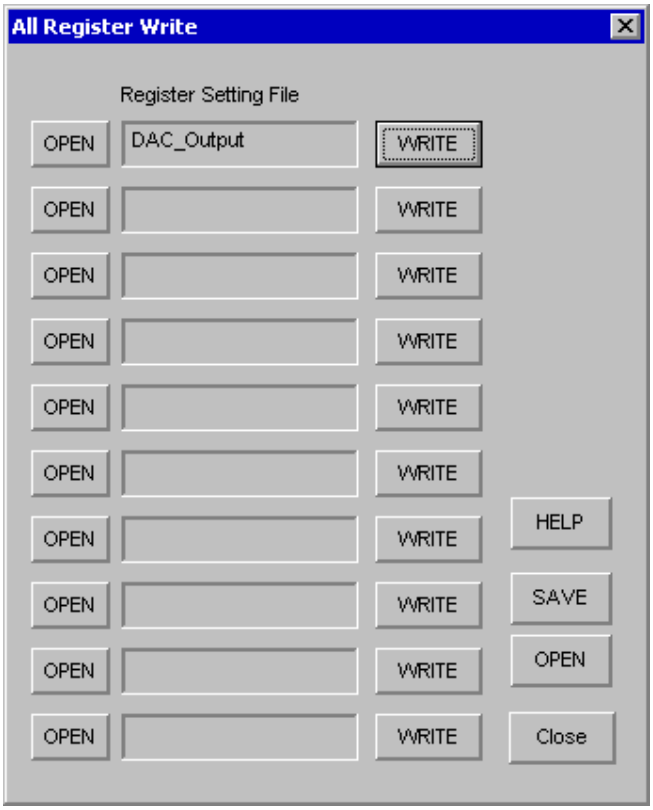


Figure 5. [F5] window (2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

Revision History

Date	Manual Revision	Board Revision	Reason	Contents
2006/11/28	KM086500	0	First Edition	
2007/04/09	KM086501	1	Error Correct	P2. Operation Sequence 1) Set up the power supply lines 1-1) Add (default) to the end of sentence. AVDD: open → open (3.0V, supply from regulator, for AVDD of AK5702) DVDD: open → open (3.0V, supply from regulator, for DVDD of AK5702) VD: for logic → (typ 3.0V, for logic of digital part) 1-2) "REG" jack should be open → open AVDD: for AVDD of AK5702 (typ.3.0V)→ (typ.3.0V, for AVDD of AK5702) DVDD: for DVDD of AK5702 (typ.3.0V)→ (typ.3.0V, for DVDD of AK5702) VD: for logic → (typ 3.0V, for logic of digital part) P2. Evaluation Mode Applicable Evaluation Mode (1) Evaluation of PLL, Master Mode → PLL Master Mode (2) Evaluation of PLL, Slave Mode → PLL Slave Mode 1 (3) Evaluation of PLL, Slave Mode → PLL Slave Mode 2 (4) Evaluation of EXT, Slave Mode → EXT Slave Mode (5) EXT, Master Mode → EXT Master Mode P3-P10 (1) Evaluation of PLL, Master Mode → PLL Master Mode a) Set up jumper pins of MCKI clock (J1: EXT_MCKI) → J1 (EXT_MCKI) JP8 → JP8 (MKFS) b) Set up jumper pins of BCLK clock JP9 → JP9 (BCLKFS) (2) Evaluation of PLL, Slave Mode → PLL Slave Mode 1 a) Set up jumper pins of MCKI clock (J1: MCLK_SEL) → J1 (EXT_MCKI) (2-a) In the case of using AK4114 J1 → J1 (EXT_MCLK) JP8 → JP8 (MKFS) (3) Evaluation of PLL, Slave Mode → PLL Slave Mode 2 (4) Evaluation of EXT, Slave Mode → EXT Slave Mode Connect PORT4 (DSP1) with DSP In this mode, BCLK and LRCK should be supplied from PORT4, but MCKI should not be supplied. → In this mode, MCKI, BCLK and LRCK should be supplied from PORT4. (4-a) In the case of using AK4114 JP16 → JP16 (XTI) JP8 → JP8 (MKFS) (5) EXT, Master Mode → EXT Master Mode a) Set up jumper pins of MCKI clock JP8 → JP8 (MKFS) b) Set up jumper pins of BCLK clock The direction of jumper setup of JP28 (M/S): S (Slave) → M (Master) P11. Other jumper pins set up 12. JP38 (AVDD_SEL) OPEN→REG SHORT→AVDD
			Circuit Change	Resistance value, Capacitance Value Change: MCKI: R13: 51→R100:100, C100: Open→22p BICK: R101: Short→100, C101: Open→22p LRCK: R102: Short→100, C102: Open→22p

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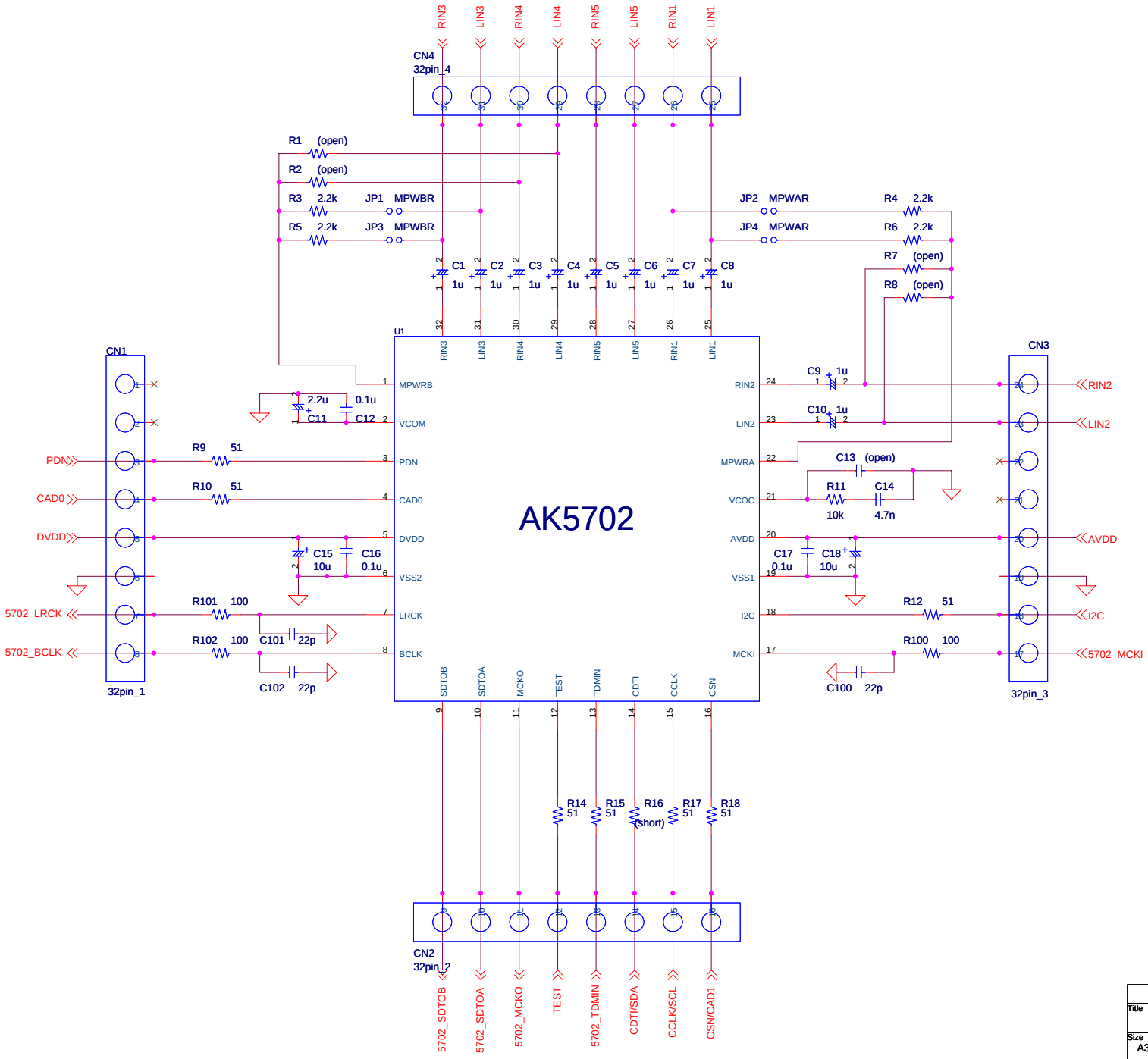

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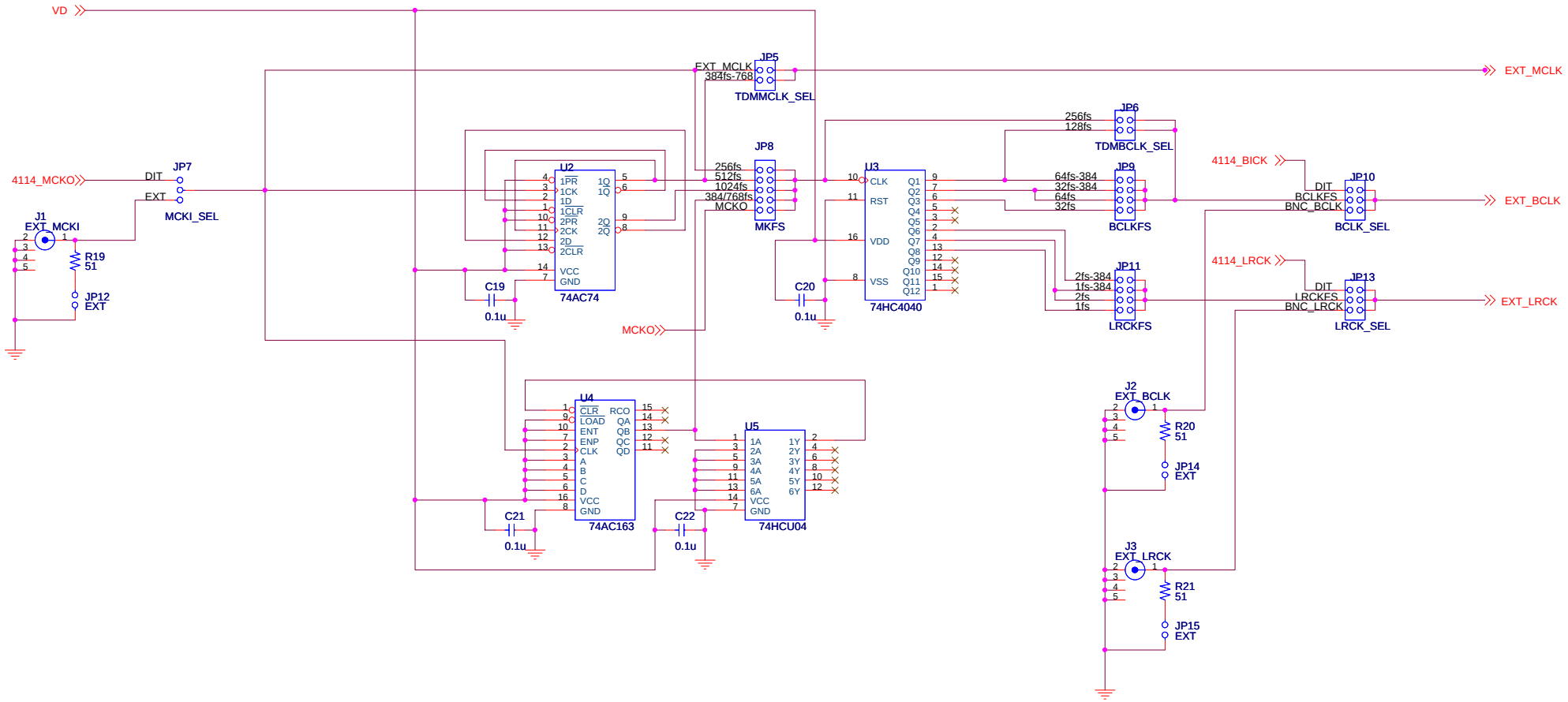
Size A3	Document Number AK5702	Rev 1
Date: Monday, April 09, 2007	Sheet 1 of 6	



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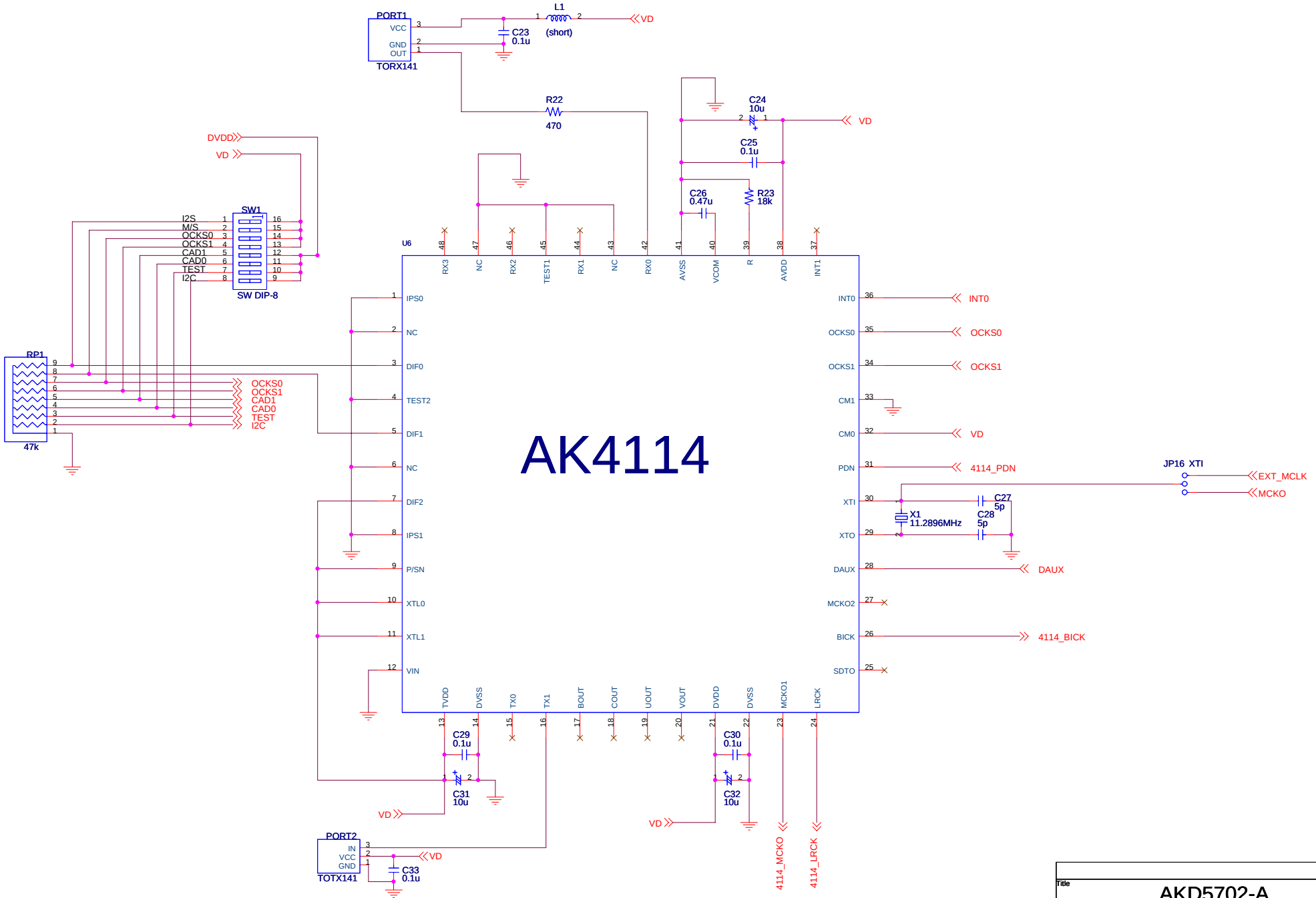

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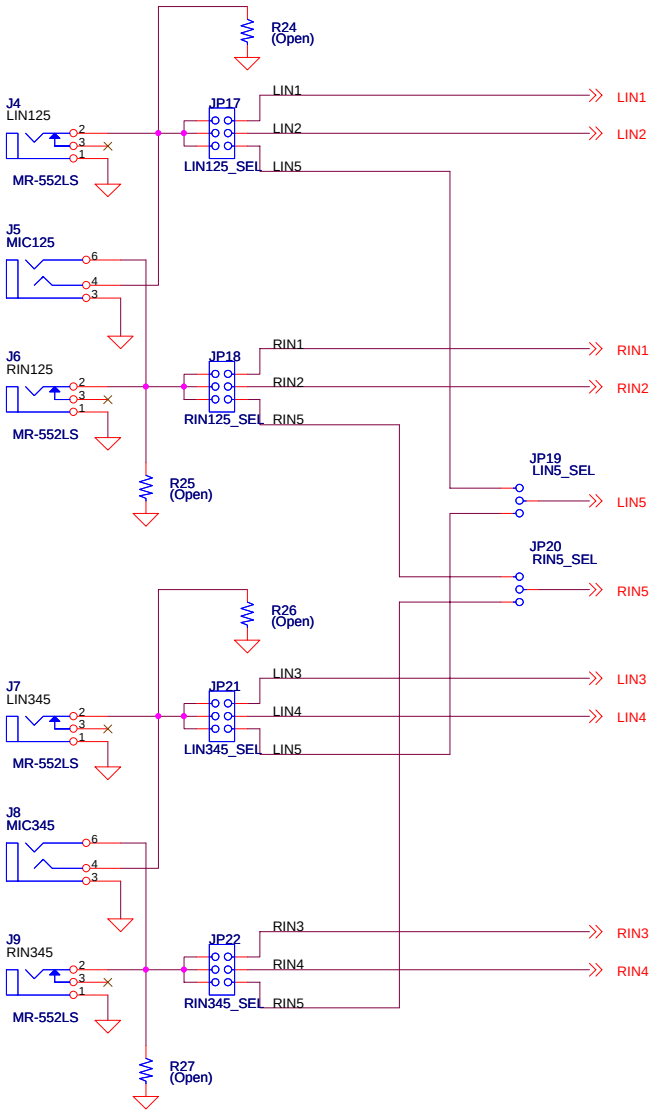
Size A3	Document Number DIT		Rev 1
Date: Monday, April 09, 2007	Sheet 3 of 6		



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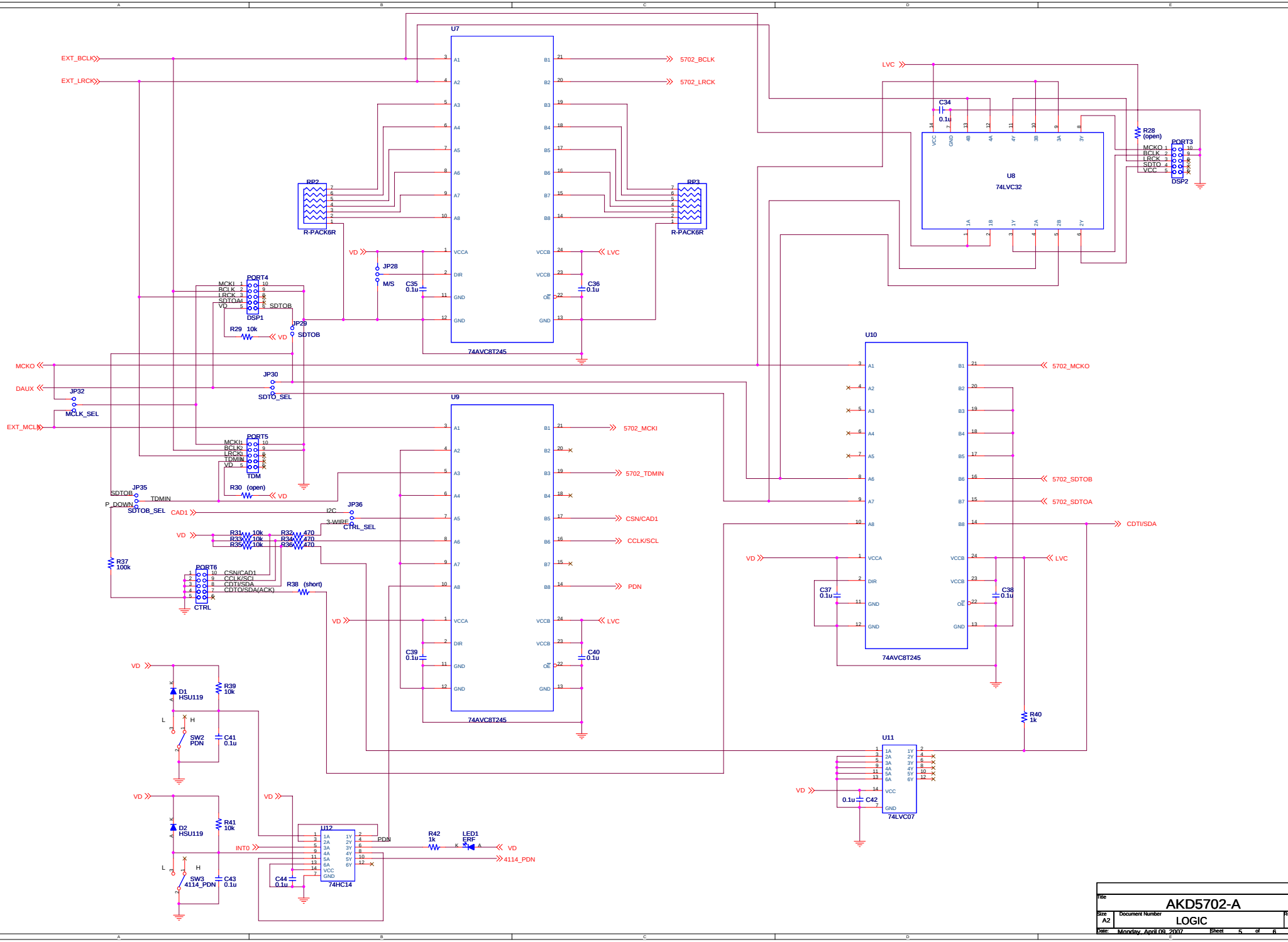
Date: Monday, April 09, 2007	Sheet 4 of 6	



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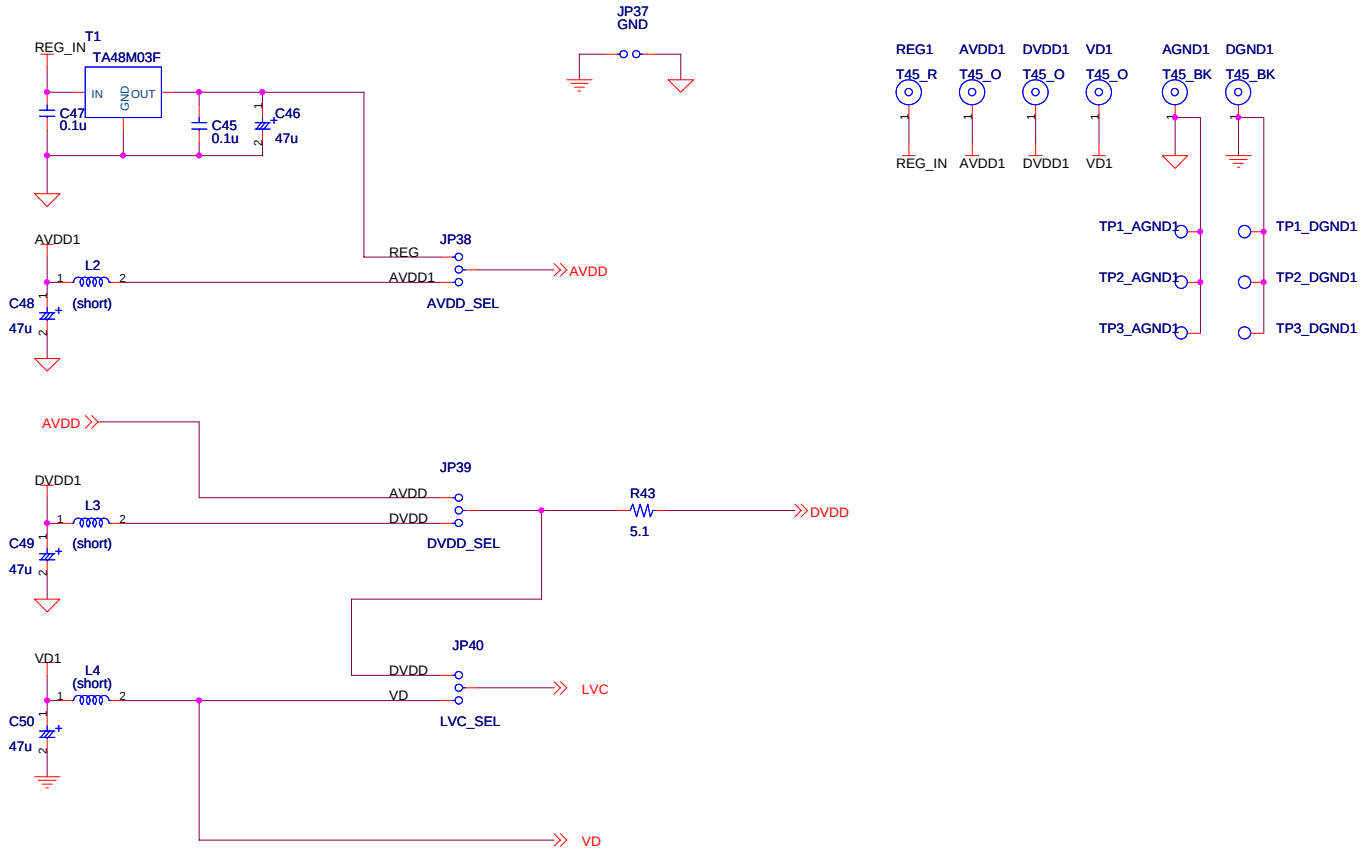
Size A2	Document Number LOGIC	Rev 1
Date: Monday, April 09, 2007	Sheet 5 of 6	



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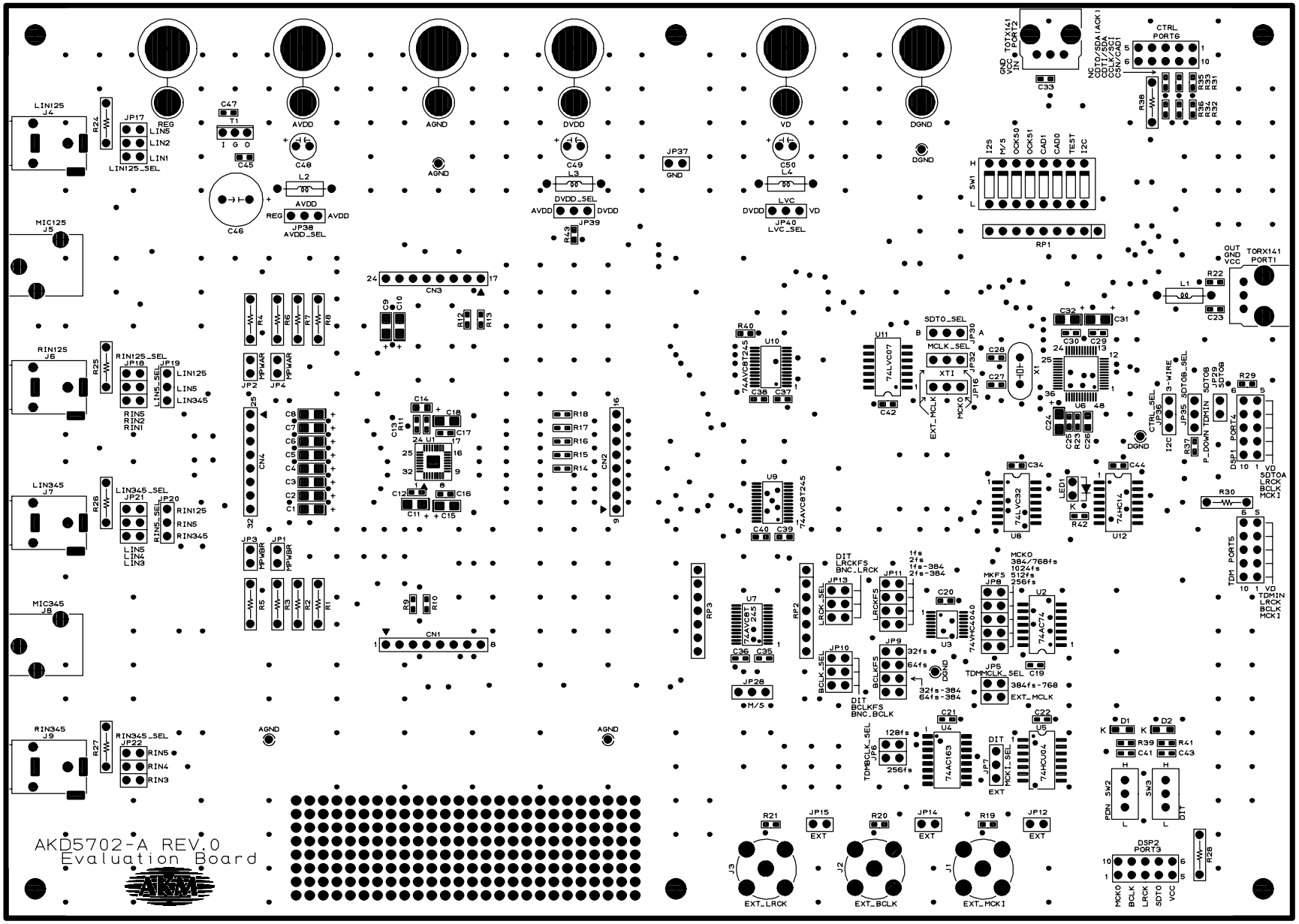
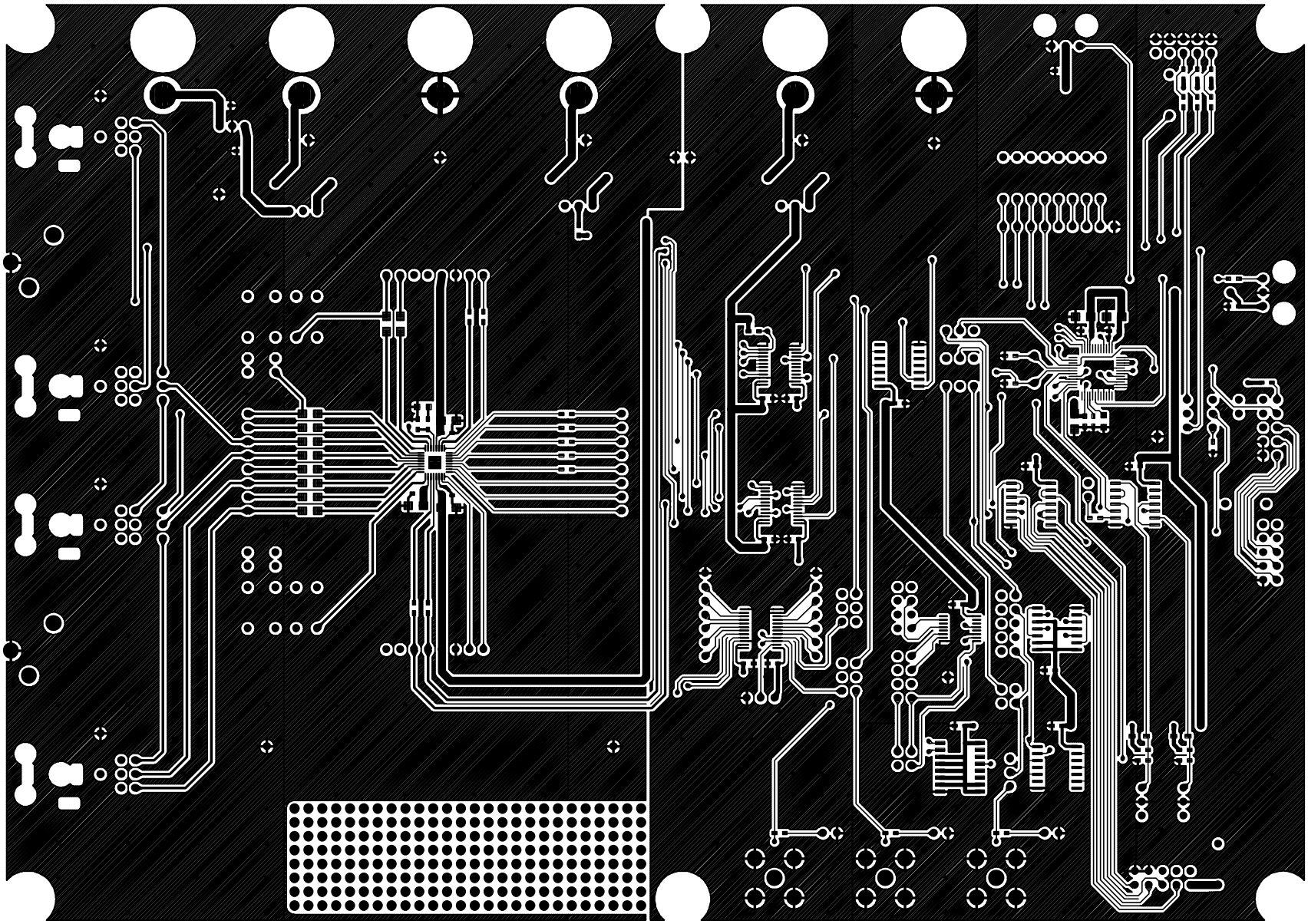
Date: Monday, April 09, 2007	Sheet 6 of 6	



AKD5702-A L1 SILK

AKD5702-A L2 SILK



AKD5702-A L1

AKD5702-A L2