

TIC236A, TIC236B, TIC236C, TIC236D, TIC236E, TIC236M, TIC236N, TIC236S

SILICON TRIACS

- High current triacs
- 12 A RMS
- Glass Passivated Wafer
- 100 V to 800 V Off-State Voltage
- Max I_{GT} of 50 mA (Quadrants 1-3)
- Compliance to ROHS

ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings	Value							Unit	
		Α	В	С	D	E	М	S	N	
V _{DRM}	Repetitive peak off-state voltage (see Note1)	100	200	300	400	500	600	700	800	V
I _{T(RMS)}	Full-cycle RMS on-state current at (or below) 70°C case temperature (see note2)	12				А				
I _{TSM}	Peak on-state surge current full-sine-wave (see Note3)		100						Α	
I _{GM}	Peak gate current		± 1						Α	
T _C	Operating case temperature range			-40 to +110					°C	
T _{stg}	Storage temperature range		-40 to +125						°C	
TL	Lead temperature 1.6 mm from case for 10 seconds	230			°C					

THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit			
R _{∂JC}	Junction to case thermal resistance	≤ 2	°C/W			
R∂JA	Junction to free air thermal resistance	≤ 62.5	C/VV			



TIC236A, TIC236B, TIC236C, TIC236D, TIC236E, TIC236M, TIC236N, TIC236S

ELECTRICAL CHARACTERISTICS

TC=25°C unless otherwise noted

Symbol	Ratings	Test Condition(s)		Тур	Max	Unit		
I _{DRM}	Repetitive peak off-state current	V_D = Rated V_{DRM} , , I_G = 0 T_C = 110°C	-	-	±2	mA		
		V_{supply} = +12 V†, R _L = 10 Ω, $t_{p(g)}$ = > 20 μs	-	12	50			
I _{GT}	Gate trigger current	V_{supply} = +12 V†, R_L = 10 Ω , $t_{p(g)}$ = > 20 μ s				mA		
		$V_{\text{supply}} = -12 \text{ V}^{\dagger}, R_{\text{L}} = 10 \Omega, t_{\text{p(g)}} = > 20 \mu \text{s}$	-	-16	-50	111/5		
		V_{supply} = -12 V†, R_L = 10 Ω , $t_{p(g)} = > 20 \ \mu s$	-	34	-			
		V_{supply} = +12 V†, R_L = 10 Ω , $t_{p(g)}$ = > 20 μ s	-	8.0	2			
V_{GT}	Gate trigger voltage	V_{supply} = +12 V†, R_L = 10 Ω , $t_{p(g)}$ = > 20 μs	-	-0.8	-2	V		
V GT		V_{supply} = -12 V†, R _L = 10 Ω , $t_{p(g)}$ = > 20 μ s	-	-0.8	-2	v		
		V_{supply} = -12 V†, R _L = 10 Ω , $t_{p(g)}$ = > 20 μ s	-	0.9	2			
I _H	Holding current	V_{supply} = +12 V†, I_G = 0 initiating I_{TM} = 100 mA	-	22	40	mA		
		$V_{\text{supply}} = -12 \text{ V}^{\dagger}, I_G = 0$ initiating $I_{\text{TM}} = -100 \text{ mA}$	-	-22	-40			
1	Latching current	V _{supply} = +12 V† (seeNote5)	-	-	80	mA		
IL.	Latering current	V _{supply} = -12 V† (seeNote5)	-	-	-80	ША		
V_{TM}	Peak on-state voltage	$I_{TM} = \pm 17 \text{ A}, I_G = 50 \text{ mA} \text{ (see Note4)}$	-	±1.4	±1.7	٧		
dv/dt	Critical rate of rise of off-state voltage	V_{DRM} = Rated V_{DRM} , I_G = 0 T_C = 110°C	-	±400	-	V/µs		
di/dt	Critical rate of rise of off-state current	V_{DRM} = Rated V_{DRM} , I_{GT} = 50 mA, di_{G}/dt = 50mA/ μ s, T_{C} = 110°C	-	±100	-	A/µs		
dv/dt _©	Critical rise of communication voltage	V_{DRM} = Rated V_{DRM} , I_{T} = 1.4 $I_{\text{T(RMS)}}$ di/dt = 0.5 $I_{\text{T(RMS)}}$ /ms, I_{C} = 80°C	±1.2	±9	-	V/µs		

- † All voltages are whit respect to Main Terminal 1.
 - Note1: These values apply bidirectionally for any value of resistance between the gate and Main Terminal 1.
 - Note2: This value applies for 50-Hz full-sine-wave operation with resistive load. Above 70°C derate linearly to 110°C case temperature at the rate of 300 mA/°C.
 - Note3: This value applies for one 50-Hz full-sine-wave when the device is operating at (or below) the rated value of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
 - Note4: This parameters must be measured using pulse techniques, $t_W = \le 1$ ms, duty cycle ≤ 2 %, voltage-sensing contacts, separate from the courrent-carrying contacts are located within 3.2mm from de device body.
 - Note5: he triacs are triggered by a 15-V (open circuit amplitude) pulse supplied by a generator with the following characteristics: $R_G = 100\Omega$, $t_{D(q)} = 20 \mu s$, $t_r = 100 \mu s$, $t_r = 1$



TIC236A, TIC236B, TIC236C, TIC236D, TIC236E, TIC236M, TIC236N, TIC236S

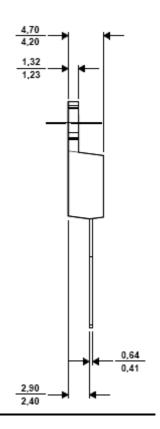
MECHANICAL DATA CASE TO-220

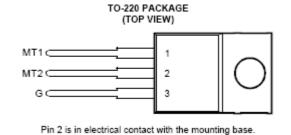
TO220 10,4 10,0 2,95 2,54 see Note B 6,6 6,0 15.90 14.55 see Note C 6,1 3,5 12,7 1,70 1.07 0,97

2,74

2,34

5,28





Pin 1 :	Main Terminal 1
Pin 2 :	Main Terminal 2
Pin 3 :	Gate

September 2012

Information furnished is believed to be accurate and reliable. However, Comset Semiconductors assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may results from its use. Data are subject to change without notice. Comset Semiconductors makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Comset Semiconductors assume any liability arising out of the application or use of any product and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Comset Semiconductors' products are not authorized for use as critical components in life support devices or systems.

www.comsetsemi.com

info@comsetsemi.com