# HD74LV164A

8-bit Parallel-out Serial-in Shift Register

HITACHI

ADE-205-266A (Z)

Rev.1
August 2001

## Description

The HD74LV164A is 8-bit shift register has gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by low level at the clear input.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

## Features

- $V_{CC}$ = 2.0 V to 5.5 V operation
- All inputs $V_{IH}$ (Max.) = 5.5 V (@$V_{CC}$ = 0 V to 5.5 V)
- All outputs $V_O$ (Max.) = 5.5 V (@$V_{CC}$ = 0 V)
- Typical $V_{OL}$ ground bounce < 0.8 V (@$V_{CC}$ = 3.3 V, Ta = 25°C)
- Typical $V_{OH}$ undershoot > 2.3 V (@$V_{CC}$ = 3.3 V, Ta = 25°C)
- Output current ±6 mA (@$V_{CC}$ = 3.0 V to 3.6 V), ±12 mA (@$V_{CC}$ = 4.5 V to 5.5 V)

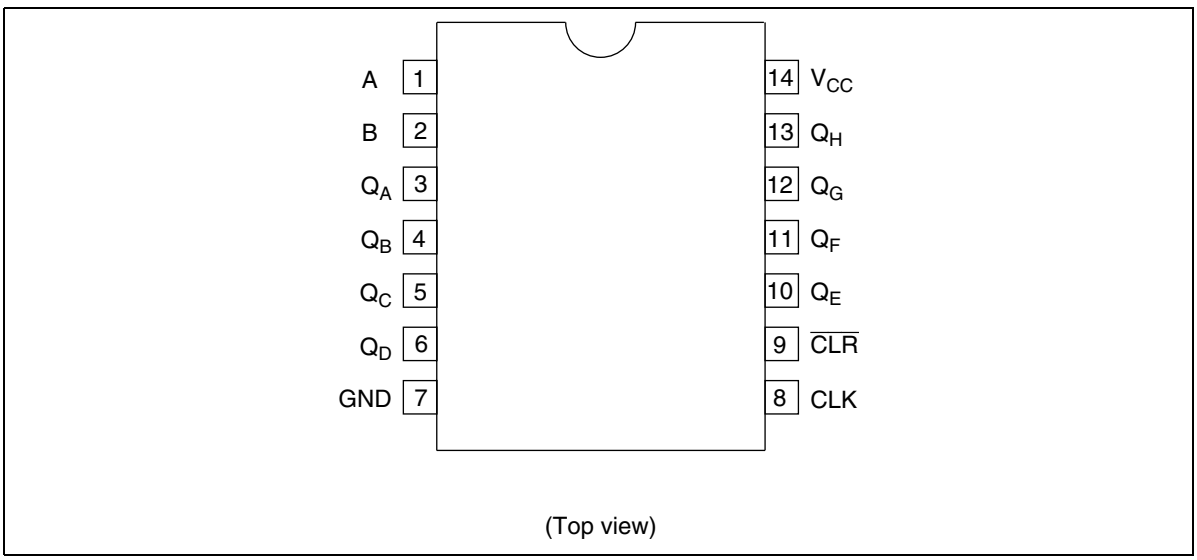
Hitachi semiconductor

## Function Table

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | A | B | QA | QB | ... | QD |
| L | X | X | X | L | L | ... | L |
| H | ↓ | X | X | $Q_{A0}$ | $Q_{B0}$ | ... | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | ... | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | ... | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | ... | $Q_{Gn}$ |

Note: H: High level
L: Low level
X: Immaterial
↑: Low to high transition
↓: High to low transition
$Q_{AD}$, $Q_{B0}$...$Q_{H0}$: Outputs remain unchanged.
$Q_{An}$, $Q_{Bn}$...$Q_{Gn}$: Data shifted from the previous stage on a positive edge at the clock input.

## Pin Arrangement




(Top view)

## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | –0.5 to 7.0 | V | |
| Input voltage range*[1] | $V_I$ | –0.5 to 7.0 | V | |
| Output voltage range*[1, 2] | $V_O$ | –0.5 to $V_{CC}$ + 0.5 | V | Output: H or L |
| | | –0.5 to 7.0 | | $V_{CC}$: OFF |
| Input clamp current | $I_{IK}$ | –20 | mA | $V_I < 0$ |
| Output clamp current | $I_{OK}$ | ±50 | mA | $V_O < 0$ or $V_O > V_{CC}$ |
| Continuous output current | $I_O$ | ±25 | mA | $V_O$ = 0 to $V_{CC}$ |
| Continuous current through $V_{CC}$ or GND | $I_{CC}$ or $I_{GND}$ | ±50 | mA | |
| Maximum power dissipation at Ta = 25°C (in still air)*[3] | $P_T$ | 785 | mW | SOP |
| | | 500 | | TSSOP |
| Storage temperature | Tstg | –65 to 150 | °C | |

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

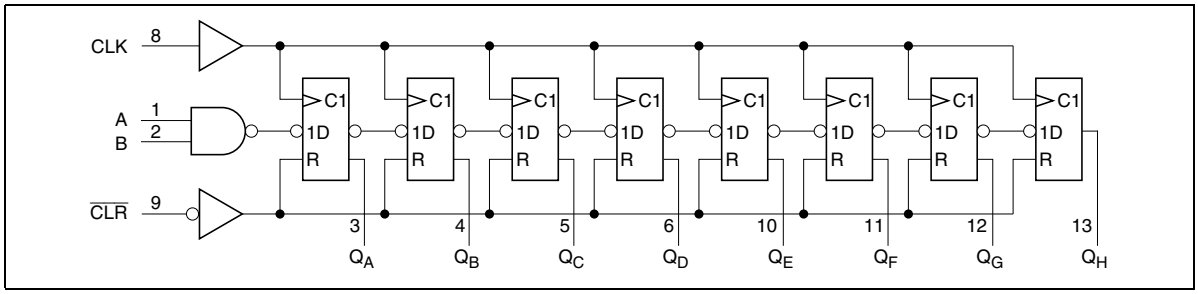
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

## Recommended Operating Conditions

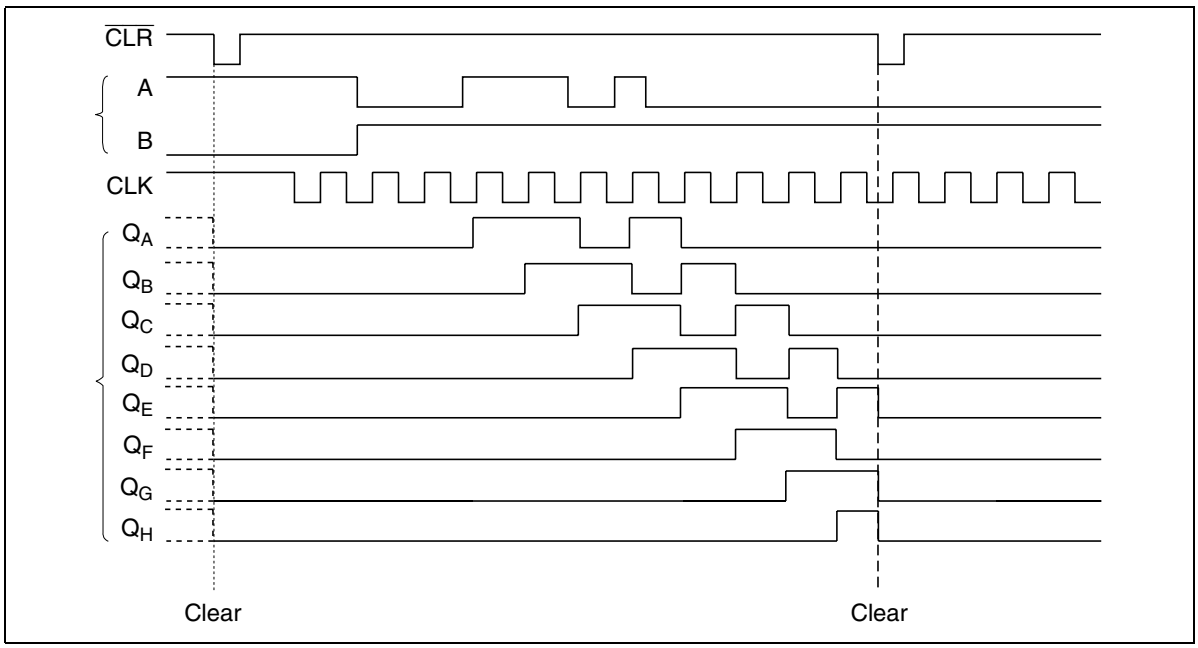
| Item | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Supply voltage range | $V_{CC}$ | 2.0 | 5.5 | V | |
| Input voltage range | $V_I$ | 0 | 5.5 | V | |
| Output voltage range | $V_O$ | 0 | $V_{CC}$ | V | H or L |
| Output current | $I_{OH}$ | — | –50 | µA | $V_{CC}$ = 2.0 V |
| | | — | –2 | mA | $V_{CC}$ = 2.3 to 2.7 V |
| | | — | –6 | | $V_{CC}$ = 3.0 to 3.6 V |
| | | — | –12 | | $V_{CC}$ = 4.5 to 5.5 V |
| | $I_{OL}$ | — | 50 | µA | $V_{CC}$ = 2.0 V |
| | | — | 2 | mA | $V_{CC}$ = 2.3 to 2.7 V |
| | | — | 6 | | $V_{CC}$ = 3.0 to 3.6 V |
| | | — | 12 | | $V_{CC}$ = 4.5 to 5.5 V |
| Input transition rise or fall rate | $\Delta t / \Delta v$ | 0 | 200 | ns/V | $V_{CC}$ = 2.3 to 2.7 V |
| | | 0 | 100 | | $V_{CC}$ = 3.0 to 3.6 V |
| | | 0 | 20 | | $V_{CC}$ = 4.5 to 5.5 V |
| Operating free-air temperature | Ta | –40 | 85 | °C | |

Note: Unused or floating inputs must be held high or low.

## Logic Diagram




## Timing Diagram



## DC Electrical Characteristics

- Ta = –40 to 85°C

| Item | Symbol | $V_{cc}$ (V)* | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | 2.0 | 1.5 | — | — | V | |
| | | 2.3 to 2.7 | $V_{CC} \times 0.7$ | — | — | | |
| | | 3.0 to 3.6 | $V_{CC} \times 0.7$ | — | — | | |
| | | 4.5 to 5.5 | $V_{CC} \times 0.7$ | — | — | | |
| | $V_{IL}$ | 2.0 | — | — | 0.5 | | |
| | | 2.3 to 2.7 | — | — | $V_{CC} \times 0.3$ | | |
| | | 3.0 to 3.6 | — | — | $V_{CC} \times 0.3$ | | |
| | | 4.5 to 5.5 | — | — | $V_{CC} \times 0.3$ | | |
| Output voltage | $V_{OH}$ | Min to Max | $V_{CC}$ – 0.1 | — | — | V | $I_{OL}$ = –50 µA |
| | | 2.3 | 2.0 | — | — | | $I_{OL}$ = –2 mA |
| | | 3.0 | 2.48 | — | — | | $I_{OL}$ = –6 mA |
| | | 4.5 | 3.8 | — | — | | $I_{OL}$ = –12 mA |
| | $V_{OL}$ | Min to Max | — | — | 0.1 | | $I_{OL}$ = 50 µA |
| | | 2.3 | — | — | 0.4 | | $I_{OL}$ = 2 mA |
| | | 3.0 | — | — | 0.44 | | $I_{OL}$ = 6 mA |
| | | 4.5 | — | — | 0.55 | | $I_{OL}$ = 12 mA |
| Input current | $I_{IN}$ | 0 to 5.5 | — | — | ±1 | µA | $V_I$ = 5.5 V or GND |
| Quiescent supply current | $I_{CC}$ | 5.5 | — | — | 20 | µA | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 |
| Output leakage current | $I_{OFF}$ | 0 | — | — | 5 | µA | $V_I$ or $V_O$ = 0 V to 5.5 V |
| Input capacitance | $C_{IN}$ | 3.3 | — | 2.2 | — | pF | $V_I$ = $V_{CC}$ or GND |

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## Switching Characteristics

- $V_{CC} = 2.5 \pm 0.2$ V

| | | Ta = 25°C | | | Ta = –40 to 85°C | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Max** | **Unit** | **Test Conditions** | **FROM (Input)** | **TO (Output)** |
| Maximum clock frequency | fmax | 55 | 105 | — | 50 | — | MHz | $C_L$ = 15 pF | | |
| | | 45 | 85 | — | 40 | — | | $C_L$ = 50 pF | | |
| Propagation delay time | $t_{PLH}/t_{PHL}$ | — | 9.2 | 17.6 | 1.0 | 20.0 | ns | $C_L$ = 15 pF | CLK | Q |
| | | — | 11.5 | 21.1 | 1.0 | 24.0 | | $C_L$ = 50 pF | | |
| | $t_{PHL}$ | — | 8.6 | 16.0 | 1.0 | 18.0 | | $C_L$ = 15 pF | $\overline{CLR}$ | |
| | | — | 10.8 | 19.5 | 1.0 | 22.0 | | $C_L$ = 50 pF | | |
| Setup time | $t_{su}$ | 6.5 | — | — | 8.5 | — | ns | | Data before CLK ↑ | |
| | | 3.0 | — | — | 3.0 | — | | | $\overline{CLR}$ inactive before CLK ↑ | |
| Hold time | $t_h$ | –0.5 | — | — | 0.0 | — | ns | | Data after CLK ↑ | |
| Pulse width | $t_w$ | 6.0 | — | — | 6.5 | — | ns | | $\overline{CLR}$ L | |
| | | 6.5 | — | — | 7.5 | — | | | CLK H or L | |

## Switching Characteristics (cont)

- $V_{CC} = 3.3 \pm 0.3$ V

| Item | Symbol | Ta = 25°C Min | Typ | Max | Ta = –40 to 85°C Min | Max | Unit | Test Conditions | FROM (Input) | TO (Output) |
|---|---|---|---|---|---|---|---|---|---|---|
| Maximum clock frequency | fmax | 80 | 155 | — | 65 | — | MHz | $C_L$ = 15 pF | | |
| | | 50 | 120 | — | 45 | — | | $C_L$ = 50 pF | | |
| Propagation delay time | $t_{PLH}/t_{PHL}$ | — | 6.4 | 12.8 | 1.0 | 15.0 | ns | $C_L$ = 15 pF | CLK | Q |
| | | — | 8.3 | 16.3 | 1.0 | 18.5 | | $C_L$ = 50 pF | | |
| | $t_{PHL}$ | — | 6.0 | 12.8 | 1.0 | 15.0 | | $C_L$ = 15 pF | $\overline{CLR}$ | |
| | | — | 7.9 | 16.3 | 1.0 | 18.5 | | $C_L$ = 50 pF | | |
| Setup time | $t_{su}$ | 5.0 | — | — | 6.0 | — | ns | | Data before CLK ↑ | |
| | | 2.5 | — | — | 2.5 | — | | | $\overline{CLR}$ inactive before CLK ↑ | |
| Hold time | $t_h$ | 0.0 | — | — | 0.0 | — | ns | | Data after CLK ↑ | |
| Pulse width | $t_w$ | 5.0 | — | — | 5.0 | — | ns | | $\overline{CLR}$ L | |
| | | 5.0 | — | — | 5.0 | — | | | CLK H or L | |

## Switching Characteristics (cont)

- $V_{CC} = 5.0 \pm 0.5$ V

| | | Ta = 25°C | | | Ta = –40 to 85°C | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Max** | **Unit** | **Test Conditions** | **FROM (Input)** | **TO (Output)** |
| Maximum clock frequency | fmax | 125 | 220 | — | 105 | — | MHz | $C_L$ = 15 pF | | |
| | | 85 | 165 | — | 75 | — | | $C_L$ = 50 pF | | |
| Propa-gation delay time | $t_{PLH}/t_{PHL}$ | — | 4.5 | 9.0 | 1.0 | 10.5 | ns | $C_L$ = 15 pF | CLK | Q |
| | | — | 6.0 | 11.0 | 1.0 | 12.5 | | $C_L$ = 50 pF | | |
| | $t_{PHL}$ | — | 4.2 | 8.6 | 1.0 | 10.0 | | $C_L$ = 15 pF | $\overline{CLR}$ | |
| | | — | 5.8 | 10.6 | 1.0 | 12.5 | | $C_L$ = 50 pF | | |
| Setup time | $t_{su}$ | 45 | — | — | 4.5 | — | ns | | Data before CLK ↑ | |
| | | 2.5 | — | — | 2.5 | — | | | $\overline{CLR}$ inactive before CLK ↑ | |
| Hold time | $t_h$ | 1.0 | — | — | 1.0 | — | ns | | Data after CLK ↑ | |
| Pulse width | $t_w$ | 5.0 | — | — | 5.0 | — | ns | | $\overline{CLR}$ L | |
| | | 5.0 | — | — | 5.0 | — | | | CLK H or L | |

## Operating Characteristics

- $C_L$ = 50 pF

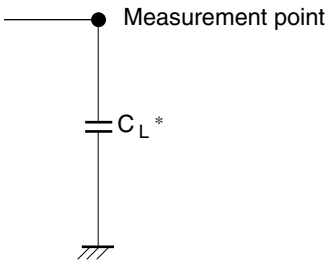
| | | | Ta = 25°C | | | | |
|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **$V_{cc}$ (V)** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| Power dissipation capacitance | $C_{PD}$ | 3.3 | — | 48.1 | — | pF | f = 10 MHz |
| | | 5.0 | — | 47.5 | — | | |

## Noise Characteristics

- $C_L$ = 50 pF

| | | | Ta = 25°C | | | | |
|---|---|---|---|---|---|---|---|
| **Item** | **Symbol** | **$V_{cc}$ (V)** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| Quiet output, maximum dynamic $V_{OL}$ | $V_{OL (P)}$ | 3.3 | — | 0.3 | 0.8 | V | |
| Quiet output, minimum dynamic $V_{OL}$ | $V_{OL (V)}$ | 3.3 | — | –0.2 | –0.8 | | |
| Quiet output, minimum dynamic $V_{OH}$ | $V_{OH (V)}$ | 3.3 | — | 3.1 | — | | |
| High-level dynamic input voltage | $V_{IH (D)}$ | 3.3 | 2.31 | — | — | V | |
| Low-level dynamic inout voltage | $V_{IL (D)}$ | 3.3 | — | — | 0.99 | | |

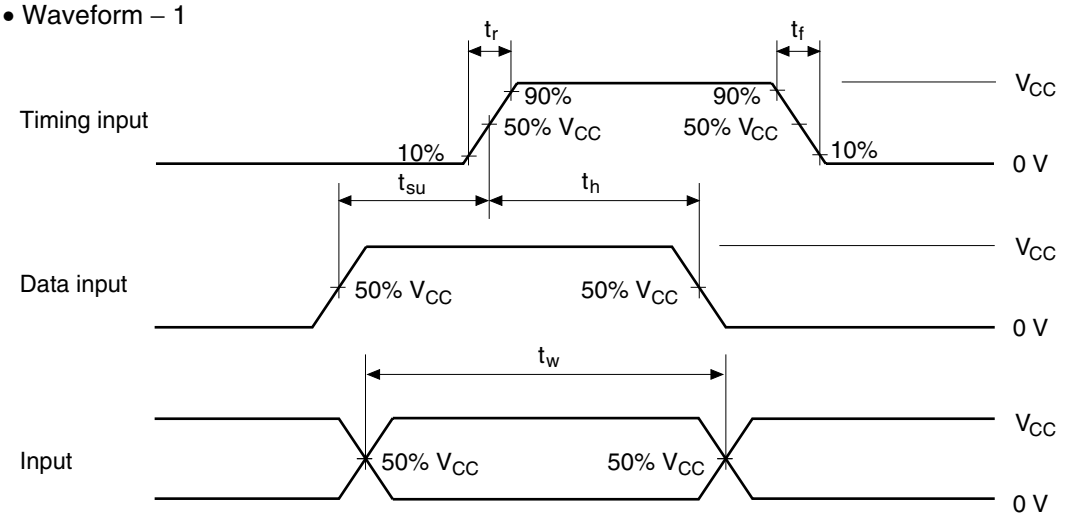
## Test Circuit



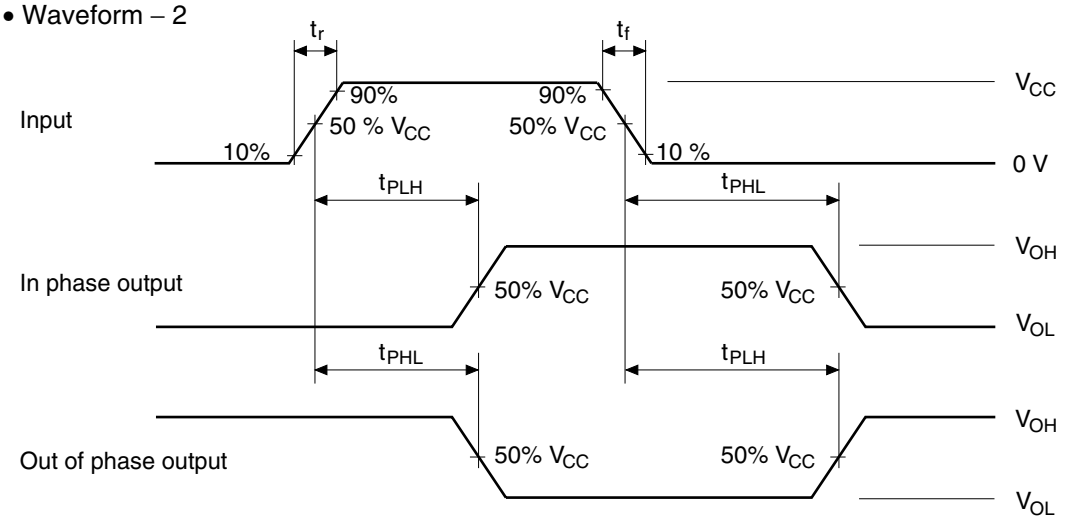

Note: $C_L$ includes the probe and jig capacitance.

## Waveform

• Waveform – 1




• Waveform – 2

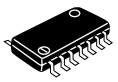


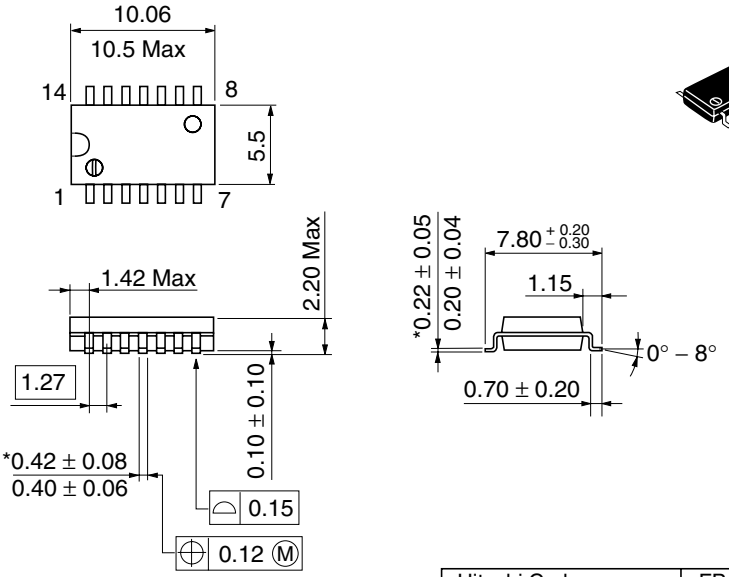

Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, $t_r \leq 3$ ns, $t_f \leq 3$ ns
2. The output are measured one at a time with one transition per measurement.

## Package Dimensions

As of January, 2001

Unit: mm

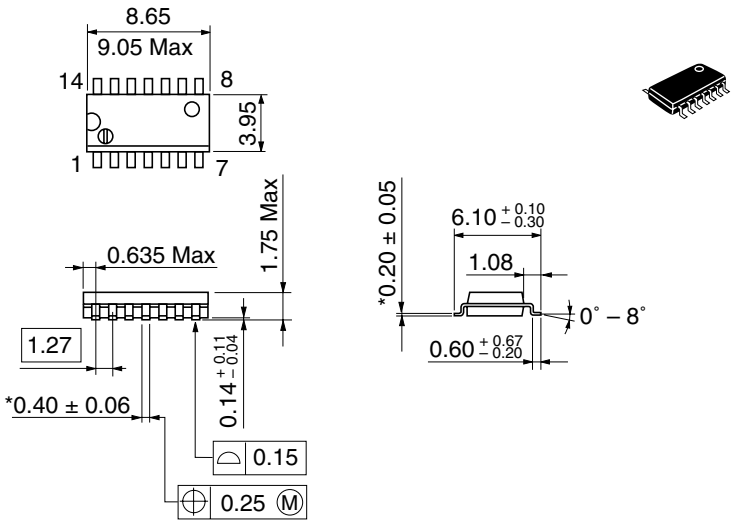





*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Hitachi Code | FP-14DA |
| JEDEC | — |
| EIAJ | Conforms |
| Mass (reference value) | 0.23 g |

Unit: mm

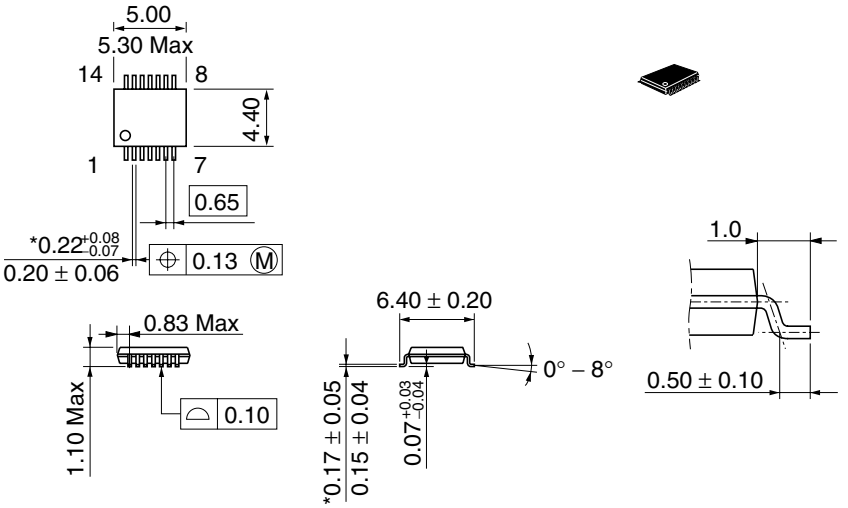



| | |
|---|---|
| Hitachi Code | FP-14DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 0.13 g |

*Pd plating

As of January, 2001

Unit: mm




*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Hitachi Code | TTP-14D |
| JEDEC | — |
| EIAJ | — |
| Mass (reference value) | 0.05 g |

## Disclaimer

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as in aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safe devices, so that the equipment incorporating the Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

## Sales Offices

HITACHI

**Hitachi, Ltd.**
Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL http://www.hitachisemiconductor.com/

**For further information write to:**

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://semiconductor.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
URL : http://semiconductor.hitachi.com.hk



Colophon 5.0