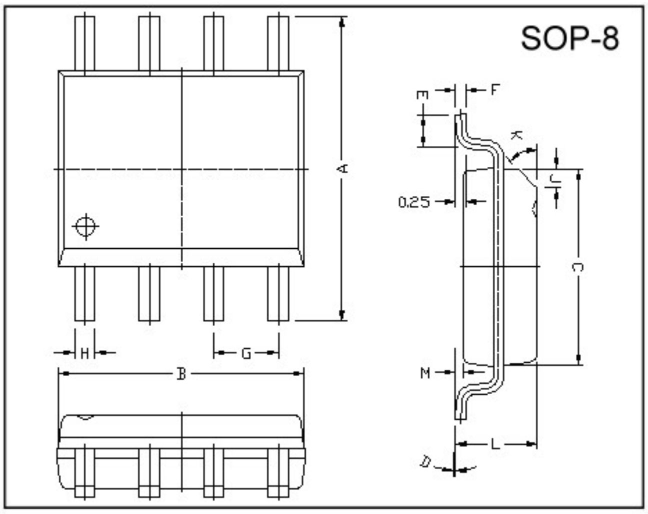
GSCNE555 SINGLE TIMER

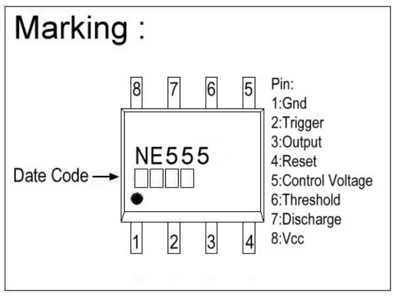
Description
The GSCNE555 is a highly stable timer integrated circuit. It can be operated in Astable mode and Monostable mode. With monostable operation, the time delay is controlled by one external and one capacitor. With a stable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

Features
- High current driver capability (=200mA)
- Adjustable duty cycle
- Timing form μSec to Hours
- Turn off time less than 2μSec

Applications
- Precision timing
- Pulse generation
- Time delay generation

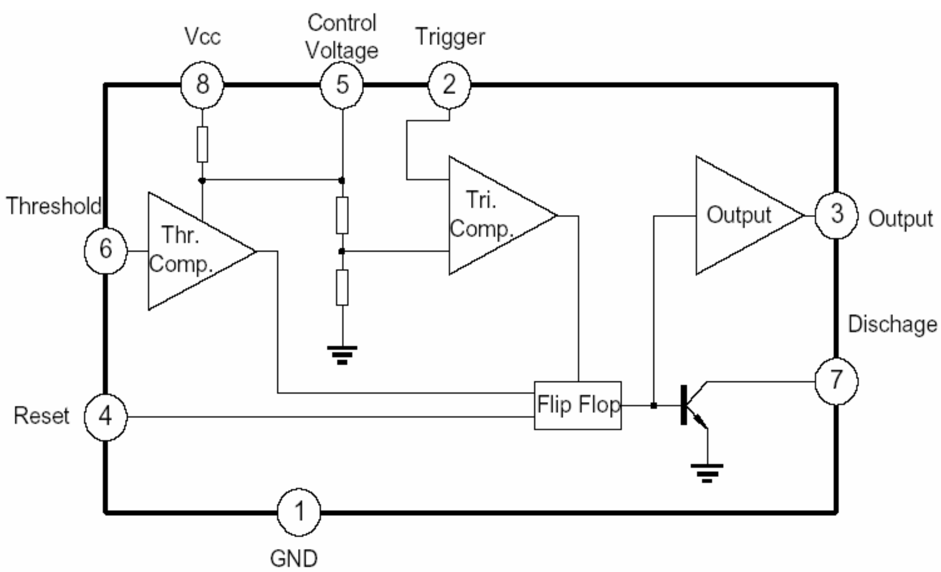
Package Dimensions





REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Block Diagram and Simplified Application & Pin Configuration



Absolute Maximum Ratings (Ta=25℃)

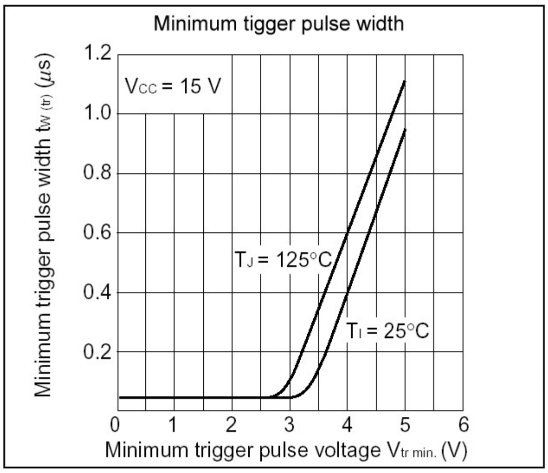
Parameter	Symbol	Value	Unit
Supply Voltage	VCC	16	V
Output Current	IO	200	mA
Power Dissipation	Pd	440	mW
Lead Temperature	Tlead	300	℃
Operating Temperature	Topr	0 ~ 70	℃
Storage Temperature	Tstg	-65 ~ 150	℃

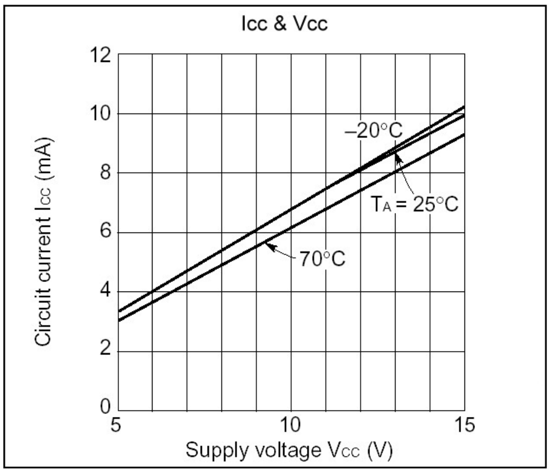
Electrical Characteristics (TA=25℃ VCC=5 ~ 15V)

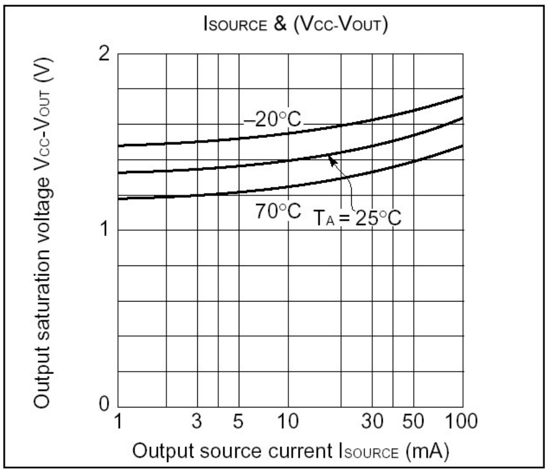
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	VCC		4.5	-	16	V
Supply Current (Note 1)	ICC	VCC=5V, RL=∞	-	3	6	mA
		VCC=15V, RL=∞	-	10	15	mA
Timing Error(monostable)						
Initial Accurary (Note 1)	ACCUR	RA=1k to 100kΩ	-	1.0	-	%
Drift with Temperature	△t/△T	C=0.1μF	-	50	-	ppm/℃
Drift with Supply Voltage	△t/△VCC		-	0.1	-	%/V
Timing Error(astable)						
Initial Accurary (Note 1)	ACCUR	RA=1k to 100kΩ	-	2.25	-	%
Drift with Temperature	△t/△T	C=0.1μF	-	150	-	ppm/℃
Drift with Supply Voltage	△t/△VCC		-	0.3	-	%/V
Control Voltage	VC	VCC=15V	9.0	10.0	11.0	V
		VCC=5V	2.6	3.33	4.0	V
Threshold Voltage	VTH	VCC=15V	9.2	10.0	10.8	V
		VCC=5V	3.1	3.33	3.55	V
Threshold Current (Note 3)	ITH		-	0.1	0.25	μA
Trigger Voltage	Vtr	VCC=5V	1.1	1.67	2.2	V
		VCC=15V	4.5	5	5.6	V
Trigger Current	Itr	Vtr=0	-	-	2.0	μA
Reset Voltage	Vrst		0.4	0.7	1.0	V
Reset Current	Irst		-	0.1	0.4	mA
Low Output Voltage	VOL	VCC=15V, Isink=10mA	-	0.06	0.25	V
		VCC=15V, Isink=50mA	-	0.3	0.75	
		VCC=5V, Isink=5mA	-	0.05	0.35	
High Output Voltage	VOH	VCC=15V, Isource=200mA	-	12.5	-	V
		VCC=15V, Isource=100mA	12.75	13.3	15	
		VCC=5V, Isource=100mA	2.75	3.3	5	
Reset Time of Output	tR		-	100	-	nSec
Fall Time of Output	tF		-	100	-	nSec
Discharge leakage Current	ILKG		-	20	100	nA

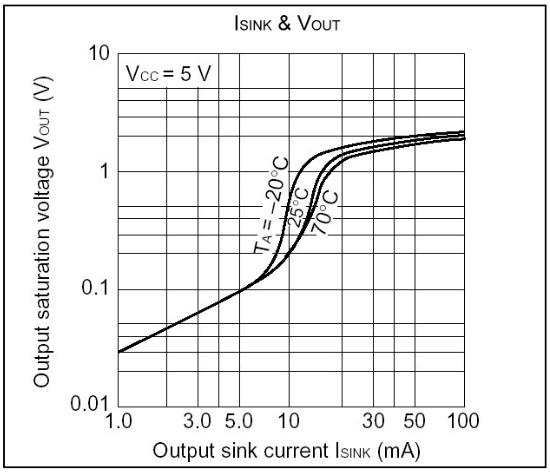
Note1: Supply current when output is high typically 1mA less at VCC=5V.
Note2: Tested at VCC=5V and VCC=15V.
Note3: This will determine the maximum value of RA+RB for 15V operation, the maximum total is R=20MΩ, and for 5V operation the maximum total is R=6.7MΩ.

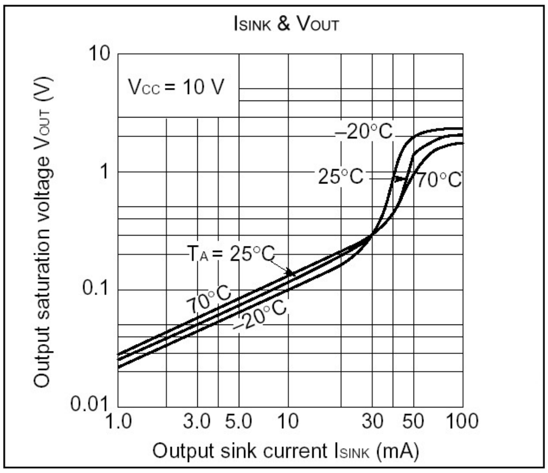
Characteristics Curve

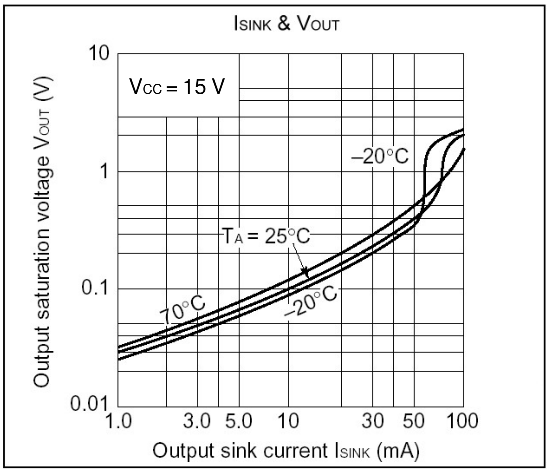


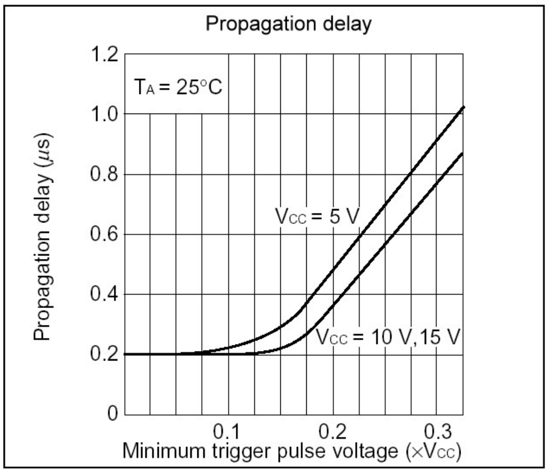


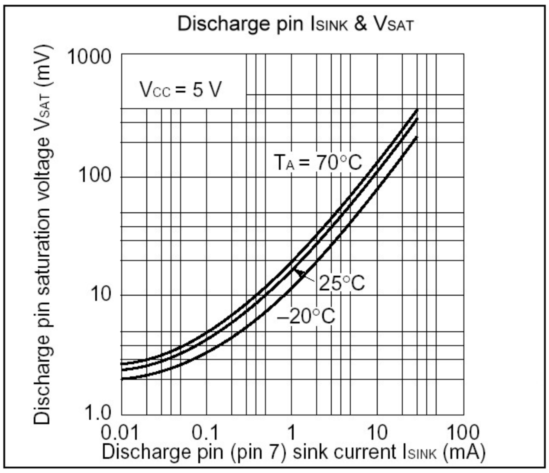


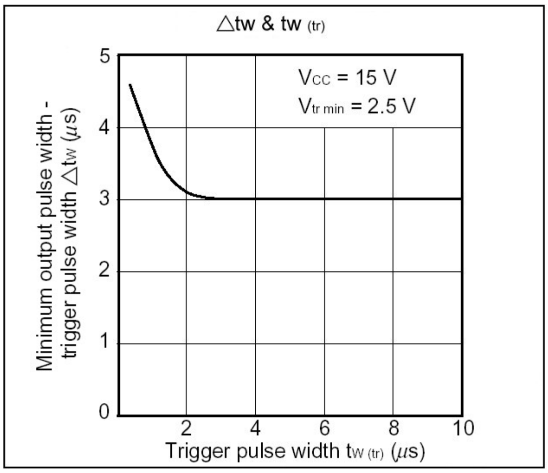


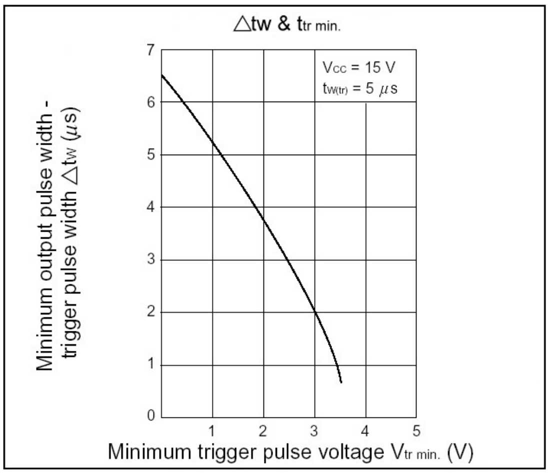




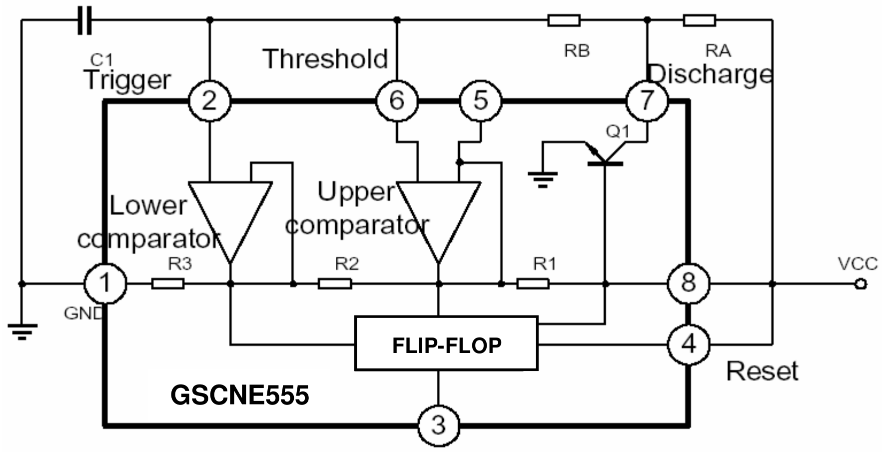

Propagation delay
T_A = 25°C
V_{CC} = 5 V
V_{CC} = 10 V,15 V
Propagation delay (μs)
Minimum trigger pulse voltage (×V_{CC})


Discharge pin I_{SINK} & V_{SAT}
V_{CC} = 5 V
T_A = 70°C
25°C
–20°C
Discharge pin saturation voltage V_{SAT} (mV)
Discharge pin (pin 7) sink current I_{SINK} (mA)


△tw & tw (tr)
V_{CC} = 15 V
$V_{tr\ min}$ = 2.5 V
Minimum output pulse width - trigger pulse width △tw (μs)
Trigger pulse width $t_{W\ (tr)}$ (μs)


△tw & $t_{tr\ min.}$
V_{CC} = 15 V
$t_{W(tr)}$ = 5 μs
Minimum output pulse width - trigger pulse width △tw (μs)
Minimum trigger pulse voltage $V_{tr\ min.}$ (V)

Application Circuit



Application Notes

The application circuit shows astable mode configuration.

Pin 6 (Threshold) is tied to Pin 2 (Trigger) and Pin 4 (Reset) is tied to VCC (Pin 8). The external capacitor C1 of Pin 6 and Pin 2 charges through RA, RB and discharge through RB only. In the internal circuit of GSCNE555, one input of the upper comparator is at voltage of 2/3VCC (R1=R2=R3), another input is connected to Pin 6. As soon as C1 is charging to higher than 2/3VCC, transistor Q1 is turned ON and discharge C1 to collector voltage of transistor Q1. Therefore, the flip-flop circuit is reset and output is low. One input of lower comparator is at voltage of 1/3VCC, discharge transistor Q1 turn off and C1 charges through RA and RB. Therefore, flip-flop circuit is set output high.

That is, when C1 charges through RA and RB, output is high and when C1 discharge through RB, output is low. The charge time (output is high) t1 is 0.693 (RA+RB) C1 and the discharge time (output is low) T2 is 0.693RB*C1.

$$\ln\left(\frac{Vcc-\frac{1}{3}Vcc}{Vcc-\frac{2}{3}Vcc}\right)=0.693$$

T1=0.693*(RA+RB)*C1

Thus the total period time T is given by

T2=0.693*RB*C1

T=T1+T2=0.693(RA+2RB)*C1

Then the frequency of astable mode is given by

$$f=\frac{1}{T}=\frac{1.44}{(RA+2RB)*C1}$$

The duty cycle is given by

$$D.C.=\frac{T2}{T}=\frac{RB}{RA+2RB}$$

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