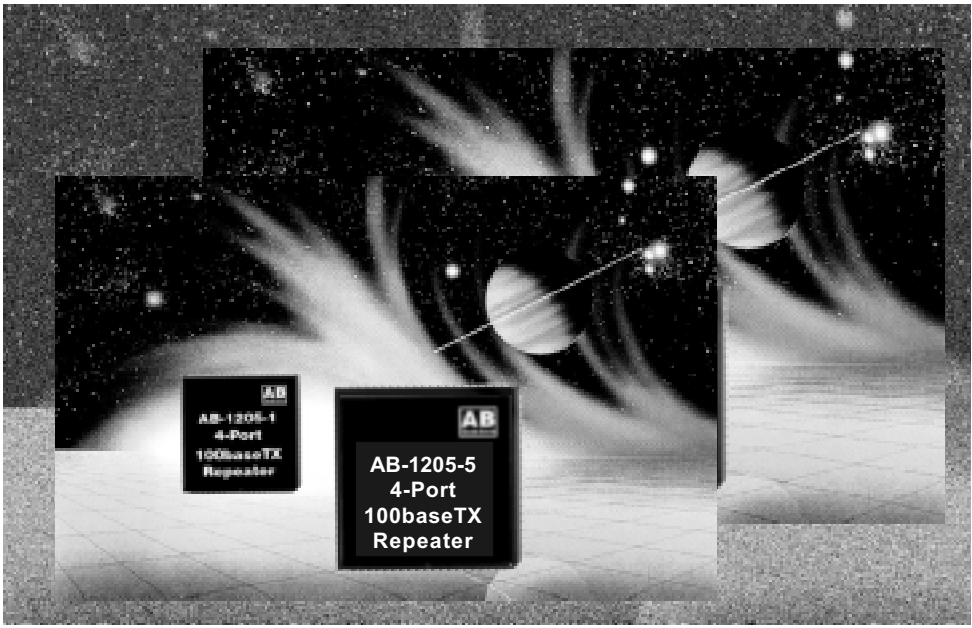
AB-1205-5

4 Port Cascadeable 100base and ATM Repeater Hub



Product Specification

AB Semicon AB1205-5

100base and ATM
Repeater Hub
Product Specification

Disclaimer

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AB-1205-5

100base and ATM
4 Port Repeater

Features:

* 4 ports for or AMD's FDDI chip sets and GEC's NWK914
* Local bi-directional high-speed bus for daisychaining
* Compatible with 100base TX, T4 and T6
* Compatible with 100base VG
* 80 pin PQFP package
* Low Power C-Mos Technology 0.8micron

INTRODUCTION

This repeater chip allows the connection of an AMD 79865 and 79866 chipset together with NSM DP83223 as the Physical Layer chip as well as being able to use the GEC NWK 914 or AB Semicon AB10100PHY which can replace the AMD and National chip set giving a maximum in flexibility. It can process 4 ports simultaneously in half duplex. The encryption and decryption circuit is built into each of the channels. A local bus allows daisychaining of any number of devices.

Chip Structure

The chip contains four high-speed 5bit channels and the control logic for the physical layer interface. Each channel has its own encryption and decryption circuit for circuit simplicity and reduced EMI. Error arbitration logic and collision detection which is also available on output pins on the chip which are capable of driving LEDs directly. There are additional LED outputs to indicate TX or RX data.

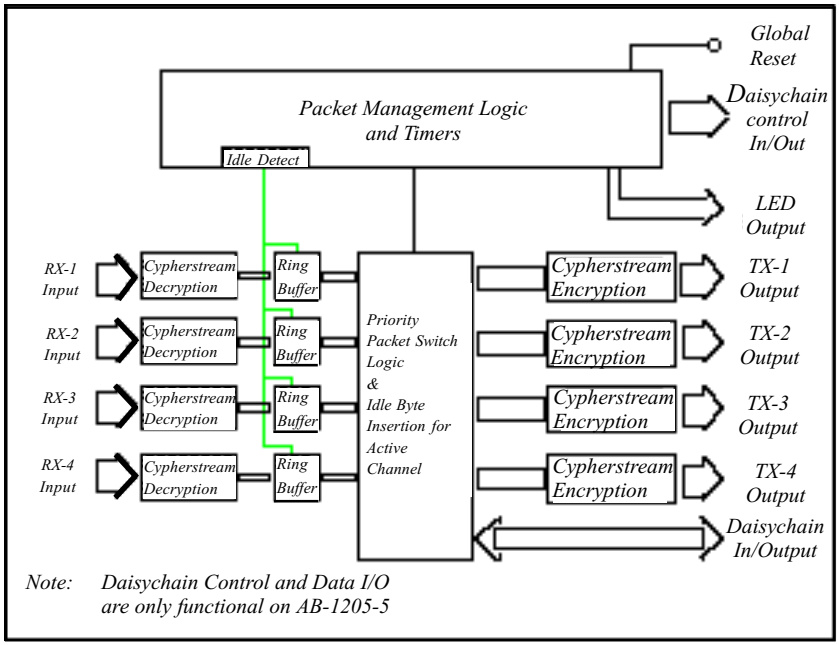


Figure 1
Functional Block Diagram

APPLICATIONS

The chip can be used in many different applications where random encryption and decryption is required to achieve a semi spread spectrum use of copper wire to reduce RFI emitted from the cable. It is most powerful for repeater devices such as 4, 8 or 16 port or any multiple of 4 ports, HUB devices. Such applications include 100baseTX repeaters.

Figure 2 gives an overview of low cost repeater applications for which this chip is suitable. Such a repeater can be used in Workgroup or Server-based environments. The data is fully transparently distributed through the Network.

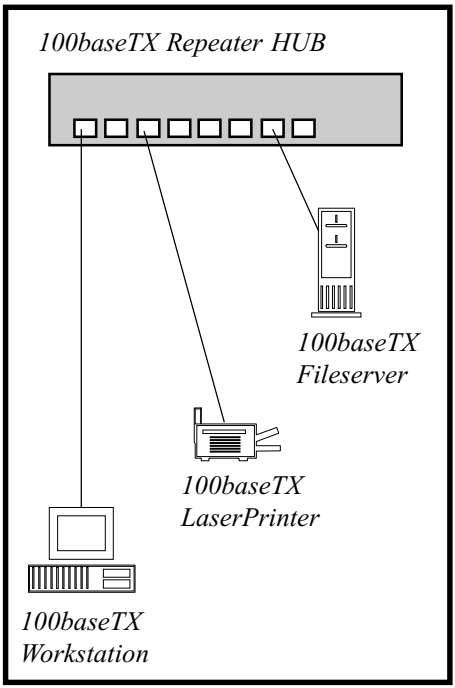


Figure 2

EXAMPLE for a 4 Port Repeater

Figure 3 shows a 4 port repeater with an extension connector to daisychain any number of 4 port repeaters.

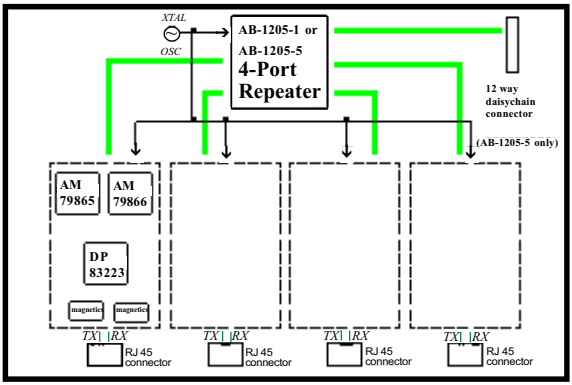


Figure 3

Interconnection of AB1205-5 and AB10100PHY Physical Layer

The diagram below shows how the signals between AB1205-5 and AB10100PHY are interconnected for a single port. This interconnection is repeated for the remaining 3 ports, please also refer to the AB10100PHY Product Specification.

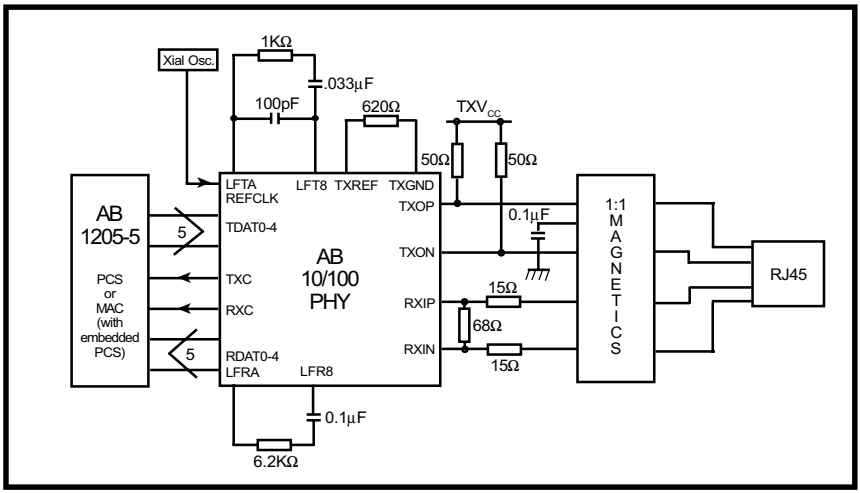


Fig 6. Connection of AB10/100PHY to AB1205-5

Clock Distribution Circuit

The following diagram shows how the clock is distributed. To assure that the clock is arriving at the same time on all channels, a ˙244 is used to re-shape the clock signal for each channel.

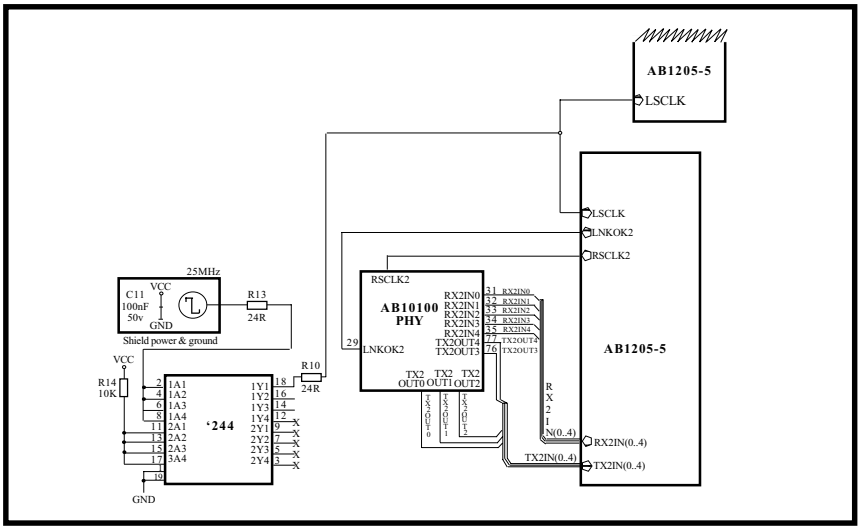
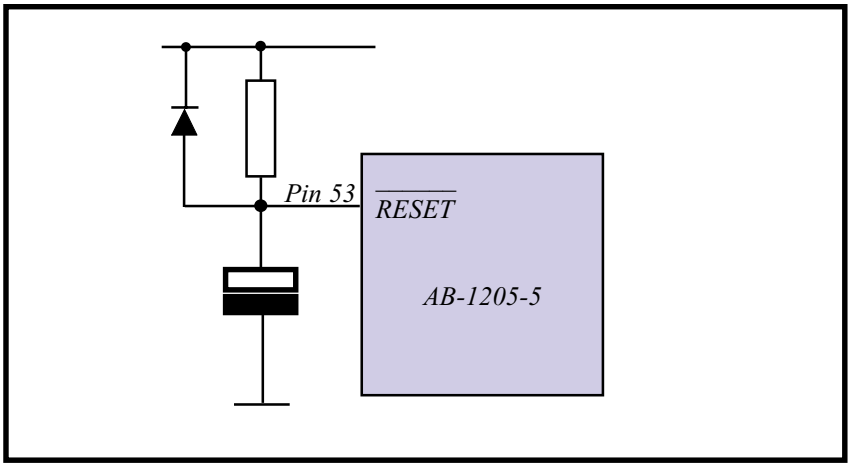


Diagram showing clock distribution

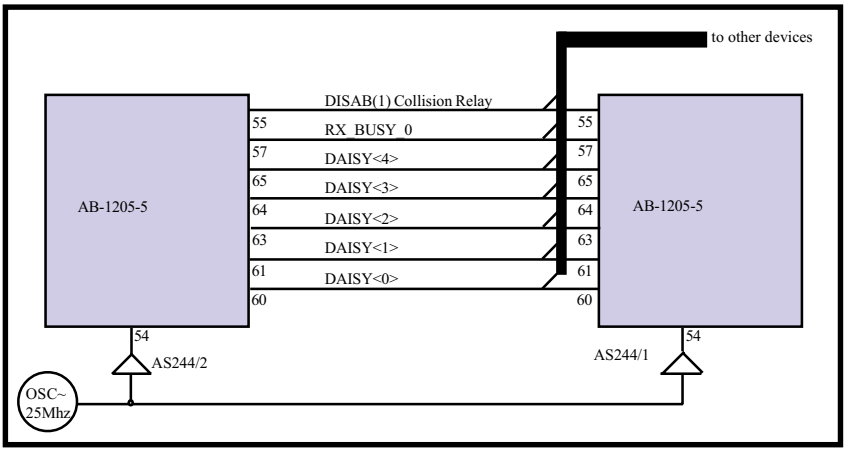
Note: When daisychaining the AB1205-5 the remaining buffers of the ˙244 may be used to re-generate the clock signal.

Reset circuitry for AB-1205-5

The following diagram shows the reset circuit for the AB-1205-5 four port and cascadeable hub chip.



Reset Circuit for AB-1205-5



Daisychaining the AB-1205-5

Thermal Characteristics for AB1205-5

This device is supplied in a plastic Quad Flat Pack with a pin count of 80. In this configuration, it has a thermal resistance (0_{JA} - Junction-to-Ambient Measurement) of 85 °C/W in an Alloy 42 Lead Frame with a value of 68 °C/W in a Copper Lead Frame.

As this device is currently supplied in the Alloy Lead Frame, only that figure has been used in the following calculations.

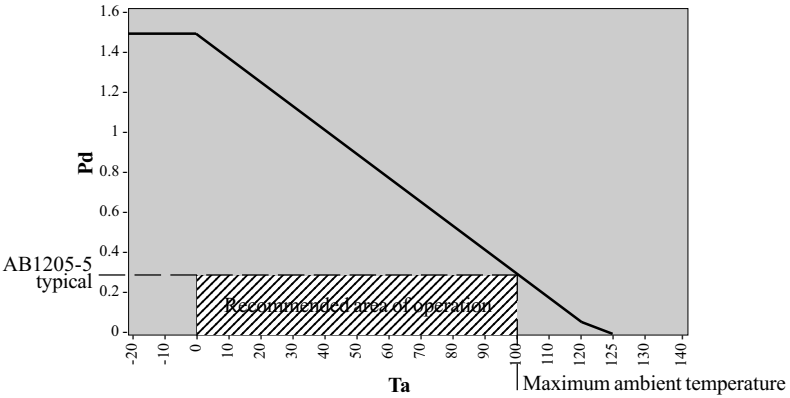
The Power Dissipation (Pd) of the device is calculated as follows:

$$Pd + \frac{T_J - T_A}{0_{JA}}$$

Thus the Power Dissipation is 1.2 Watts at an ambient of 25 °C and 650 mW at 70 °C.

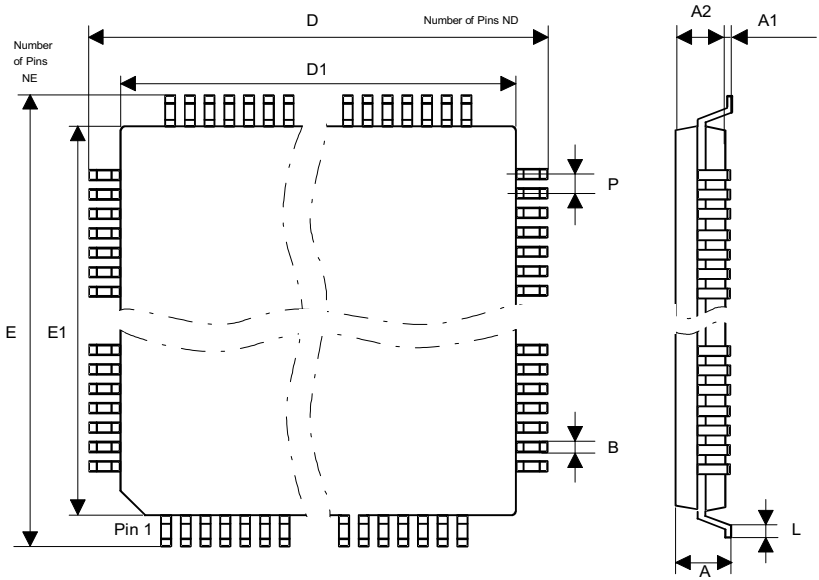
The following plot shows the variation of Power Dissipation with ambient:

Power Dissipation of AB1205-5 typical 300mW



A value of T_J max of 125 °C was used. The range of T_J is -40 to 125 °C.

Packaging information



	80 ◆ LEAD		
	MIN.	NOM.	MAX.
A	2.82	3.07	3.32
A1	0.25	0.35	0.45
A2	2.57	2.72	287
D	23.00	23.20	23.40
D1	19.90	20.00	20.10
E	17.00	17.20	17.40
E1	13.90	14.00	14.10
L	0.65	0.75	0.95
P		0.80	
B	0.25	0.35	0.45
ND		24	
NE		16	

I/O Pin Assignment

Pin ID	*Signal*	*Designator*
1	*GND*	*Ground*
2	*NC*	
3	*NC*	
4	*Output*	*TX3_OUT3*
5	*Output*	*TX3_OUT4*
6	*Output*	*TX4_OUT0*
7	*Vcc*	*Power*
8	*Output*	*TX4_OUT1*
9	*Output*	*TX4_OUT2*
10	*Output*	*TX4_OUT3*
11	*Output*	*TX4_OUT4*
12	*Output*	*-LINK4-(LED)*
13	*Output*	*-LED3-(LED)*
14	*Output*	*-LINK2-(LED)*
15	*Output*	*-LINK1-(LED)*
16	*Output*	*-REC4-(LED)*
17	*Output*	*-REC3-(LED)*
18	*Output*	*-REC2-(LED)*
19	*GND*	*Ground*
20	*Output*	*-REC1-(LED)*
21	*Input*	*LINKOK1*
22	*Input*	*RSCLK1*
23	*Vcc*	*Power*
24	*Input*	*RX1_IN0*
25	*Input*	*RX1_IN1*

I/O Pin Assignment

Pin ID	*Signal*	*Designator*
26	*Input*	*RX1_IN2*
27	*Input*	*RX1_IN3*
28	*Input*	*RX1_IN4*
29	*Input*	*LINKOK2*
30	*Input*	*RSCLK2*
31	*Input*	*RX2_IN0*
32	*Input*	*RX2_IN1*
33	*Input*	*RX2_IN2*
34	*Input*	*RX2_IN3*
35	*Input*	*RX2_IN4*
36	*Input*	*-LINKOK3-*
37	*Input*	*-RSCLK3-*
38	*Input*	*RX3IN0*
39	*Input*	*RX3IN1*
40	*Input*	*RX3IN2*
41	*Input*	*RX3IN3*
42	*Vdd*	*Power (Core)*
43	*GND*	*Ground*
44	*Input*	*RX3IN4*
45	*Input*	*-LINKOK4-*
46	*GNDc*	*Ground (Core)*
47	*Input*	*RSCLK4*
48	*Input*	*RX4_IN0*
49	*Input*	*RX4_IN1*
50	*Input*	*RX4_IN2*

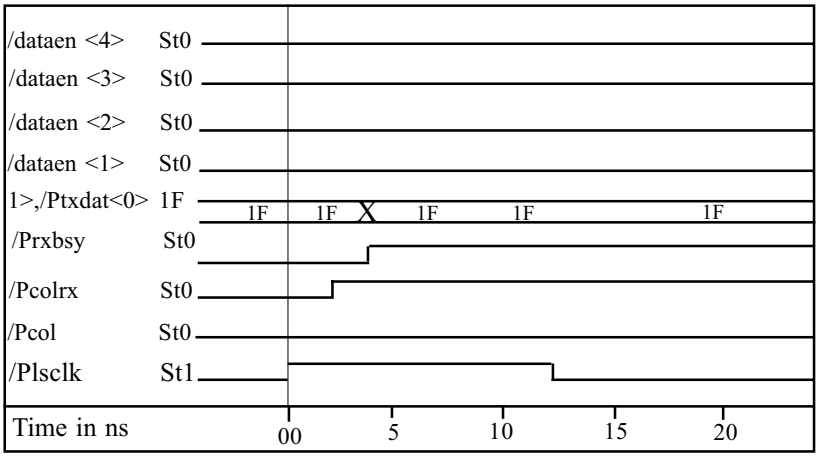
I/O Pin Assignment

Pin ID	*Signal*	*Designator*
51	*Input*	*RX4_IN3*
52	*Input*	*RX4_IN4*
53	*Input*	*-RESET-*
54	*Input*	*LSCLK*
55	*Output*	*-DISAB1-(Col)*
56	*N/C*	*N/C*
57	*Input/Output*	*RX_BUSY_0*
58	*Vcc*	*Power*
59	*GND*	*Ground*
60	*Input/Output*	*DAISY 0*
61	*Input/Output*	*DAISY 1*
62	*Vcc*	*Power*
63	*Input/Output*	*DAISY 2*
64	*Input/Output*	*DAISY 3*
65	*Input/Output*	*DAISY 4*
66	*GND*	*Ground*
67	*Output*	*TX1_OUT0*
68	*Output*	*TX1_OUT1*
69	*Output*	*TX1_OUT2*
70	*Output*	*TX1_OUT3*
71	*Output*	*TX1_OUT4*
72	*Output*	*TX2_OUT0*
73	*Output*	*TX2_OUT1*
74	*Vcc*	*Power*
75	*Output*	*TX2_OUT2*

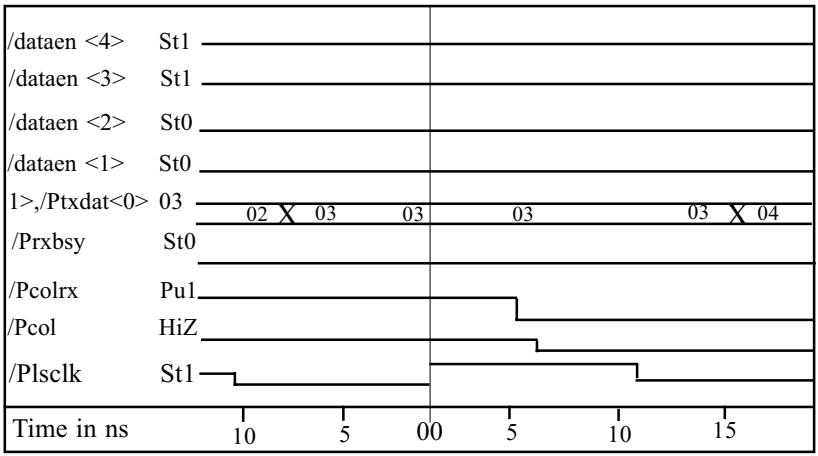
I/O Pin Assignment

Pin ID	*Signal*	*Designator*
76	*Output*	*TX2_OUT3*
77	*Output*	*TX2_OUT4*
78	*Output*	*TX3_OUT0*
79	*Output*	*TX3_OUT1*
80	*Output*	*TX3_OUT2*

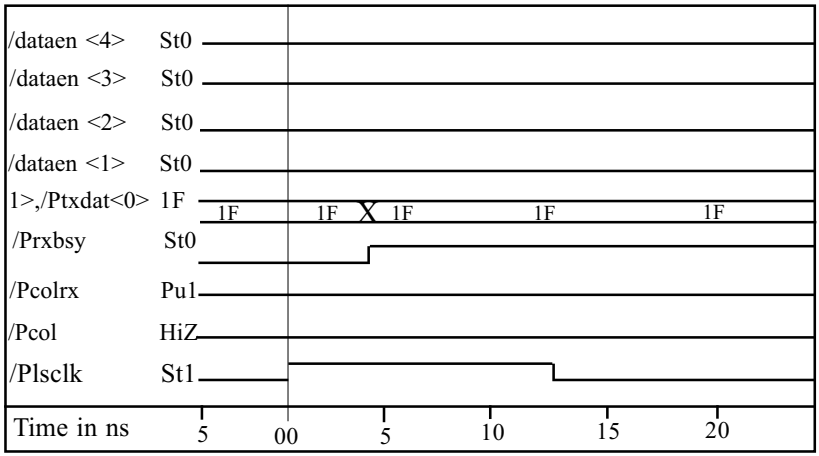
Clock to Pcolrx inactive at end of collided packet



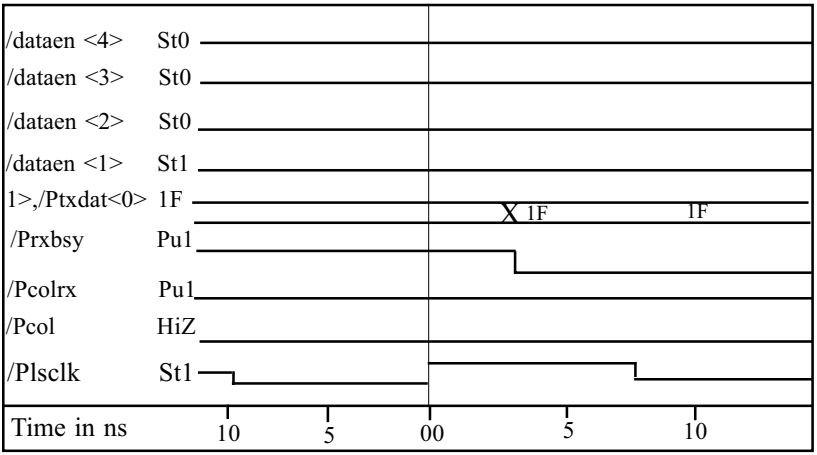
Clock to Pcolrx and Pcol active when a collision occurs



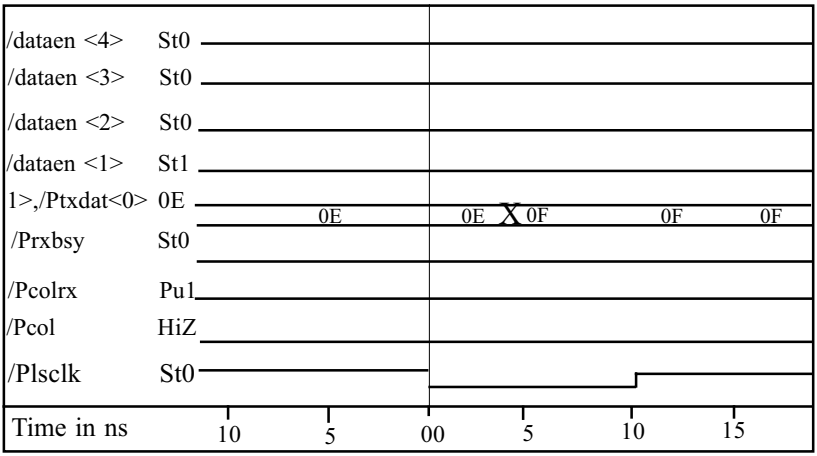
Clock to Prxbsy high and byway data disable at end of packet



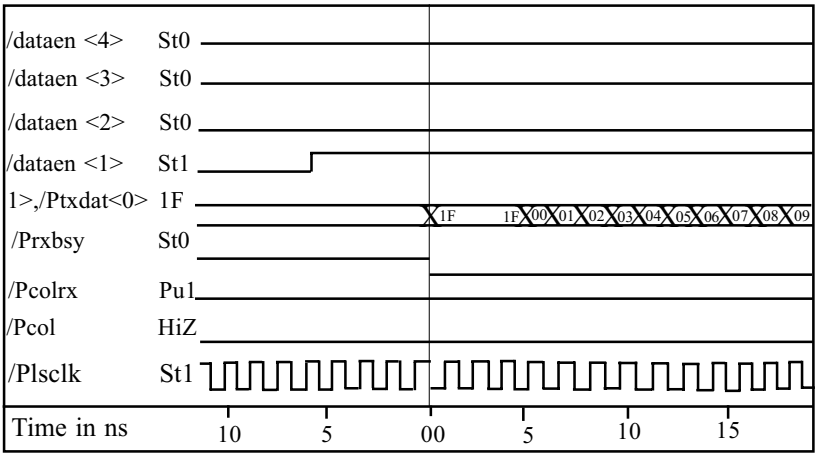
Clock to Prxbsy low and by way data enable at beginning of packet



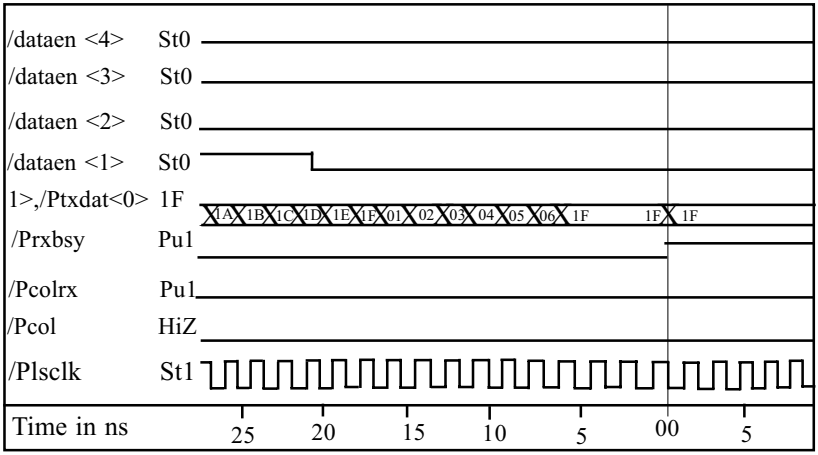
Clocking of byway data



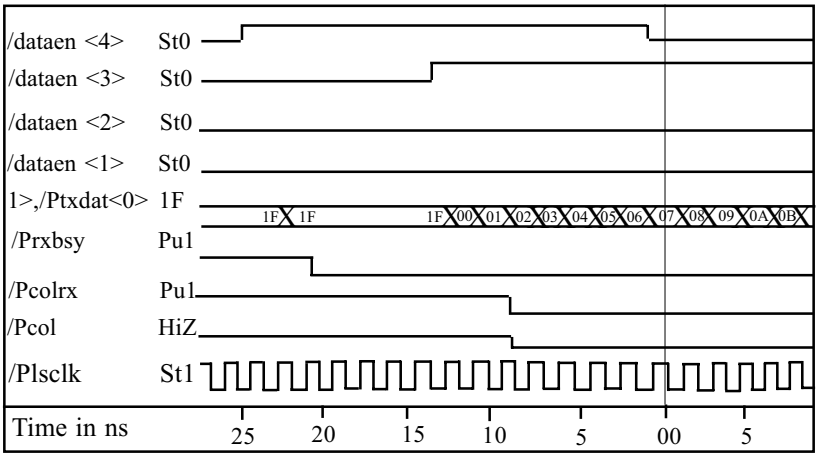
Beginning of packet
(1 channel starts transmission)



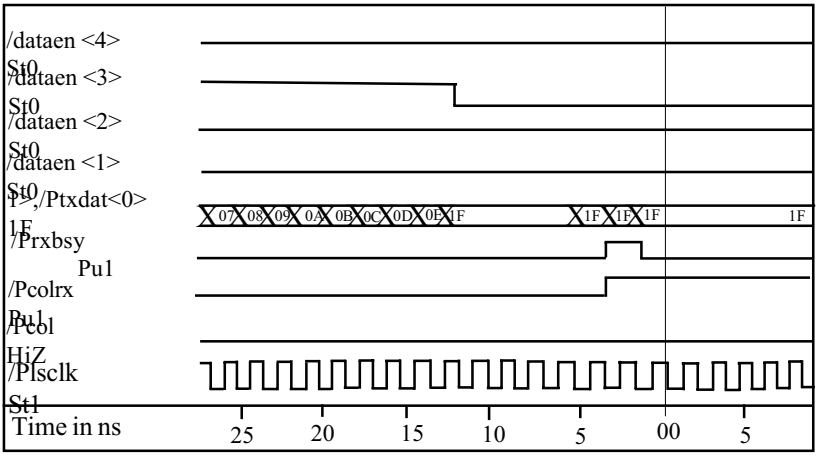
End of packet
(1 channel ends transmission)



Beginning of collision
(two channels try to transmit simultaneously)



End of collision
(the collided channels ceased transmission)



Electrical Specification

Vcc	*+5V ± 10%*
Vdd (Core)	*+5V ± 10%*
Icu	*50 mA (typical) 60 mA (max)*
GND and GNDc	*0V*
Input - Low	*< 0.7V*
Input - High	*≥ 1.8V*
Output - Low	*< 0.6V*
Output - High	*≥ 2.6V*
Input - Load	*5 gates*
LSCLK	*25 Mhz*

Operating Temperature:
Range 0℃ - 70℃
Humidity 90% (Non condensing)

Storage Temperature:
Range -10℃ - +80℃
Humidity 95% (Non condensing)

Product has to be used within 6-7 hours after unpacking.

AB Semicon Inc.
8305 Highway 71 West
Austin
Texas 78735
USA
Tel: +1 512 288 6750
Fax: +1 512 288 7676

AB Semicon Limited
AB Semicon House
62 Victoria Road
Burgess Hill
West Sussex
RH15 9LH
Tel: +44 1444 870408
Fax: +44 1444870452
www.ab-semicon.com

Distributed in Japan
Rikei Corporation
1-26-2 Nishi-Shinjuku
Shinjuku-Ku
Tokyo 163-05
Japan
Tel: +81 3 3345 2189
Fax: +81 3 3344 3949