Application Note	T-55343GD035JU-LW-ADN	Date	July 21, 2008
		REV	0

Application Note
T-55343GD035JU-LW-ADN
(3.5inch TFT Transmissive)

OPTREX CORPORATION PM Division

Revision	Date	Approval	Check	Issue	Modification
0	July 21, '08	Nakazawa	Okamoto	Yuchi	First edition

Index

1. Application

This application note applies to TFT LCD Module（T-55343GD035JU-LW-ADN

Please see the detail spec at the specification sheet of this LCD Module.

2. General Specifications

Item	Specification	
Screen Size	3.5Inches（8.9cm diagonal）	
Active Area	70.08(W) × 52.56(H) mm	
Display format	320(W) × 3[R,G,B] × 240(H)	
Pixel Size	0.073(W) × 3[R,G,B] × 0.219(H)mm	
Pixel Arrangement	RGB-Stripe	
Color Depth	16M Color	
Display Mode	Normally White	
Viewing Direction	12O'color（Angle of Least Color Inversion）	
Surface Treatment	AG Coating	
Interface	Register	Serial Interface
	Image Data	24bits Digital-RGB（8bits/color）
Outline Dimension	79.0(W) × 65.0(H) × 3.2Max*（D）mm *Without FPC and Component Area	
Weight	29.5gMax	

3. How to use

3.1 Interface Connection

(1) LCD Module side

LCD Module side is matched with 44-conductor FPC / FFC to ZIF connector.

<Connector Specification>

Produced by	Kyocera Elco
Type Number	046240040023846+
Pin Numbers	40
Pitch	0.5 mm Pitch
Cable Connection	Zero insertion force (ZIF) Right angle
Contact Location	Bottom Contact
Height	2.00mm
Lock Type	One Touch Lock

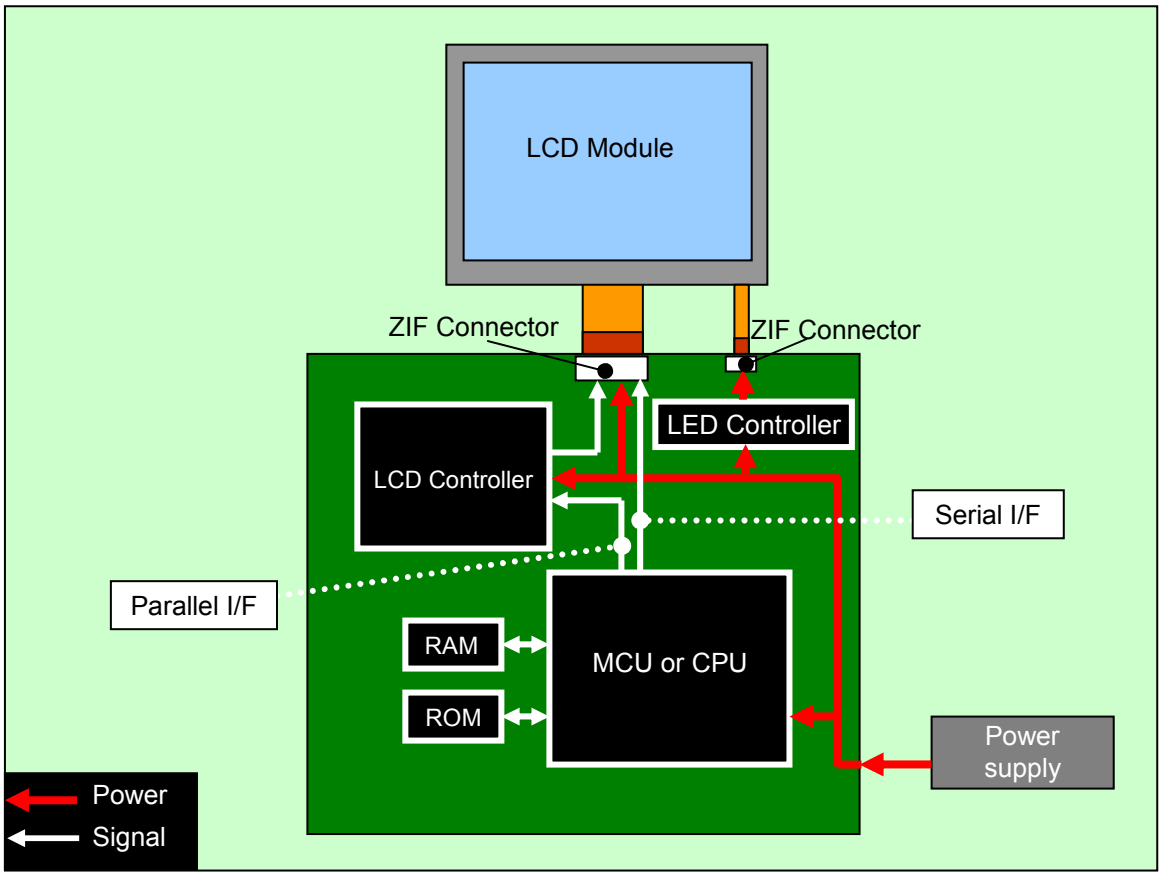
(2) Backlight side

Backlight side is matched with 3-conductor FPC / FFC to ZIF connector.

<Connector Specification>

Produced by	Kyocera Elco
Type Number	046298003000883
Pin Numbers	3
Pitch	0.5 mm Pitch
Cable Connection	Zero insertion force (ZIF) Right angle
Contact Location	Bottom Contact
Height	0.9mm
Lock Type	One Touch Lock

3.2 Brief of system circuit



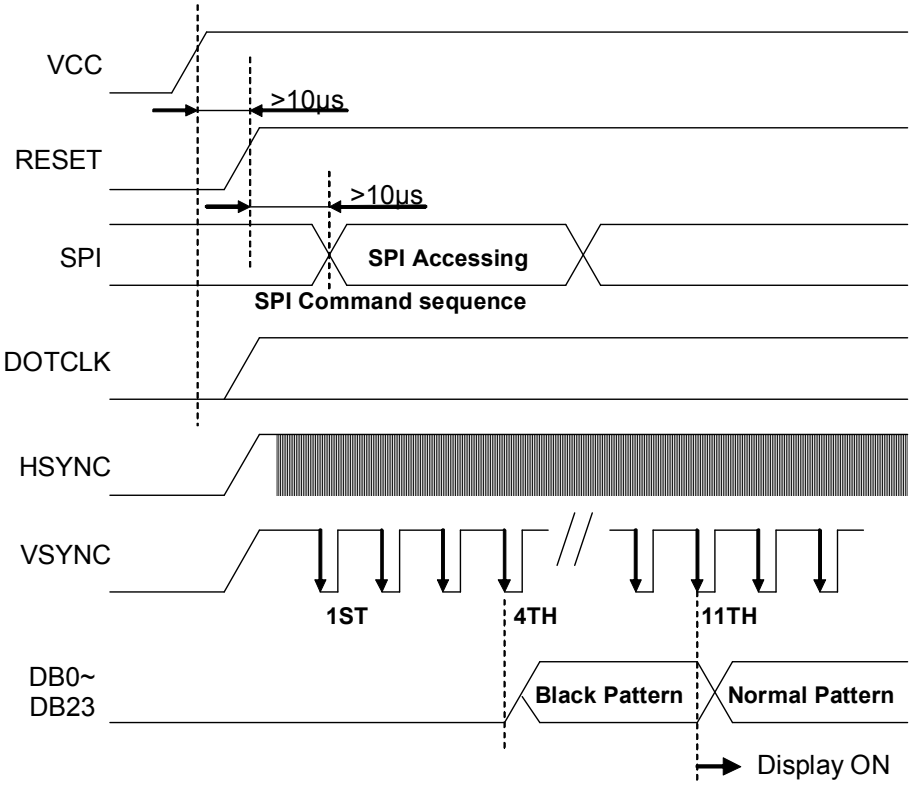
Exp. Customer's equipment circuit board

3.3 Driving the LCD Module

(1) Power On Sequence

We show the power on sequence for this LCD moduke.

※Please see the specification sheet for T-55264 for detail of timing value needed to operate the display.



VCC Power ON
↓
Wait 10µsec~
↓
Release RESET
↓
Input Control Signal
(DOTCLK/HSYNC/VSYNC)
↓
Execute SPI Command Setting
See the (2) Power On register setting
↓
Input Black data
↓
LCD Display ON after 11 frames

(2) Power On register setting

Example for register setting. (Recommended value)

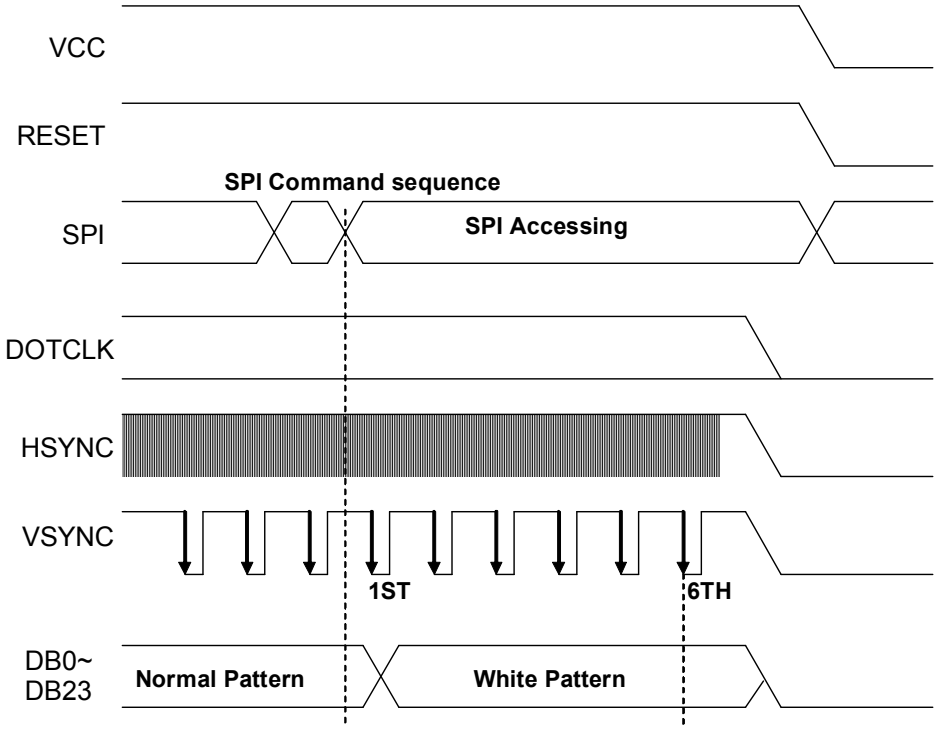
S : No need to change after power ON

A : Need to change or adjust after power ON

Driver output control	01h	6300h	S	
LCD driver AC control Line Inversion	02h	0200h	A	the grayscale level can be reversed.
Power control (1)	03h	6064h	S	**Step Up-cycle Fline*5 0110 VGH = (VCIX2 * 3) VGL = -(VCIX2 * 3) + VCI 0000 Step Up-cycle Fline*5 0110 OPamp power Small to Medium 0100**
Data and color filter control	04h	0447h	S	
Function control	05h	B0C4h	S	
Contrast/Brightness control	0Ah	3F08h	S	
Frame cycle control	0Bh	D400h	S	
Power control (2)	0Dh	423Dh	S	**VRC = 5.9 (VCIX2) 0100 VDD = 2.2 (If pin "REGVDD" is set to VDDIO) 0010 VLCD63 = Vref * 4.408 (Vref=1.25) 00111101**
Power control (3)	0Eh	3140h	S	**VCOMA = 1.0875 * VLCD63 1 0001 01**
Gate scan starting Position	0Fh	0000h	S	
Horizontal Porch	16h	9F80h	S	
Vertical Porch	17h	2212h	S	
Power control (4)	1Eh	00DBh	A	**Adjust the VCOM. nOTP = 1 VCOMH = 0.800 * VLCD63 101 1011**
γ Control1	30h	0000h	S	
γ Control2	31h	0607h	S	
γ Control3	32h	0006h	S	
γ Control4	33h	0307h	S	
γ Control5	34h	0107h	S	
γ Control6	35h	0001h	S	
γ Control7	36h	0707h	S	
γ Control8	37h	0703h	S	
γ Control9	3Ah	0C00h	S	
γ Control10	3Bh	0006h	S	

(3) Power off sequence

We show the example of Power off sequence.



Execute SPI Command Setting
↓
Input White Data
↓
LCD Display OFF after 6 frames
↓
Stop Control Signal
(DOTCLK/HSYNC/VSYNC)
↓
VCC Power OFF

(4) Power off register setting.

Example of register setting. (Recommended)

Setting Item	Index	Value
Power Control (1)	0003 h	0100 h

(5) Detail of register setting

Driver Output Control (R01h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	RL	REV	PINV	BGR	SM	TB	CPE	0	0	0	0	0	0	0	0

CPE :

CPE = 0 GATE Voltage、Source voltage 、VCOM Voltage are shut down

CPE = 1 GATE Voltage、Source voltage 、VCOM Voltage are enabled.

REV : Grayscale level reverse setting.

REV = 1 Displays all character and graphics display sections with same data.

REV = 0 Displays all character and graphics display sections with reversal.

PINV : POL信号の出力状態を設定

PINV = 0 POL output is same phase with internal VCOM signal. (Generally set POL = 1)

PINV = 1 POL output phase is reversed with VCOM signal.

BGR : Select the [R][G][B] alignment.

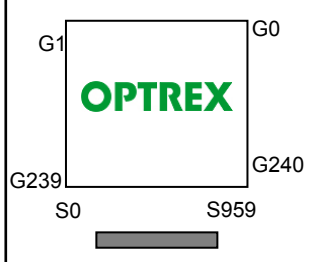
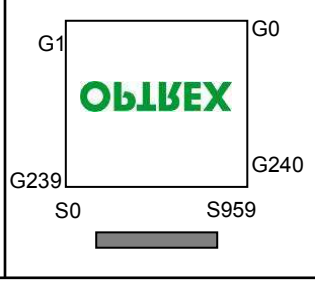
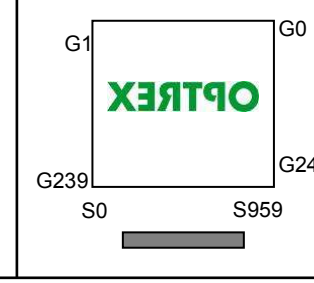
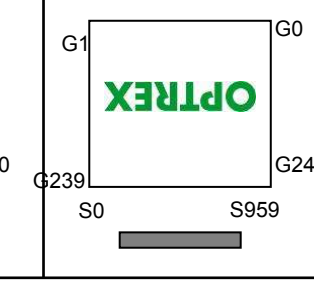
BGR = 0 [R][G][B] color is assigned from S0.（Generally set BGR = 0）

BGR = 1 [B][G][R] color is assigned from S0.

SM : Set SM = 0

TB :

RL :

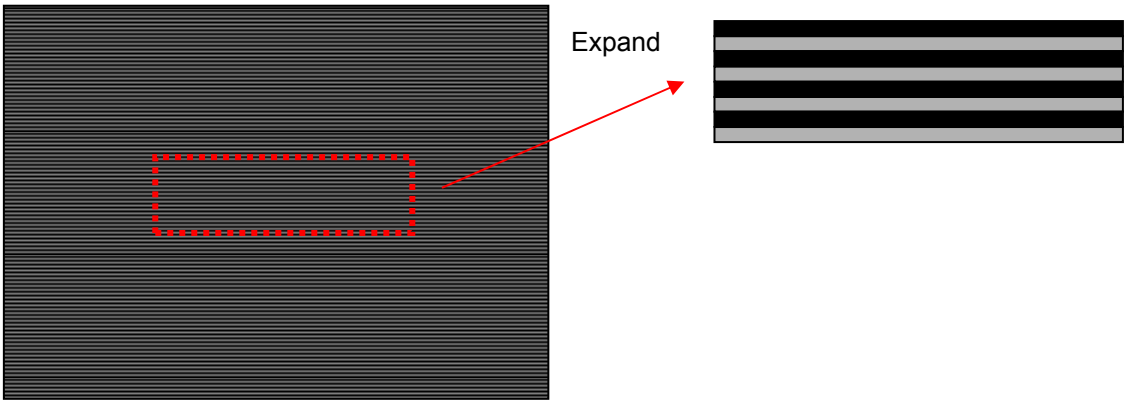
TB=1 RL=1	TB=0 RL=1	TB=1 RL=0	TB=0 RL=0
			

LCD-Driving-Waveform Control (R02h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	0	0	0	0	0	B/C	CPE	0	0	0	0	0	0	0	0

B/C : Select the LCD driving signal
B/C = 0, frame inversion
B/C = 1, Line inversion ⇒ Please set B/C = 1.

(Note) Note of using line inversion
Compared to frame inversion, we can improve the image quality LCD, when select the line inversion.
When display the 1line black and gray border pattern, display show the stronger flicker.
It is due to the line inversion is the driving method which is inverse each line.
So, we highly recommend not to use this image for background image.



Power control 1 (R03h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	DCT 3	DCT 2	DCT 1	DCT 0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0

DCT3-0 : Set the step-up cycle of the step-up circuit for 8-color mode.
*This LCD module cannot use 8 color mode, so ignore this register.
Please set DCT3-0 = 0110.

BT2-0、BTF : Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power supply voltage to be used. Generally set BTF,2-0=0000.

BTF	BT2	BT1	BT0	VGH output	VGL output
0	0	0	0	VCIX2J x 3	- (VCIX2J x 2) + VCI
0	0	0	1	VCIX2J x 3	- (VCIX2J x 2)
0	0	1	0	VCIX2J x 3	- (VCIX2J x 3)
0	0	1	1	VCIX2J x 2 + VCI	- (VCIX2J x 2) + VCI
0	1	0	0	VCIX2J x 2 + VCI	- (VCIX2J x 2)
0	1	0	1	VCIX2J x 2 + VCI	- (VCIX2J x 2) + VCI
0	1	1	0	VCIX2J x 2	- (VCIX2J x 2)
0	1	1	1	VCIX2J x 2	- (VCIX2J x 2) + VCI
1	x	x	X	VCIX2J x 3	- VCIX2J

DC3-0 : Set the step-up cycle of the step-up circuit for 262k-color mode.
※Color mode is always fixed as 262 - color mode in this module.
When the cycle is accelerated, the driving ability of the step-up circuit are increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption. Generally set DC3-0 = 0110.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

AP2−0 : Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no
display, such as when the system is in a sleep mode, set AP2-0 = “000” to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to Medium
0	1	1	Medium
1	0	0	Medium to Large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

Input Data and Color Filter Control (R04h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	0	0	0	0	PAL M	BLT 1	BLT 0	OEA 1	OEA 0	SEL 2	SEL 1	SEL 0	SW D2	SW D1	SW D0

SWD2-0 : Select the TFT alignment, Delta or Stripe.
This LCD module is Stripe alignment, so please set SWD2-0 = “111”
SEL2-0 : Define the input interface mode.
This LCD Module supports Parallel-RGB data format, so please set SEL2-0 = 000.
BLT1-0 : Set the initial power on black image insertion time.
00 : 10 Fields ⇒ Generally set BLT1-0 = 00
01 : 20 Fields
10 : 40 Fields
11 : 80 Fields
PALM : Set the input data line number in PAL mode
0 : 280 lines
1 : 288 Lines
OEA1-0 : Odd/Even field advanced function.
Generally set OEA1-0 = 00

OEA1	OEA0	
0	0	Display Start @ VBP delay for Odd field and @ ***VBP-1*** for Even field.
0	1	Display Start @ VBP delay for Odd field and @ ***VBP*** for Even field.
1	0	Display Start @ VBP delay for Odd field and @ ***VBP+1*** for Even field.
1	1	No use

Function Control (R05h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0

FB2-0 : Set PWM feedback level adjustment.
*In this LCD module, no function for PWM. So, please set FB2-0=000.
PWM : Set PWM feedback level adjustment. PWM=0 : PWM OFF PWM=1 : PWM ON
*In this LCD module, no function for PWM. So, please set PWM=0と設定してください。
DIT : Set the Dithering function. DIT=0 : Dithering OFF DIT=1 : Dithering ON
Use 24bits : DIT = 1
Use 18bits : DIT = 0
DEO : Set DE mode.
DEO = 0 : VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP [6:0] and the horizontal first valid data is defined by DE signal.
DEO=1, only DEN signal is needed in DE mode.

HSP : Set the polarity of HSYNC.HSP=0, Negative polarity HSYNC. HSP=1, Positive polarity HSYNC.
VSP : Set the polarity of HSYNC.VSP=0, Negative polarity VSYNC. VSP=1, Positive polarity VSYNC.
CKP : Set the direction of data latch of CLK.
CKP = 0, Data is latched in CLK falling edge.
CKP = 1, Data is latched in CLK rising edge.
DEP : Set the polarity of DEN. DEP=0, DEN Negative polarity active. DEP=1, DEN Negative polarity active.
LPF : Set the low pass filter in YUV mode.
*This LCD doesn't support the YUV interface, so please ignore this register.
GDIS : Set the discharge of VGL.
GDIS=0, VGL has no discharge path to VSS in sleep mode.
GDIS=1, VGL will discharge to VSS in sleep mode.
※When CPE=0, GDIS is fixed to 0, and you can't change it by SPI.
XDK : Set the pumping way of VCIX2。
XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2 = 3 x VCI)
XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2 = 2 x VCI)
GHN : Set the output of VGH.
GHN=0, All gate outputs are forced to VGH.
GHN=1, Gate driver is normal operation.

Contrast/Brightness Control (R0Ah)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON 4	CON 3	CON 2	CON 1	CON 0

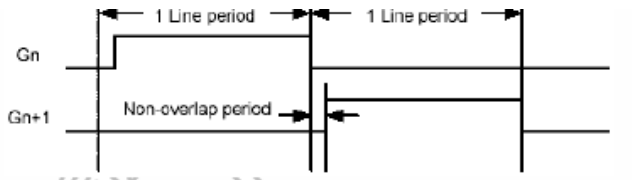
CON4-0 : Display Contrast level adjustment. (0.125/step) Adjust range from 00h (level = 0) to 1Fh (level = 3.875). Generally set CON4-0=1000.
BR6-0 : Display Brightness level adjustment. (2/step) Adjust range from 00h (level = -128) to 7Fh (level = +126). Generally set BR-6-0 = 3Fh

Frame Cycle Control Control (R0Bh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	NO1	NO0	SDT 1	SDT 0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0

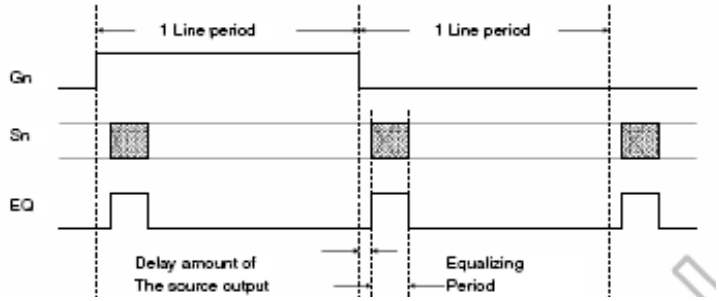
NO1-0 : Set amount of non-overlap of the gate output.
Set NO1-0 = 01

NO1	NO0	Non-overlap
0	0	1.5us
0	1	3us
1	0	4.5us
1	1	6us



STD1-0 : Set delay amount from the gate output signal falling edge to the source outputs.
Set STD1-0 = 00

STD1	STD0	Delay
0	0	1us
0	1	3us
1	0	5us
1	1	7us



EQ2-0 : Sets the equalizing period.
Set EQ2-0 = 000

EQ2	EQ1	EQ0	EQ Period
0	0	0	No EQ
0	0	1	3us
0	1	0	4us
0	1	1	5us
1	0	0	6us
1	0	1	7us
1	1	0	8us
1	1	1	9us

Power control 2 (R0Dh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	VRC 2	VRC 1	VRC 0	0	0	VDS 1	VDS 0	0	0	VRH 5	VRH 4	VRH 3	VRH 2	VRH 1	VRH 0

VRC2-0 : Set the VCIX2 charge pump voltage clamp
VRC [2:0]=000, 5.1V
VRC [2:0]=001, 5.3V
VRC [2:0]=010, 5.5V
VRC [2:0]=011, 5.7V
VRC [2:0]=100, 5.9V
VRC [2:0]=101, reserved
VRC [2:0]=110, reserved
VRC [2:0]=111, reserved
VDS1:0 : Set the VDD regulator voltage if pin “REGVDD” is set to VDDIO.
VDS [1:0]=00, 1.8V
VDS [1:0]=01, 2.0V
VDS [1:0]=10, 2.2V
VDS [1:0]=11, 2.5V
VRH5-0 : Set amplitude magnification of VLCD63.
Vref = 1.25V

VRH 5	VRH 4	VRH 3	VRH 2	VRH 1	VRH 0	VLCD63 Voltage
0	0	0	0	0	0	Vref x 2.456
0	0	0	0	0	1	Vref x 2.488
0	0	0	0	1	0	Vref x 2.520
0	0	0	0	1	1	Vref x 2.552
0	0	0	1	0	0	Vref x 2.584
0	0	0	1	0	1	Vref x 2.616
0	0	0	1	1	0	Vref x 2.648
0	0	0	1	1	1	Vref x 2.680
0	0	1	0	0	0	Vref x 2.712
0	0	1	0	0	1	Vref x 2.744
0	0	1	0	1	0	Vref x 2.776
0	0	1	0	1	1	Vref x 2.808
0	0	1	1	0	0	Vref x 2.840
0	0	1	1	0	1	Vref x 2.872
0	0	1	1	1	0	Vref x 2.904
0	0	1	1	1	1	Vref x 2.936
0	1	0	0	0	0	Vref x 2.968
0	1	0	0	0	1	Vref x 3.000
0	1	0	0	1	0	Vref x 3.032
0	1	0	0	1	1	Vref x 3.064
0	1	0	1	0	0	Vref x 3.096
0	1	0	1	0	1	Vref x 3.128
0	1	0	1	1	0	Vref x 3.160
0	1	0	1	1	1	Vref x 3.192
0	1	1	0	0	0	Vref x 3.224
0	1	1	0	0	1	Vref x 3.256
0	1	1	0	1	0	Vref x 3.288
0	1	1	0	1	1	Vref x 3.320
0	1	1	1	0	0	Vref x 3.352
0	1	1	1	0	1	Vref x 3.384
0	1	1	1	1	0	Vref x 3.416
0	1	1	1	1	1	Vref x 3.448

VRH 5	VRH 4	VRH 3	VRH 2	VRH 1	VRH 0	VLCD63 Voltage
1	0	0	0	0	0	Vref x 3.480
1	0	0	0	0	1	Vref x 3.512
1	0	0	0	1	0	Vref x 3.544
1	0	0	0	1	1	Vref x 3.576
1	0	0	1	0	0	Vref x 3.608
1	0	0	1	0	1	Vref x 3.640
1	0	0	1	1	0	Vref x 3.672
1	0	0	1	1	1	Vref x 3.704
1	0	1	0	0	0	Vref x 3.736
1	0	1	0	0	1	Vref x 3.768
1	0	1	0	1	0	Vref x 3.800
1	0	1	0	1	1	Vref x 3.832
1	0	1	1	0	0	Vref x 3.864
1	0	1	1	0	1	Vref x 3.896
1	0	1	1	1	0	Vref x 3.928
1	0	1	1	1	1	Vref x 3.960
1	1	0	0	0	0	Vref x 3.992
1	1	0	0	0	1	Vref x 4.024
1	1	0	0	1	0	Vref x 4.056
1	1	0	0	1	1	Vref x 4.088
1	1	0	1	0	0	Vref x 4.120
1	1	0	1	0	1	Vref x 4.152
1	1	0	1	1	0	Vref x 4.184
1	1	0	1	1	1	Vref x 4.216
1	1	1	0	0	0	Vref x 4.248
1	1	1	0	0	1	Vref x 4.280
1	1	1	0	1	0	Vref x 4.312
1	1	1	0	1	1	Vref x 4.344
1	1	1	1	0	0	Vref x 4.376
	1	1	1	0	1	Vref x 4.408
	1	1	1	1	0	Vref x 4.440
	1	1	1	1	1	Vref x 4.472

Power control 3 (R0Eh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	0	1	VDV 6	VDV 5	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	0	0	0

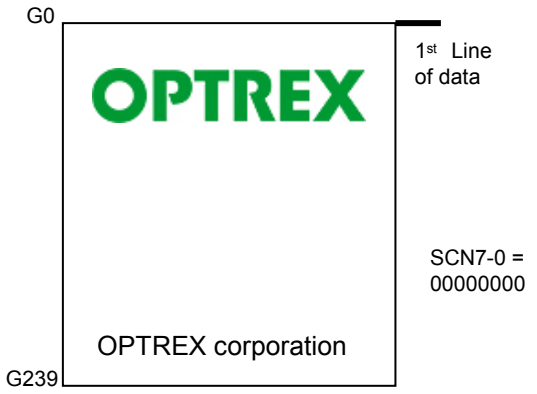
VDV6-0 : Set the alternating amplitudes of VCOM at the VCOM alternating drive.

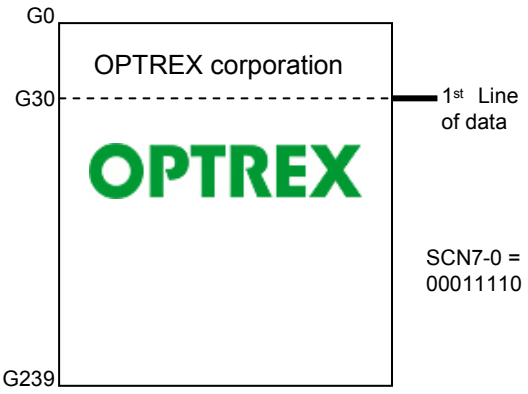
VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	0	0	VLCD63 x 0.6000
0	0	0	0	0	0	1	VLCD63 x 0.6075
0	0	0	0	0	1	0	VLCD63 x 0.6150
0	0	0	0	0	1	1	VLCD63 x 0.6225
0	0	0	0	1	0	0	VLCD63 x 0.6300
....							Step = 0.0075
0	1	1	1	0	1	0	VLCD63 x 1.0350
0	1	1	1	0	1	1	VLCD63 x 1.0425
0	1	1	1	1	*	*	Reference from external voltage (VCOMR)
1	0	0	0	0	0	0	VLCD63 x 1.0500
1	0	0	0	0	0	1	VLCD63 x 1.0575
....							Step = 0.0075
1	0	1	1	0	1	0	VLCD63 x 1.2450
1	0	1	1	0	1	1	VLCD63 x 1.2525
1	0	1	1	1	*	*	Reserved
1	0	1	*	*	*	*	Reserved

Gate Scan Position (R0Fh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	0	0	0	0	0	0	0	SCN 7	SCN 6	SCN 5	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0

SCN8-0 : Set the scanning starting position of the gate driver.





Horizontal Porch (R16h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	XLI M8	XLI M7	XLI M6	XLI M5	XLI M4	XLI M3	XLI M2	XLI M1	XLI M0	0	0	0	0	0	0	0

XLIM8-0 : Set the scanning starting position of the gate driver.

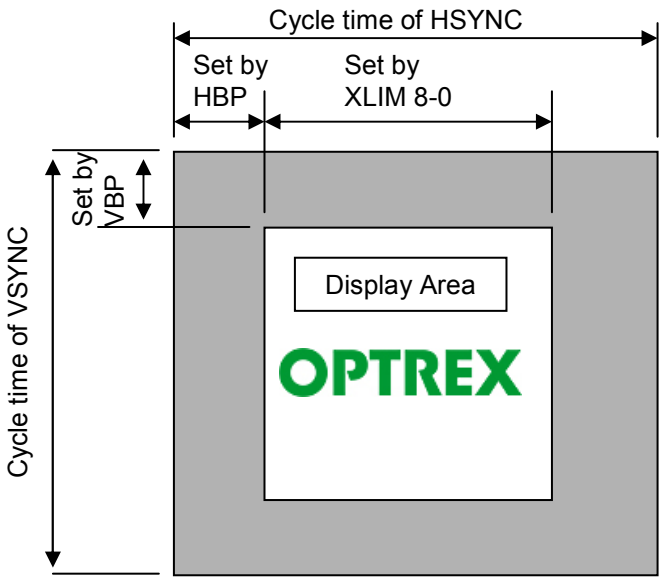
XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				....					STEP = 1
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	0	1	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

Vertical Porch (R17h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	STH 1	STH 0	HBP 6	HBP 5	HBP 4	HBP 3	HBP 2	HBP 1	HBP 0	VBP 6	VBP 5	VBP 4	VBP 3	VBP 2	VBP 1	VBP 0

HBP6-0 : Set the number of valid pixel per line.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of Clock Cycle
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	Can't set
0	0	0	0	0	1	1	Can't set
0	0	0	0	1	0	0	Can't set
0	0	0	0	1	0	1	Can't set
0	0	0	0	1	1	0	Can't set
0	0	0	0	1	1	1	Can't set
0	0	0	1	0	0	0	Can't set
1	0	0	0	0	0	1	9
1	0	0	0	0	1	0	10
....							Step – 1
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127



STH1-0 : Adjust the first valid data by dot clock.

* This setting is not valid in parallel RGB input interface. Please ignore this setting.

STH = 00: + 0 dot clock
STH = 01: + 1 dot clock
STH = 10: + 2 dot clock
STH = 11: + 3 dot clock

VBP6-0 : Set the delay period from falling edge of VSYNC to first valid line.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of Clock Cycle
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
....							Step – 1
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Power control 4 (R1Eh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

nOTP :

nOTP = “0” VCOMH voltage equals to programmed OTP value.

nOTP = “1” Setting of VCM6-0 becomes valid and voltage of VCOMH can be adjusted.

VCM6−0 : Set the VCOMH voltage if nOTP = “1”.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VLCD63 x 0.360
0	0	0	0	0	0	1	VLCD63 x 0.365
0	0	0	0	0	1	0	VLCD63 x 0.370
0	0	0	0	0	1	1	VLCD63 x 0.375
0	0	0	0	1	0	0	VLCD63 x 0.380
....							Step = 0.005
1	1	1	1	1	1	0	VLCD63 x 0.990
1	1	1	1	1	1	1	VLCD63 x 0.995

（Note）About the adjustment of VCOMH

VCOM is not adjusted to optimum value in this model. Therefore, it is necessary to adjust the VCOMH value. To adjust the VCOMH, display the gray and black border line. And please set the value which minimize the flicker.

Gamma control 1 (R30h to R37)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
W	1	0	0	0	0	0	FRP 12	FRP 11	FRP 10	0	0	0	0	0	FRP 02	FRP 01	FRP 00
W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00

PKP52–00 : Gamma micro adjustment registers for the positive polarity output.
PRP12-00 : Gradient adjustment registers for the positive polarity output.
PKN52-00 : Gamma micro adjustment registers for the negative polarity output.
PRN12-00 : Gradient adjustment registers for the negative polarity output.

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

VRP14–00 : Adjustment registers for amplification adjustment of the positive polarity output.
VRN14–00 : Adjustment registers for the amplification adjustment of the negative polarity output.

3.4 Example of driving the LCD Controller

You can use LCD controller for Digital RGB Interface.
Part Name :S1D13743 (Seiko Epson)
This manufacturers are presented for information only.
Optrex has not tested the performance and reliability of their products and makes no warranty to their fitness for use.
(2) Connection
Show the wiring between this LCD module and the LCD controller.

(Case1 18bits)

This Module Pin No.	Pin No. S1D15743	Symbol Name (S1D side)
1	—	RL
2	—	TB
3	8	DOTCLOCK (PCLK)
4	5	VSYNC (VS)
5	4	HSYNC (HS)
6	3	ENABLE (DE)
7	60	DB23(VD21)
8	55	DB22(VD20)
9	50	DB21(VD19)
10	45	DB20(VD18)
11	40	DB19(VD17)
12	20	DB18(VD16)
13	60	DB17(VD21)
14	55	DB16(VD20)
15	2など	GND
16	61	DB15(VD13)
17	56	DB14(VD12)
18	51	DB13(VD11)
19	48	DB12(VD10)
20	44	DB11(VD9)

This Module Pin No.	Pin No. S1D15743	Symbol Name (S1D side)
21	38	DB10(VD8)
22	61	DB9(VD13)
23	56	DB8(VD12)
24	2など	GND
25	62	DB7(DB5)
26	57	DB6(DB4)
27	54	DB5(DB3)
28	49	DB4(DB2)
29	43	DB3(DB1)
30	39	DB2(DB0)
31	62	DB1(DB5)
32	57	DB0(DB4)
33	—	SDI
34	—	SCL
35	—	CS
36	—	RESET
37	—	SDO
38	2など	GND
39	1など	VCC(PIOVDD)
40	1など	VCC(PIOVDD)

（Case2 24bits）

This Module Pin No.	Pin No. S1D15743	Symbol Name (S1D side)
1	—	RL
2	—	TB
3	8	DOTCLOCK (PCLK)
4	5	VSYNC (VS)
5	4	HSYNC (HS)
6	3	ENABLE (DE)
7	12	DB23(VD23)
8	13	DB22(VD22)
9	60	DB21(VD21)
10	55	DB20(VD20)
11	50	DB19(VD19)
12	45	DB18(VD18)
13	40	DB17(VD17)
14	20	DB16(VD16)
15	2など	GND
16	14	DB15(VD15)
17	15	DB14(VD14)
18	61	DB13(VD13)
19	56	DB12(VD12)
20	51	DB11(VD11)

This Module Pin No.	Pin No. S1D15743	Symbol Name (S1D side)
21	48	DB10(VD10)
22	44	DB9(VD9)
23	38	DB8(VD8)
24	2など	GND
25	21	DB7(DB7)
26	63	DB6(DB6)
27	62	DB5(DB5)
28	57	DB4(DB4)
29	54	DB3(DB3)
30	49	DB2(DB2)
31	43	DB1(DB1)
32	39	DB0(DB0)
33	—	SDI
34	—	SCL
35	—	CS
36	—	RESET
37	—	SDO
38	2など	GND
39	1など	VCC(PIOVDD)
40	1など	VCC(PIOVDD)

5.4 C Code

The following example scripts

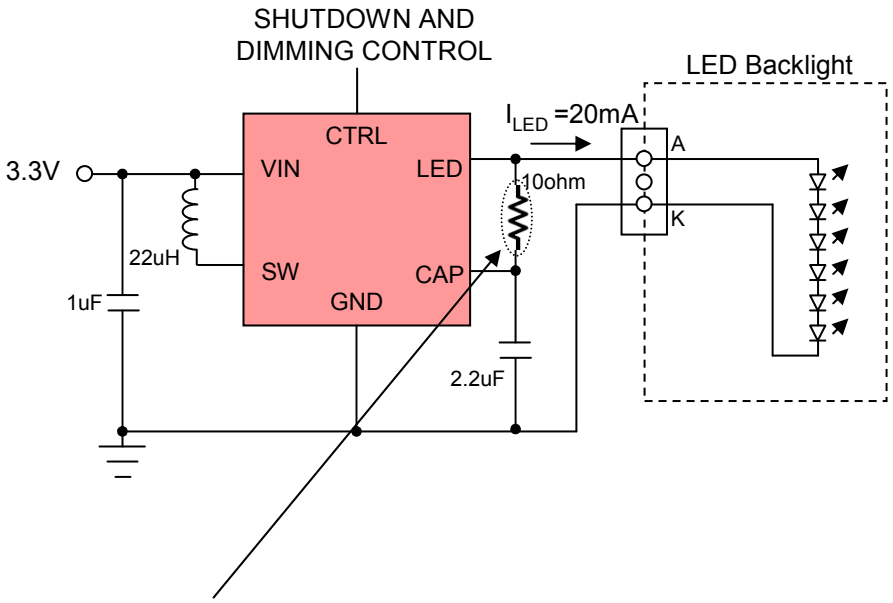
```
//-------------------------------------------------
// T55343(3.5inch:320x240dots)
//-------------------------------------------------
//「PowerON_Sequence」Power on setting
//「PowerOFF_Sequence」Power off setting
//「Display_output」  Image display setting
//Please use the header file for each development environment.

//*********************************************************
void Transfer_S1D13743(short reg ,short data)
{
        //---------------------------------------
        // index register write(intel80 16bit)
        clear_bit( IO_DC );                             //DC Low        Pararel_16bitout( reg );
        //---------------------------------------
        // instruction write(intel80 16bit)
        set_bit( IO_DC );                               //DC High       Pararel_16bitout( data );
}


//*********************************************************
void Transfer_HX8238(short reg ,short data)
{
        //---------------------------------------
        // index register write(SPI 24bit)
        clear_bit( IO_CSB );                            //CSB Low       SPI_8bitout( 0x70 );
                                //DeviceID,RS=0,RW=0
        SPI_8bitout( HIBYTE(reg) );
        SPI_8bitout( LOBYTE(reg) );
        set_bit( IO_CSB );                                              //CSB High
        //---------------------------------------
        // instruction write(SPI 24bit)
        clear_bit( IO_CSB );                            //CSB Low       SPI_8bitout( 0x72 );
                                //DeviceID,RS=1,RW=0
        SPI_8bitout( HIBYTE(data) );
        SPI_8bitout( LOBYTE(data) );
        set_bit( IO_CSB );                                              //CSB High
}
```

```
//*********************************************************
// The reference setting of Power On
//          320x240dots 18-bit TFT panel
//   CoreVdd = PLLVdd =1.50V input
//   IOVdd   = PIOVdd =3.30V input
//          CLKI    =  4.096MHz
//          SYSCLK  = 49.152MHz
//*********************************************************
void PowerON_Sequence(void)
{
        clear_bit( IO_RES );                                    //Reset Low       delay_ms(1);
                                                                //1ms wait
        set_bit( IO_RES );                                                      //Reset High
        delay_ms(10);                                                                   //10ms wait

        //=====================================================
        // S1D13743 intialize
        //=====================================================
        Transfer_S1D13743(0x56 ,0x02);//REG[56h] enter sleep mode
        //--------- CLK configuraion ---------
        Transfer_S1D13743(0x04 ,0x03);//REG[04h] PLL M-divider
                                      //PLLin=CLKI/4=1.024MHz
        Transfer_S1D13743(0x06 ,0xf8); //REG[06h] PLL setting 0
        Transfer_S1D13743(0x08 ,0x80);//REG[08h] PLL setting 1
        Transfer_S1D13743(0x0a ,0x28);//REG[0Ah] PLL setting 2
        Transfer_S1D13743(0x0c ,0x00);//REG[0Ch] PLL setting 3
        Transfer_S1D13743(0x0e ,0x2f); //REG[0Eh] PLL setting 4
                                      //LL=48 PLLCLK=49.152MHz
        Transfer_S1D13743(0x12 ,0x31);//REG[12h] Clock source select
                                      //PCLK=7.022MHz SYSCLK=49.152MHz
        //--------- Panel configuraion ---------
        //FLM = 7.022MHz/(320+88)/(240+22) = 65.69Hz
        //1clk(R6,G6,B6)=18bit
        Transfer_S1D13743(0x14 ,0x00);//REG[14h] Panel Type
                                      //0b:18bit /1b:24bit
        Transfer_S1D13743(0x16 ,0x28);//REG[16h] Horizontal display width
                                      //HDP = 320
        Transfer_S1D13743(0x18 ,0x58);//REG[18h] Horizontal non- display period
                                      //HNDP = 88
        Transfer_S1D13743(0x1a ,0xf0); //REG[1Ah] Vertical display height 0
        Transfer_S1D13743(0x1c ,0x00);//REG[1Ch] Vertical display height 1
                                      //VDP = 240
        Transfer_S1D13743(0x1e ,0x16);//REG[1Eh] Vertical non-display period
                                      //VNDP = 22
        Transfer_S1D13743(0x20 ,0x10);//REG[20h] HS pulse width
                                      //HSW = 16 pixels
        Transfer_S1D13743(0x22 ,0x20);//REG[22h] HS pulse start position
                                      //HPS = 32 pixels
        Transfer_S1D13743(0x24 ,0x02);//REG[24h] VS pulse width
                                      //VSW = 2 lines
        Transfer_S1D13743(0x26 ,0x04);//REG[26h] VS pulse start position
                                      //VPS = 4 lines
        Transfer_S1D13743(0x28 ,0x80);//REG[28h] PCLK polarity
                                      //80h:
                Transfer_S1D13743(0x2a ,0x02);          //REG[2Ah] Input mode
                                                        //RGB 6:6:6
        //--------- GPIO configuraion ---------
        //GPIO0=RL , GPIO1=TB
        Transfer_S1D13743(0x5a ,0x03);//REG[5Ah] GPIO configuration
                                      //b1-0 output
        Transfer_S1D13743(0x5c ,0x03);//REG[5Ch] GPIO port
                                      //TB=1 , RL=1
        Transfer_S1D13743(0x56 ,0x00);//REG[56h] disable sleep mode
        delay_ms(10);                                   //10ms wait
```

```
        //=====================================================
        // HX8238 intialize
        //=====================================================
        Transfer_HX8238(0x1e ,0x00d0);//REG[1Eh] power control 4

                                      //nOTP=1,VCM=1010000b
        Transfer_HX8238(0x05 ,0xbcc4);//REG[05h] function control
                                      //DEP=1
}


//*********************************************************
// The reference setting of Power Off
//*********************************************************
void PowerOFF_Sequence(void)
{
        Transfer_S1D13743(0x56 ,0x02);//REG[56h] enter sleep mode
        delay_ms(100);                                  //100ms wait
        clear_bit( IO_RES );                            //Reset Low}


//*********************************************************
// Write the image data to the Memory Data Port
//*********************************************************
void Display_output(short xdot ,short ydot)
{
        short       x,y;

        //-------- Window Aria set ----------
        Transfer_S1D13743(0x38 ,0x00);                  //REG[38h] Window X Start Position0
        Transfer_S1D13743(0x3a ,0x00);                  //REG[3Ah] Window X Start Position1
        Transfer_S1D13743(0x3c ,0x00);                  //REG[3Ch] Window Y Start Position0
        Transfer_S1D13743(0x3e ,0x00);                  //REG[3Eh] Window Y Start Position1

        Transfer_S1D13743(0x40 ,LOBYTE(xdot-1));        //REG[40h] Window X End Position0
        Transfer_S1D13743(0x42 ,HIBYTE(xdot-1));        //REG[42h] Window X End Position1
        Transfer_S1D13743(0x44 ,LOBYTE(ydot-1));        //REG[44h] Window Y End Position0
        Transfer_S1D13743(0x46 ,HIBYTE(ydot-1));        //REG[46h] Window Y End Position1

        clear_bit( IO_DC );                                             //DC Low
                Pararel_16bitout( 0x48 );                               //REG[48h]
        set_bit( IO_DC );                                               //DC High
        //-------- bit map data out ----------
        // 1dot=18bpp=RRRRRRxx GGGGGGxx BBBBBBxx  // 1dot=24bpp=RRRRRRRR GGGGGGGG BBBBBBBB          for(y=0 ;
        y<ydot ; y++) {
                for(x=0 ; x<xdot ; x+=2) {
                                Pararel_16bitout( (  Reg(x  ,y)<<8)|(Green(x  ,y));
                                Pararel_16bitout( ( Blue(x  ,y)<<8)|(  Red(x+1,y));
                                Pararel_16bitout( (Green(x+1,y)<<8)|( Blue(x+1,y));
                }
        }
}
```

3.5 Example of driving the LED Controller

You can use LED controller for Backlight driving.
Part Name :LT3591 （Linear Technology）
This manufacturers are presented for information only.
Optrex has not tested the performance and reliability of their products and makes no warranty to their fitness for use.



<R_{SENSE}>

The LED current can be programmed by as follow.

I_{LED} = 200mV / R_{SENSE}