



MOTOROLA
Semiconductors

2N6576
2N6577
2N6578

NPN SILICON POWER DARLINGTON TRANSISTORS

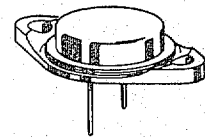
General-purpose EpiBase power darlington transistors, suitable for linear and switching applications.

- Replacement for 2N3055 and Driver
- High Gain Darlington Performance
- Built-In Diode Protection for Reverse Polarity Protection
- Can Be Driven from Low-Level Logic
- Popular Voltage Range
- Operating Range — -65 to +200°C

15 AMPERE
POWER TRANSISTORS

NPN SILICON
DARLINGTON

60, 90, 120 VOLTS
120 WATTS



***MAXIMUM RATINGS**

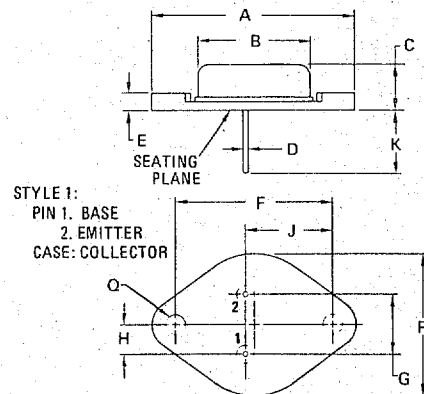
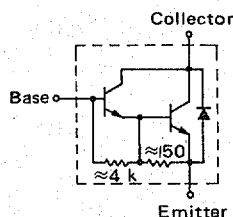
Rating	Symbol	2N6576	2N6577	2N6578	Unit
Collector-Emitter Voltage	$V_{CE(sus)}$	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current — Continuous	I_C	← 15 →			Adc
— Peak		← 30 →			
Base Current — Continuous	I_B	← 0.25 →			Adc
— Peak		← 0.50 →			
Emitter Current — Continuous	I_E	← 15.25 →			Adc
— Peak		← 30.5 →			
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above 25°C	P_D	← 120 →			Watts
		← 0.685 →			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.46	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for 10s.	T_L	265	°C

*Indicates JEDEC Registered Data

DARLINGTON SCHEMATIC



STYLE 1:
PIN 1: BASE
2: EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

CASE 11-03
TO-3

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^{\circ}\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1) ($I_C = 200 \text{ mAdc}$, $I_B = 0$)	$V_{CE(sus)}$	60 90 120	—	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated Value}$)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current ($V_{CER} = \text{Rated } V_{CE(sus)} \text{ Value}$, $R_{BE} = 10 \text{ k}\Omega$, $T_C = 150^{\circ}\text{C}$)	I_{CER}	—	5.0	mAdc
Collector Cutoff Current $V_{CEX} = \text{Rated } V_{CE(sus)} \text{ Value}$, $V_{BE(off)} = 1.5 \text{ Vdc}$	I_{CEV}	—	5.0	mAdc
Collector Cutoff Current ($V_{CB} = \text{Rated Value}$)	I_{CBO}	—	0.5	mAdc

ON CHARACTERISTICS

DC Current Gain ($I_C = 15 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 4.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 0.4 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	100 500 2000 200	— 5,000 20,000 —	—
Collector-Emitter Saturation Voltage ($I_C = 15 \text{ Adc}$, $I_B = 0.15 \text{ Adc}$) ($I_C = 10 \text{ Adc}$, $I_B = 0.1 \text{ Adc}$)	$V_{CE(sat)}$	— —	4.0 2.8	Vdc
Base-Emitter Saturation Voltage ($I_C = 15 \text{ Adc}$, $I_B = 0.15 \text{ Adc}$) ($I_C = 10 \text{ Adc}$, $I_B = 0.1 \text{ Adc}$)	$V_{BE(sat)}$	— —	4.5 3.5	Vdc
Collector-Emitter Diode Voltage Drop ($I_{EC} = 15 \text{ Adc}$)	V_F	—	4.5	Vdc

DYNAMIC CHARACTERISTICS

Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	$ h_{fe} $	10	200	—
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SWITCHING CHARACTERISTICS

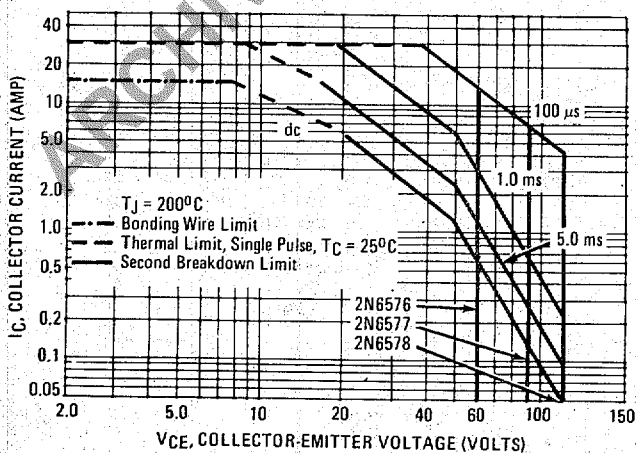
RESISTIVE LOAD (Figure 2)

Delay Time ($V_{CC} = 30 \text{ Vdc}$, $I_C = 10 \text{ Adc}$, $I_{B1} = 0.1 \text{ Adc}$, $t_p = 300 \mu\text{s}$, Duty Cycle $< 2.0\%$)	t_d	—	0.15	μs
Rise Time	t_r	—	1.0	μs
Storage Time ($V_{CC} = 30 \text{ Vdc}$, $I_C = 10 \text{ Adc}$, $I_{B1} = I_{B2} = 0.1 \text{ Adc}$, $t_p = 300 \mu\text{s}$, Duty Cycle $< 2.0\%$)	t_s	—	2.0	μs
Fall Time	t_f	—	7.0	μs

* Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

FIGURE 1 – RATED FORWARD BIASED SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^{\circ}\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%.

$T_J(pk)$ may be calculated from the data in Figure 7. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



FIGURE 2 — DC CURRENT GAIN

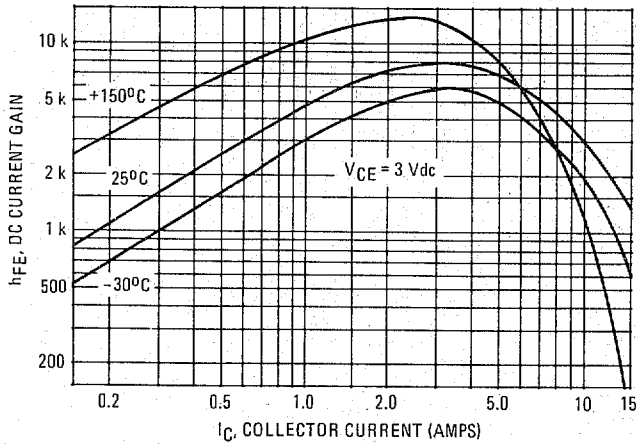


FIGURE 3 — COLLECTOR-SATURATION REGION

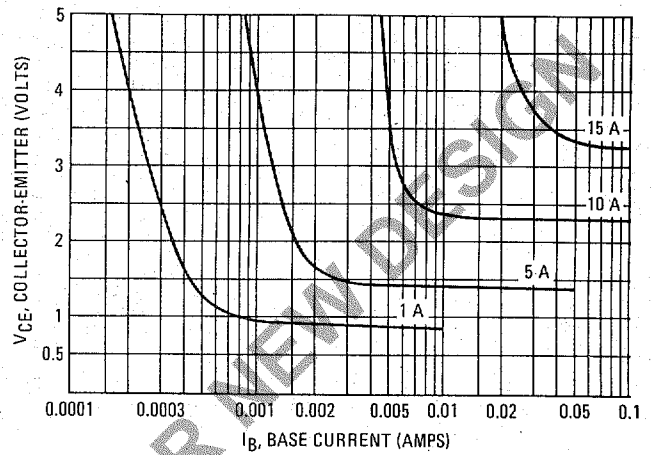


FIGURE 4 — COLLECTOR SATURATION VOLTAGE

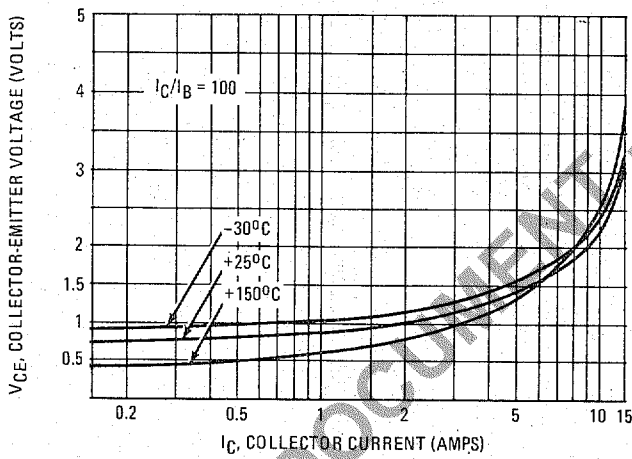


FIGURE 5 — BASE-EMITTER VOLTAGE

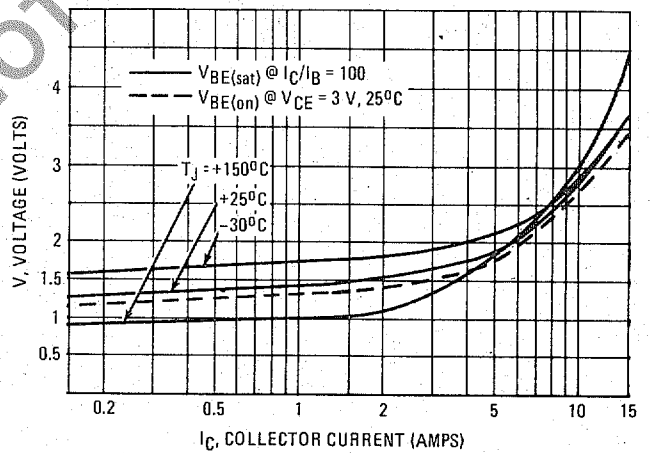


FIGURE 6 — THERMAL RESPONSE

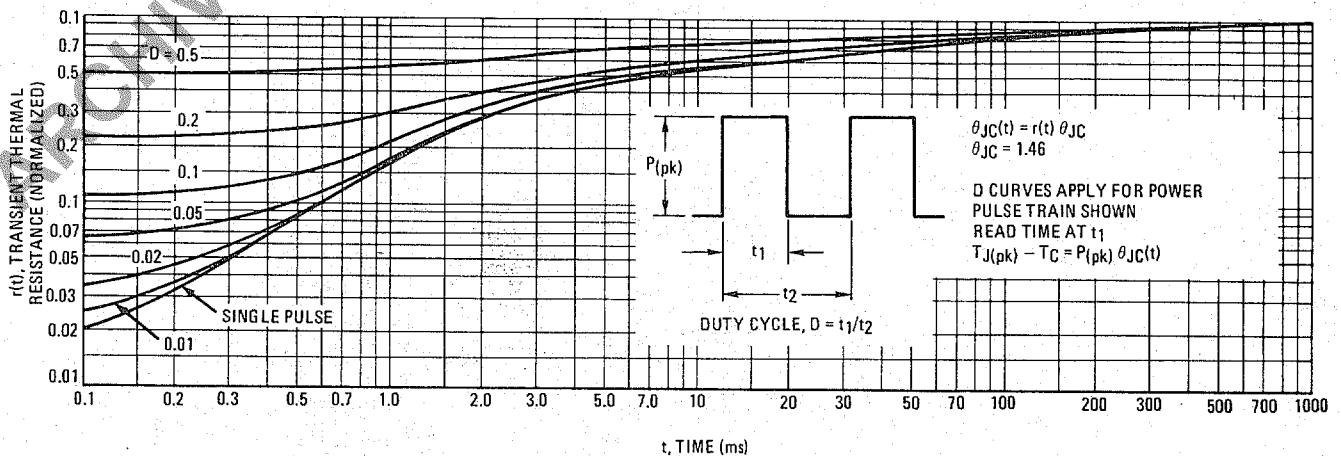
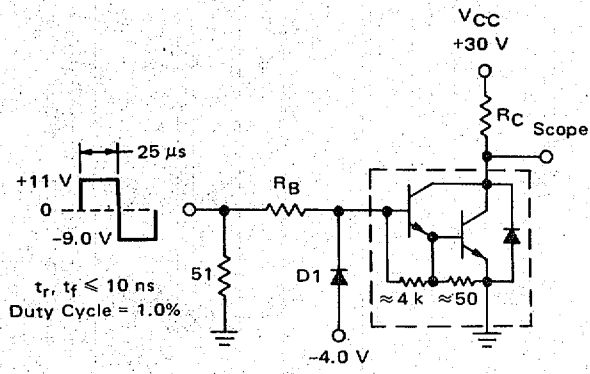


FIGURE 7 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C Varied to Obtain Desired Current Levels
 D1 Must be Fast Recovery Type, eg:

FIGURE 8 – SWITCHING TIMES

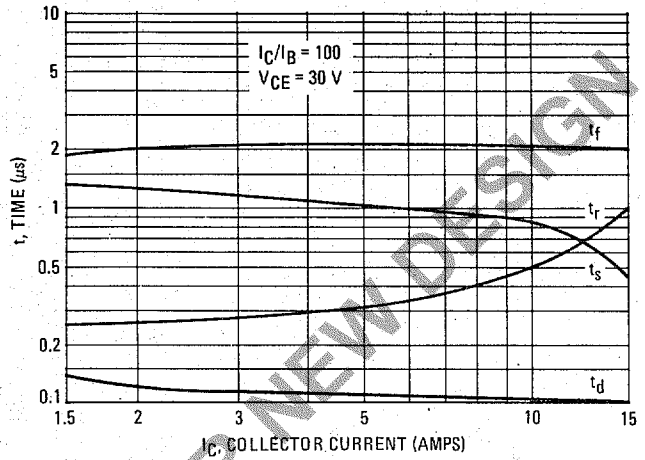


FIGURE 9 – COLLECTOR CUT-OFF REGION

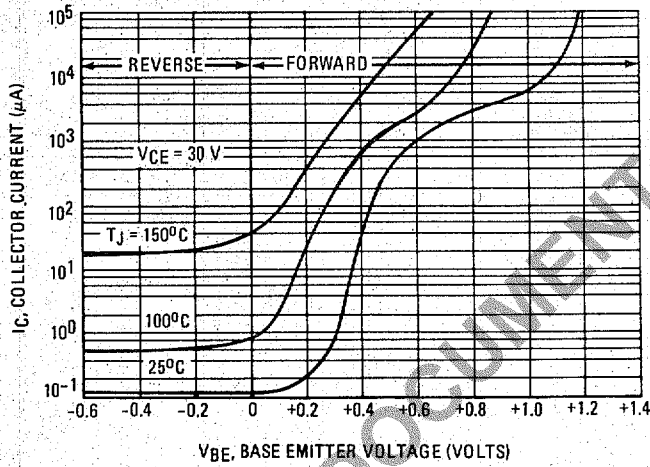


FIGURE 10 – CAPACITANCE

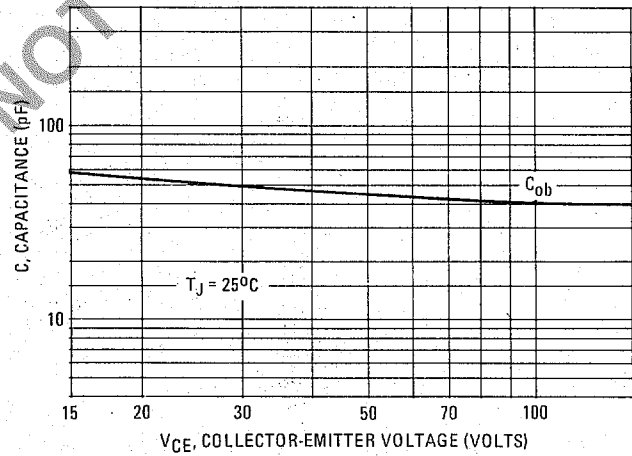


FIGURE 11 – COLLECTOR-EMITTER VOLTAGE

