MOTOROLA

Quad Parallel Register With Enable

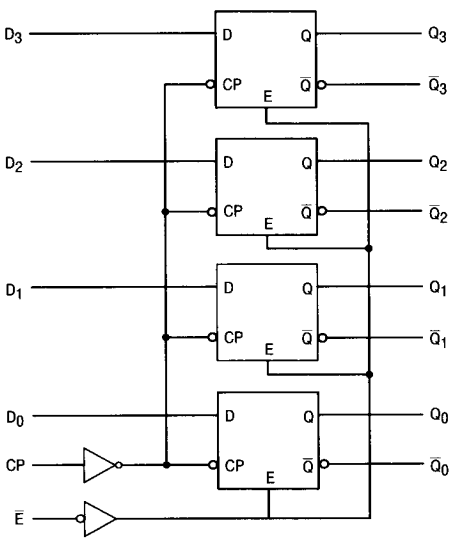
ELECTRICALLY TESTED PER:
MIL-M-38510/34109

The 54F379 is a 4-Bit register with a buffered common Enable. This device is similar to the 54F175 but features common Enable rather than common Master Reset.

The 'F379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When $\overline{E}$ is HIGH, the register will retain the preset data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed. This circuit is designed to prevent false clocking by transitions on the $\overline{E}$ input.

- Edge-Triggered D Type Inputs
- Buffered Positive Edge-Triggered Clock
- Buffered Common Enable Input
- True and Complement Outputs

LOGIC DIAGRAM



Please note that this logic diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Military 54F379

AVAILABLE AS:

1) JAN: JM38510/34109BXA
2) SMD: N/A
3) 883C: 54F379/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{E}$	1	1	2	GND
Q_0	2	2	3	OPEN
$\overline{Q}_0$	3	3	4	OPEN
D_0	4	4	5	V_{CC}
D_1	5	5	7	V_{CC}
$\overline{Q}_1$	6	6	8	OPEN
Q_1	7	7	9	OPEN
GND	8	8	10	GND
CP	9	9	12	V_{CC}
Q_2	10	10	13	OPEN
$\overline{Q}_2$	11	11	14	OPEN
D_2	12	12	15	V_{CC}
D_3	13	13	17	V_{CC}
$\overline{Q}_3$	14	14	18	OPEN
Q_3	15	15	19	OPEN
V_{CC}	16	16	20	V_{CC}

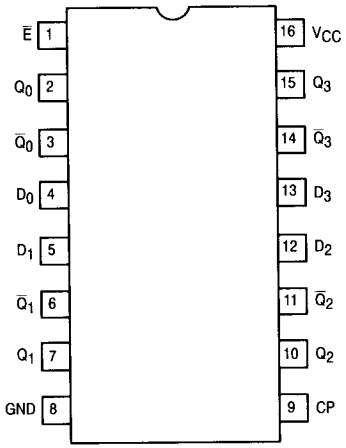
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

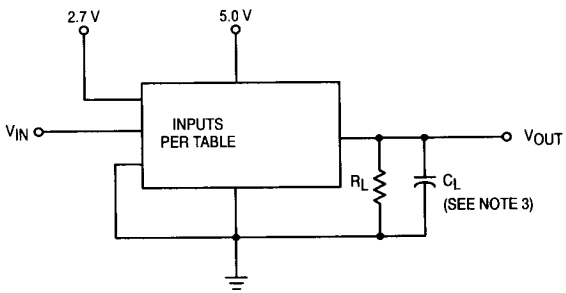
Inputs			Outputs	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⎍	X	NC	NC
L	⎍	H	H	L
L	⎍	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
⎍ = Transition from Low to High Level
NC = No Change

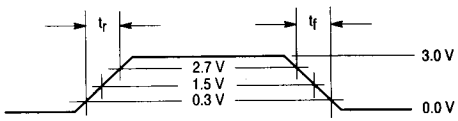
CONNECTION DIAGRAM



AC TEST CIRCUIT



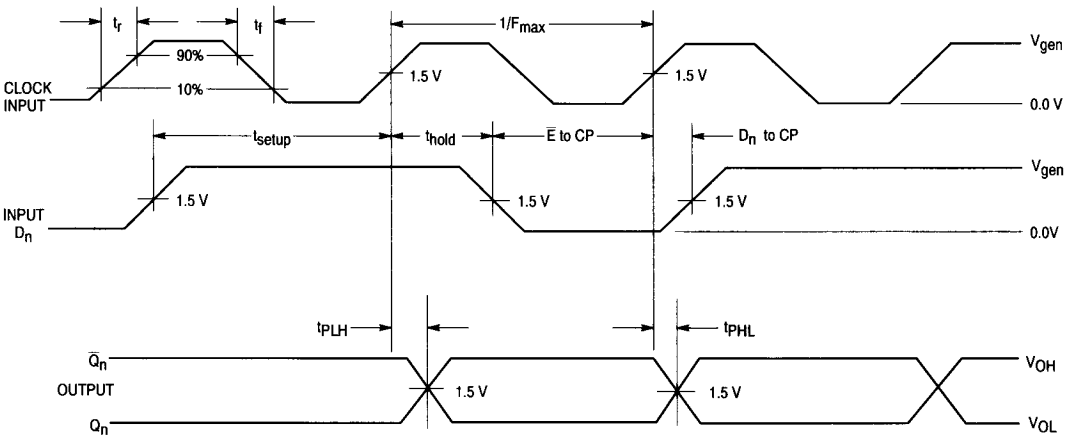
WAVEFORM



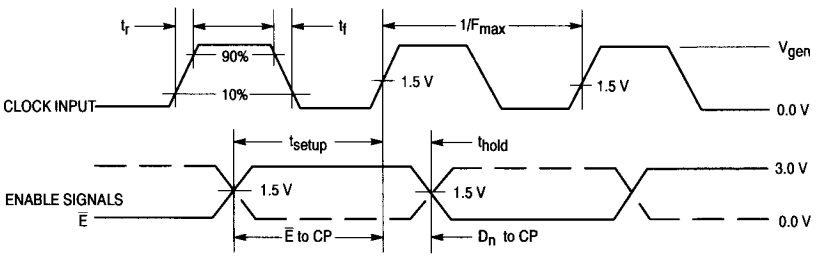
NOTES:

1. V_{IN} = Input pulse and has the following characteristics: PRR ≤ 1.0 MHz, $t_r = t_f \leq 2.5$ ns.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. R_L = 499 Ω ± 1.0%.
5. Voltage measurements are to be made with respect to network ground terminal.

WAVEFORMS



NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3.0 ± 0.2 V, $t_r = t_f \leq$ 2.5 ns and PRR ≤ 1.0 MHz.
2. D input has the following characteristics: V_{gen} = 3.0 ± 0.2 V, t_{setup} = 3.0 ns minimum, t_{hold} = 1.0 ns minimum, $\overline{E}$ to CP = t_{setup} (D_n > CLK), D_n to CP = t_{hold} (D_n > CLK).
3. For f_{MAX} testing, see table 1.
4. t_{PLH} and t_{PHL} are shown for Q_n only, (CLK > Q_n, Q_n). The $\overline{Q}_n$ output will have these reversed and are omitted for clarity.



NOTES:
1. Clock input pulse has the following characteristics: V_{gen} = 3.0 ± 0.2 V, $t_r = t_f \leq$ 2.5 ns and PRR ≤ 1.0 MHz.
2. Enable characteristics are: $\overline{E}$ > CP, t_{setup} = $\overline{E}$ to CP = 6.0 ns, t_{hold} = D_n to CP = 2.0 ns.
3. For f_{MAX} testing, see table.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 2.0 V or 0.8 V per truth table, $\overline{E}$ = 0.8 V, CP = (See Note 2).
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, $\overline{E}$ = 0.8 V, V_{IN} = 0.8 V or 2.0 V per truth table, CP = (See Note 1).
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, other inputs are open.
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, V_{IN} = GND or 4.5 V per truth table, $\overline{E}$ = GND, V_{OUT} = 2.5 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V or GND per truth table, CP = (See Note 3), $\overline{E}$ = GND, V_{OUT} = GND.
I_{CC}	Power Supply Current		40		40		40	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), CP = (See Note 3).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, **(Repeat at)**, V_{CC} = 5.5 V, V_{INL} = 0.5 V, V_{INH} = 2.5 V.

NOTES:
1. Apply all voltages, then apply 0 V, 3.0 V, 0 V to clock pulse, then make measurement.
2. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to clock pulse, then make measurement.
3. Apply all voltages, then apply 0 V, 3.0 V to clock pulse, then make measurement.
4. f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half the input frequency.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output Output High-Low	3.0	9.0	2.5	10.5	2.5	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 1.0%.
t_{PLH1}	Propagation Delay /Data-Output Output Low-High	2.5	6.5	2.0	8.5	2.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 1.0%.
f_{MAX}	Maximum Clock Frequency	90		70		70		MHz	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 1.0%.