Compiled Memory

5

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OVERVIEW

This section is an overview of the STD130 compiled memory. In STD130 compiled memories provide application-specific memory solution high-density and low-power application. That is, two different compiled memory libraries are available in STD130: STD130-HD(High-Density) and STD130-LP(Low-Power).

The high-density compiled memories are suitable for high integration application. The low-power compiled memories are suitable for portable applications. Each of these memory types may be customized to satisfy the specific circuit requirements. Each memory uses state-of-the-art design architecture techniques. The final memory block is implemented as stand-alone, pitch-matched and customized leafcells. The compiled memory is fully generated by a user-configurable compiler, called memory compiler.
The user defines the memory related specifications such as word depth, bit per word, and column mux type. The compiler then produces any or all of the following items:

— Complete functional model for simulation
— Tabular model for timing and power characteristics
— Automatic generated datasheet including all information for specific memory configuration
— Full GDS and schematic netlist for layout verification
— Phantom cell to use in chip-level floor planning and layout

Additional information about memory compilers can be obtained from your local Samsung and Design Center or Samsung's worldwide headquarters.

COMPILED MEMORY NAMING CONVENTION

In this chapter, we describe the naming convention of memory. The memory name, Figure 5-1 consists of the following convention.

'memory_name':= [memory_code]_[appl_code]_[procs_code]_[opt_code]_[config_code]

Figure 5-1. Compiled Memory Naming Convention

The first string, 'memory_code', is the name of memory type. In STD130 compiled memory types are as follows:

- SPSRAM : Single-Port Synchronous SRAM
- SPSRAMBW : Single-Port Synchronous SRAM with Bit-Write
- SPSRAMR : Single-Port Synchronous SRAM with Redundancy
- DPSRAM : Dual-Port Synchronous SRAM
- DPSRAMBW : Dual-Port Synchronous SRAM with Bit-Write
- SPARAM : Single-Port Asynchronous SRAM
- SPARAMBW : Single-Port Asynchronous SRAM with Bit-Write
- DROM : Synchronous Diffusion-Programmable ROM
- MROM : Synchronous Metal2-Programmable ROM
- ARFRAM : Multi-Port Asynchronous Register File
- FIFO : Synchronous First-In First-Out Memory
- CAM : Synchronous Content Addressable Memory

The second string, 'appl_code', means the specific application to suitably support the compiled memory and the application code is one of HD(High-Density) and LP(Low-Power). The third string, 'procs_code', represents the process and the process code is one of Generic process and Low-Power process(L). In case of Generic process, you don't have to specify 'procs_code'. If there is no process code, it means that the memory is developed under Generic process. If the process code is set to L, it means that the memory is under Low-power process. The fourth string, 'opt_code', represents the number of read and write ports for multi-port memory and the option code is composed of the following convention:

'opt_code' = <n>r<m>w

Currently this field is only used for ARFRAM, where n is the total number of read ports (1~2) and m is the total number of write ports (1~2). The last string, 'config_code', represents the configuration of the memory to be specified. This configuration code is composed of the following convention:

'config_code' = <WORD> x <BPW> m <YMUX> b <BANK>

Where, WORD is the word depth, BPW is bit per word, YMUX is the available column mux type and BANK is the number of bank used. For example, 'spsram_hd_1024x32m16b2' refers to a High-Density single-port synchronous SRAM with 1024 words, 32 bits, 16 column mux and 2 bank under Generic process. Second, 'arfram_hd_1r2w_32x32m2' refers to a High-Density three-port (1 read/2 write) asynchronous register file with 32 word, 32 bits and 2 column mux under Generic process. 'spsram_lpl_1024x32m16' refers to a Low-Power single-port synchronous SRAM with 1024 words, 32 bits 16 column mux under Low-power process.

CHARACTERISTICS FOR TIMING AND POWER

STD130 compiled memories are fully optimized for 1.8V ± 0.15V supply voltage. Compiled memory in this section has been characterized using typical-process at 25 degree and 1.8V supply. The worst-case and best-case parameters can be found by using the derating factor calculated from the following equation:

$$t_{WC}(t_{BC}) = K_{P\_local} \times K_{V\_local} \times K_{T\_local} \times t_{NOM}$$

Where,

t_{WC} is a worst-case propagation delay

t_{BC} is a best-case propagation delay

t_{NOM} is a typical-case propagation delay characterized under typical-process, 25 degree and 1.8V supply

K_{P_local} is a local process derating factor corresponding to each memory type.

K_{V_local} is a local voltage derating factor corresponding to each memory type.

K_{T_local} is a local temperature derating factor that varies by memory type.

Note that K_{P_local}, K_{V_local} and K_{T_local} are only used in compiled memories.

A two-dimensional timing characteristics table look-up model has been adopted to yield more accuracy. Based on the combination of input slopes and output loads, the propagation delay is measured from the input crossing 50% V_{DD} to the output crossing 50% V_{DD}. The timing values reported in the tables are also taken from the same voltage level as the switching characteristics with 0.2ns for input slope and 10SL (Standard Load) for output load.

The power consumption for read and write modes is measured for on input slope of 0.2ns, an output load of 10SL and an input switching activity factor of 0.5. The total power consumption can be calculated by the following equation:

$$P_{total} = ((SA_{read} \times P_{read}) + (SA_{write} \times P_{write})) \times f_{MAX}$$

Where,

P_{total} is the total power consumption in microwatts

P_{read} is the read power consumption in microwatts per MHz

P_{write} is the write power consumption in microwatts per MHz

SA_{read} is the read access ratio on every cycle

SA_{write} is the write access ratio on every cycle

f_{MAX} is the RAM clock frequency in MHz.

The value of SA_{read} or SA_{write} is between 0 and 1. However, the sum of SA_{read} and SA_{write} must be less than or equal to 1.

The power values reported in the tables are also taken from 50% switching activity, SA=0.5. For compiled memory, the read power consumption, the write power consumption and the standby power consumption are available. The standby power consumption is measured on the condition that CSN (Chip Select Negative) disabled and for other signals in their normal operating mode except that OEN (Output Enable Negative) is held low. If any of the signals are not active during standby mode, the standby power is near zero and only static leakage power consumed. In dual-port memories, the power consumption is measured with only one port active and the other port isolated.

BUILT-IN SELF TEST AND BUILT-IN REDUNDANCY-ANALYSIS

Samsung provides engineering design services to support Built-In Self-Test (BIST) and Built-In Redundancy Analysis (BIRA) for compiled memories.

BIST is the recommended test solution for compiled memories. Samsung BIST circuits are designed to detect a complete range of fault types such as stuck-at faults, transition faults, coupling faults, and address macrocells of the same or different types exist together in a circuit, Samsung supports the BIST for all to the memories as a single architecture.

BIRA design services is also provided to test redundancy RAMs with testers. BIRA tests a SRAM and generates fail information after redundancy analysis. The fail information gathered by logic tester is automatically processed and transferred to the laser repair machine. For multiple redundancy RAMs, Samsung BIRA architecture has an integration module to support parallel testing, minimum test pin usage, and optimize logic tester interface.

For more detailed information regarding to the BIST and BIRA, please contact your local Samsung and Design Center or Samsung's worldwide headquarters.

SELECTION GUIDE FOR COMPILED MEMORY

High-Density Compiled Memory

High-Density	Description
SPSRAM_HD	- High-Density Single-Port Synchronous Static RAM - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Dual bank available - Flexible aspect ratio (Ymux = 4, 8, 16, 32)
SPSRAMBW_HD	- High-Density Single-Port Synchronous Static RAM - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Dual bank available - Flexible aspect ratio (Ymux = 4, 8, 16, 32)
SPSRAMR_HD	- High-Density Single-Port Synchronous Static RAM with Redundancy - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Row-only redundancy available - Failure analysis by BIRA and laser repair - Flexible aspect ratio (Ymux = 8, 16, 32)
DPSRAM_HD	- High-Density Dual-Port Synchronous Static RAM - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio (Ymux = 4, 8, 16, 32)
DPSRAMBW_HD	- High-Density Dual-Port Synchronous Static RAM - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio (Ymux = 4, 8, 16, 32)
SPARAM_HD	- High-Density Single-Port Asynchronous Static RAM - Synchronous write operation / Asynchronous read operation - Dual bank available - Flexible aspect ratio (Ymux = 4, 8, 16, 32)
SPARAMBW_HD	- High-Density Single-Port Asynchronous Static RAM - Bit-write feature available - Synchronous write operation / Asynchronous read operation - Dual bank available - Flexible aspect ratio (Ymux = 4, 8, 16, 32)

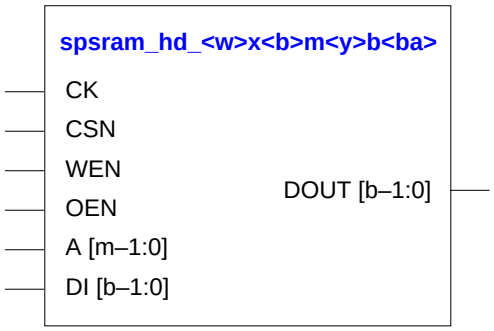
High-Density	Description
DROM_HD	- High-Density Synchronous Diffusion programmable ROM - Diffusion programmable coded - Duty-free clock operation - Zero hold time for address and other control pins - Dual bank available - Flexible aspect ratio (Ymux = 8, 16, 32)
MROM_HD	- High-Density Synchronous Metal-2 programmable ROM - Metal-2 programmable coded - Duty-free clock operation - Zero hold time for address and other control pins - Dual bank available - Flexible aspect ratio (Ymux = 8, 16, 32)
ARFRAM_HD	- High-Density Multi-Port Asynchronous Register File - Synchronous write operation / Asynchronous read operation - 1-to-2 write ports / 1-to-2 read ports - Flexible aspect ratio (Ymux = 2, 4, 8)
FIFO_HD	- High-Density Synchronous First-In First-Out Memory - Duty-free clock operation - Reset and Re-transmit operation available - Flexible aspect ratio (Ymux = 2, 4, 8, 16)
CAM_HD	- High-Density Synchronous Binary Content Addressable Memory - Duty-free clock operation - Single cycle compare operation - Built-in priority address encoder available - Global hit/miss handling

Low-Power Compiled Memory

Low-Power	Description
SPSRAM_LP	- Low-Power Single-Port Synchronous Static RAM - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio (Ymux = 2, 4, 8, 16)
SPSRAMBW_LP	- Low-Power Single-Port Synchronous Static RAM - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio (Ymux = 2, 4, 8, 16)
DPSRAM_LP	- Low-Power Dual-Port Synchronous Static RAM - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio (Ymux = 2, 4, 8, 16)
DPSRAMBW_LP	- Low-Power Dual-Port Synchronous Static RAM - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio (Ymux = 2, 4, 8, 16)
SPARAM_LP	- Low-Power Single-Port Asynchronous Static RAM - Synchronous write operation / Asynchronous read operation - Flexible aspect ratio (Ymux = 2, 4, 8, 16)
SPARAMBW_LP	- Low-Power Single-Port Asynchronous Static RAM - Bit-write feature available - Synchronous write operation / Asynchronous read operation - Flexible aspect ratio (Ymux = 2, 4, 8, 16)

NOTE

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512K bits capacity
- Up to 32K number of words
- Up to 128 number of bits per word

Function Description

SPSRAM_HD is a single-port synchronous static RAM which is provided as a compiler. SPSRAM_HD is intended for use in high-density applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data on DI[] is written into the memory location specified on A[]. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAM_HD Function Table

CK	CSN	WEN	OEN	A	DI	DOUT	COMMENT
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

Parameter Description

SPSRAM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	ba = 1	Min	32	64	128	256
		Max	2048	4096	8192	16384
		Step	16	32	64	128
	ba = 2	Min	64	128	256	512
		Max	4096	8192	16384	32768
		Step	32	64	128	256
Bpw (b)		Min	1	1	1	1
		Max	128	64	32	16
		Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

Unit: [SL]

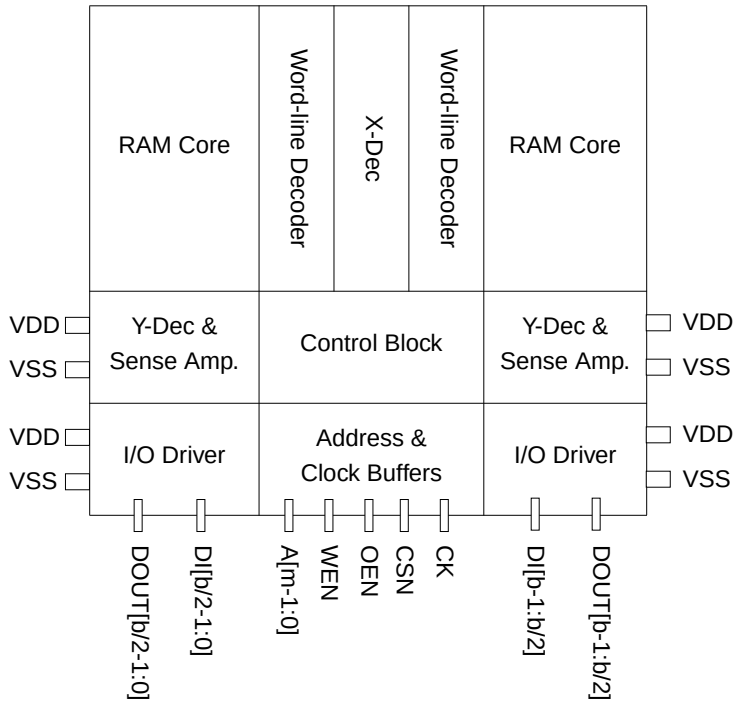
CK	CSN	WEN	OEN	A	DI	DOUT
10.83	6.39	4.45	4.45	4.45	4.45	16.06

NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

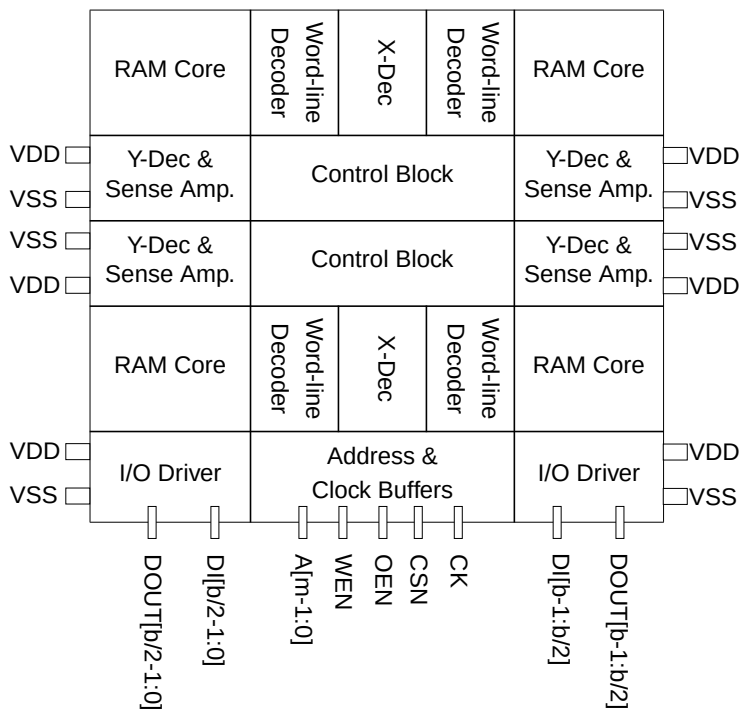
Block Diagrams

SPSRAM_HD has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPSRAM_HD compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the middle-edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>



<2-bank architecture >



Application Notes

1. Permitting over-the-cell routing.
In chip-level layout, over-the-cell routing in SPSRAM_HD is permitted only for Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAM_HD.

4. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**256**	**256**	**512**	**512**	**768**	**768**
bpw	**32**	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	1.94	1.95	2.00	1.98	2.09	2.04	2.18	2.11
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.66	0.68	0.66	0.68	0.67	0.68	0.68	0.69
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.40	0.40	0.38	0.39	0.37	0.37	0.37	0.37
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.53
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.61	1.61	1.66	1.65	1.76	1.71	1.84	1.77
t_{da}	1.15	1.14	1.21	1.17	1.29	1.23	1.37	1.28
t_{dz}	0.10	0.10	0.11	0.11	0.12	0.12	0.13	0.13
t_{zd}	0.13	0.13	0.14	0.14	0.16	0.16	0.17	0.17
t_{od}	0.59	0.59	0.61	0.61	0.63	0.63	0.65	0.65
Power (µW/MHz)								
Power_read	144.92	160.26	202.35	219.94	263.87	283.04	328.57	351.72
Power_write	151.91	166.62	218.63	232.05	300.52	306.10	391.86	388.47
Power_standby	47.65	55.85	65.40	75.64	83.52	96.39	101.11	117.03
Area (µm)								
Width	494.08	579.84	686.08	814.72	878.08	1049.60	1090.68	1305.08
Height	178.42	259.68	225.58	306.84	319.90	401.16	414.22	495.48

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.26	2.17	2.45	2.26	2.48	2.35	2.60
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.68	0.69	0.69	0.68	0.69	0.68	0.67
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.36	0.36	0.35	0.35	0.35	0.35	0.35
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.53	0.54	0.53	0.54	0.53	0.51
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.92	1.83	2.12	1.92	2.15	2.01	2.26
t_{da}	1.44	1.32	1.63	1.40	1.65	1.47	1.70
t_{dz}	0.13	0.13	0.14	0.14	0.14	0.14	0.14
t_{zd}	0.18	0.18	0.19	0.19	0.19	0.19	0.19
t_{od}	0.67	0.67	0.70	0.70	0.72	0.72	0.72
Power (µW/MHz)							
Power_read	392.52	419.57	472.31	493.91	537.70	570.89	623.00
Power_write	491.61	474.42	633.34	582.60	780.80	700.40	848.20
Power_standby	119.50	139.17	137.86	163.08	156.20	187.73	203.00
Area (µm)							
Width	1282.68	1539.96	1474.68	1774.84	1666.68	2009.72	2009.72
Height	508.54	589.80	697.18	778.44	885.82	967.08	1721.64

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**512**	**512**	**1024**	**1024**	**1536**	**1536**
bpw	**16**	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	1.95	1.95	2.00	1.99	2.09	2.05	2.18	2.11
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.66	0.68	0.66	0.68	0.67	0.68	0.68	0.68
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.40	0.40	0.39	0.39	0.38	0.39	0.38	0.38
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.54	0.54	0.54	0.54	0.53	0.54	0.53
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.61	1.61	1.67	1.65	1.76	1.71	1.84	1.77
t_{da}	1.16	1.14	1.21	1.17	1.29	1.23	1.37	1.28
t_{dz}	0.09	0.09	0.10	0.10	0.11	0.11	0.11	0.11
t_{zd}	0.12	0.12	0.13	0.13	0.14	0.14	0.15	0.15
t_{od}	0.57	0.57	0.59	0.59	0.60	0.60	0.62	0.62
Power (µW/MHz)								
Power_read	116.65	130.11	160.09	174.55	207.92	222.17	258.88	275.91
Power_write	124.89	139.54	175.19	189.93	234.88	245.91	301.63	308.92
Power_standby	31.36	39.18	40.98	50.50	51.02	62.46	60.13	73.90
Area (µm)								
Width	494.08	536.96	686.08	750.40	878.08	963.84	1090.68	1197.88
Height	178.42	259.68	225.58	306.84	319.90	401.16	414.22	495.48

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.26	2.17	2.46	2.26	2.48	2.35	2.60
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.68	0.68	0.69	0.68	0.69	0.68	0.67
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.37	0.37	0.37	0.37	0.36	0.36	0.36
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.53	0.54	0.53	0.54	0.53	0.51
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.92	1.83	2.12	1.92	2.15	2.01	2.26
t_{da}	1.44	1.32	1.63	1.40	1.65	1.48	1.70
t_{dz}	0.12	0.12	0.12	0.12	0.13	0.13	0.13
t_{zd}	0.16	0.16	0.17	0.16	017	0.17	0.18
t_{od}	0.64	0.64	0.66	0.66	0.67	0.67	0.67
Power (µW/MHz)							
Power_read	308.45	327.15	373.81	383.06	424.30	440.75	483.30
Power_write	371.36	371.15	467.15	447.76	560.80	529.25	615.70
Power_standby	70.23	86.72	80.29	100.40	90.43	114.43	123.10
Area (µm)							
Width	1282.68	1411.32	1474.68	1624.76	1666.68	1838.20	1838.20
Height	508.54	589.80	697.18	778.44	885.82	967.08	1721.64

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**1024**	**1024**	**2048**	**2048**	**3072**	**3072**
bpw	**8**	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	1.96	1.98	2.02	2.02	2.11	2.08	2.20	2.14
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.66	0.68	0.66	0.68	0.67	0.68	0.68	0.68
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.40	0.40	0.40	0.40	0.39	0.39	0.39	0.39
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.54	0.54	0.54	0.54	0.53	0.54	0.53
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.63	1.64	1.68	1.67	1.77	1.73	1.86	1.80
t_{da}	1.16	1.14	1.21	1.17	1.29	1.23	1.37	1.28
t_{dz}	0.09	0.09	0.10	0.10	0.10	0.10	0.11	0.11
t_{zd}	0.12	0.12	0.13	0.13	0.14	0.14	0.14	0.14
t_{od}	0.57	0.57	0.58	0.58	0.59	0.59	0.61	0.61
Power (µW/MHz)								
Power_read	88.02	101.27	117.15	131.22	150.71	164.10	186.90	202.61
Power_write	91.51	106.57	123.77	139.65	162.73	176.74	206.39	219.79
Power_standby	24.43	31.99	30.59	39.64	37.13	47.78	42.65	54.99
Area (µm)								
Width	494.08	515.52	686.08	718.24	878.08	920.96	1090.68	1144.28
Height	178.42	259.68	225.58	306.84	319.90	401.16	414.22	495.48

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.27	2.20	2.47	2.29	2.50	2.38	2.63
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.68	0.68	0.69	0.68	0.69	0.68	0.67
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.38	0.38	0.38	0.38	0.37	0.37	0.37
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.53	0.54	0.53	0.54	0.53	0.51
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.94	1.86	2.14	1.95	2.16	2.04	2.29
t_{da}	1.44	1.32	1.63	1.40	1.65	1.48	1.70
t_{dz}	0.11	0.11	0.12	0.12	0.12	0.12	0.12
t_{zd}	0.15	0.15	0.15	0.15	0.16	0.16	0.16
t_{od}	0.62	0.62	0.64	0.64	0.65	0.65	0.65
Power (µW/MHz)							
Power_read	222.00	238.66	272.75	278.62	308.80	320.01	358.60
Power_write	251.47	261.65	314.38	311.83	371.00	365.32	421.20
Power_standby	49.29	63.82	55.88	73.06	62.58	82.42	87.79
Area (µm)							
Width	1282.68	1347.00	1474.68	1549.72	1666.68	1752.44	1752.44
Height	508.54	589.80	697.18	778.44	885.82	967.08	1721.64

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**1024**	**1024**	**2048**	**2048**	**4096**	**4096**	**6144**	**6144**
bpw	**4**	**4**	**6**	**6**	**8**	**8**	**10**	**10**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	1.99	2.03	2.05	2.07	2.14	2.13	2.23	2.20
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.66	0.68	0.66	0.68	0.67	0.68	0.68	0.68
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.41	0.41	0.40	0.40	0.39	0.39	0.39	0.39
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.54	0.54	0.54	0.54	0.53	0.54	0.53
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.65	1.69	1.70	1.73	1.80	1.79	1.89	1.85
t_{da}	1.16	1.14	1.21	1.17	1.29	1.23	1.37	1.28
t_{dz}	0.09	0.09	0.09	0.09	0.10	0.10	0.10	0.10
t_{zd}	0.12	0.12	0.12	0.12	0.13	0.13	0.14	0.14
t_{od}	0.57	0.57	0.58	0.58	0.59	0.59	0.60	0.60
Power (µW/MHz)								
Power_read	73.69	87.03	95.57	109.80	121.91	135.38	150.87	165.93
Power_write	74.35	89.81	97.31	113.99	125.56	141.40	157.38	173.46
Power_standby	20.44	27.86	24.61	33.43	29.17	39.39	32.37	43.74
Area (µm)								
Width	494.08	504.80	686.08	702.16	878.08	899.52	1090.68	1117.48
Height	178.42	259.68	225.58	306.84	319.90	401.16	414.22	495.48

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

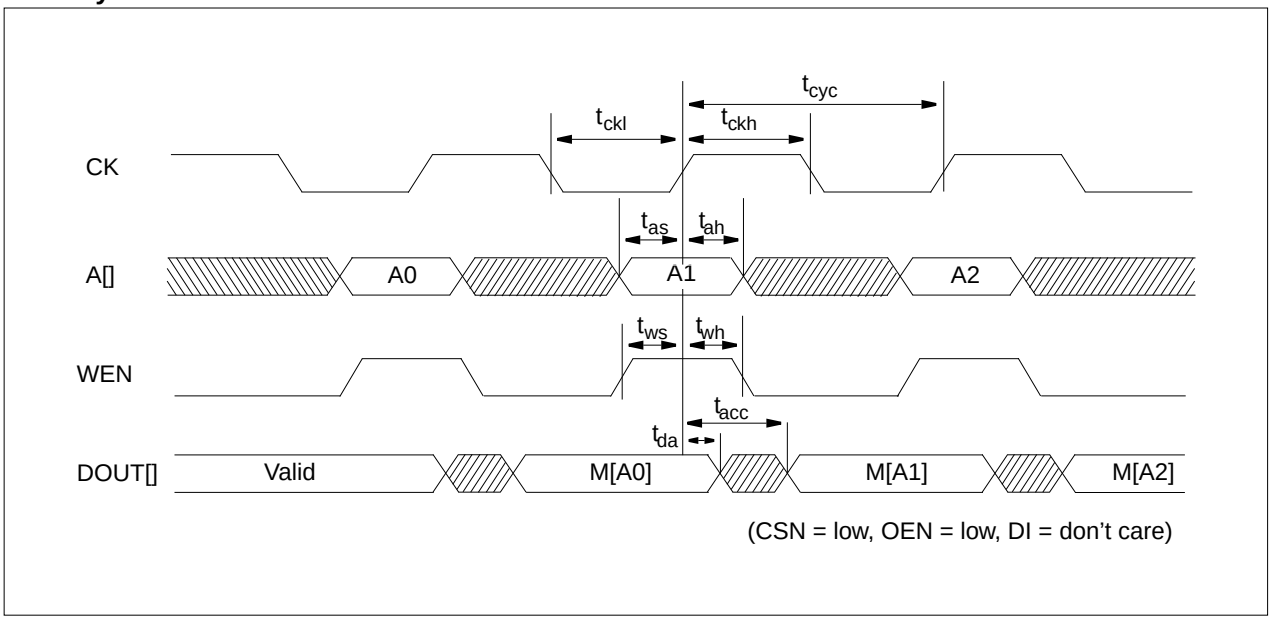
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**8192**	**8192**	**12288**	**12288**	**16384**	**16384**	**32768**
bpw	**12**	**12**	**14**	**14**	**16**	**16**	**16**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.31	2.26	2.50	2.35	2.53	2.44	2.69
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.68	0.68	0.69	0.68	0.69	0.68	0.67
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.38	0.38	0.38	0.38	0.38	0.38	0.38
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.53	0.54	0.53	0.54	0.53	0.51
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.96	1.91	2.16	2.00	2.19	2.09	2.34
t_{da}	1.44	1.32	1.63	1.40	1.65	1.48	1.70
t_{dz}	0.11	0.11	0.11	0.11	0.12	0.12	0.12
t_{zd}	0.14	0.14	0.15	0.15	0.15	0.15	0.15
t_{od}	0.61	0.61	0.62	0.62	0.64	0.64	0.64
Power (µW/MHz)							
Power_read	178.79	194.59	222.44	226.86	251.10	260.48	296.20
Power_write	189.75	204.73	236.25	241.90	274.10	281.34	321.90
Power_standby	37.12	50.47	41.89	57.37	46.58	64.30	67.98
Area (µm)							
Width	1282.68	1314.84	1474.68	1512.20	1666.68	1709.56	1709.56
Height	508.54	589.80	697.18	778.44	885.82	967.08	1721.64

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

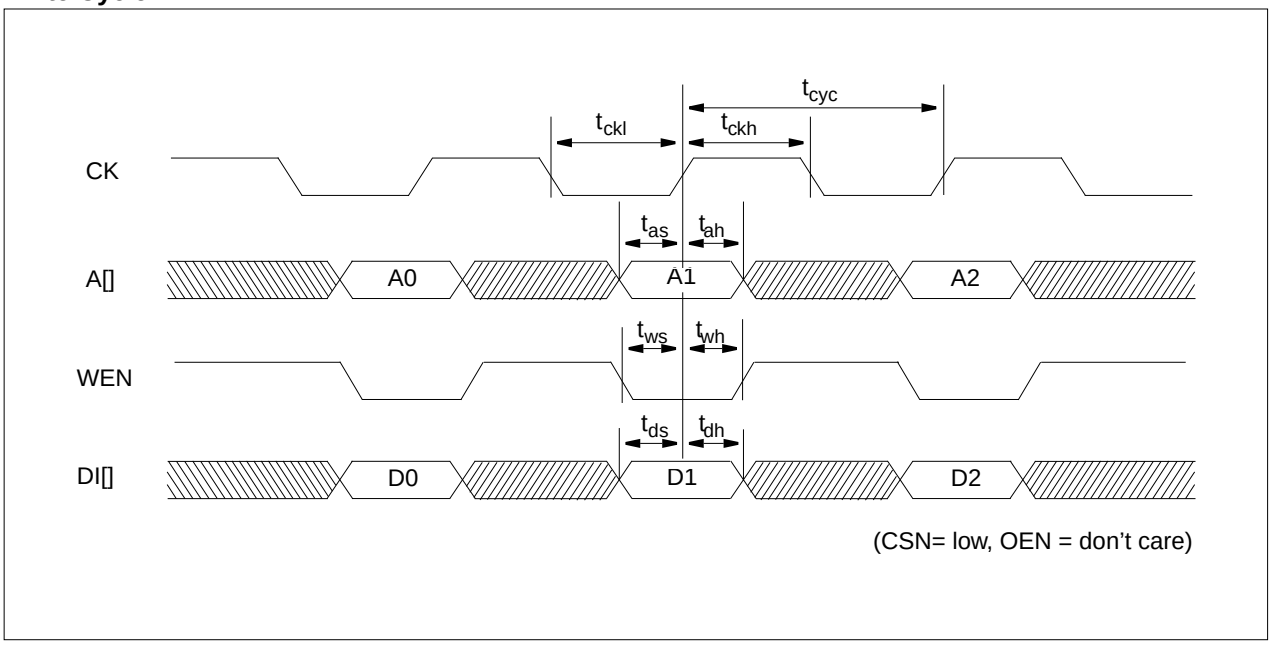
Timing Diagrams

Read Cycle



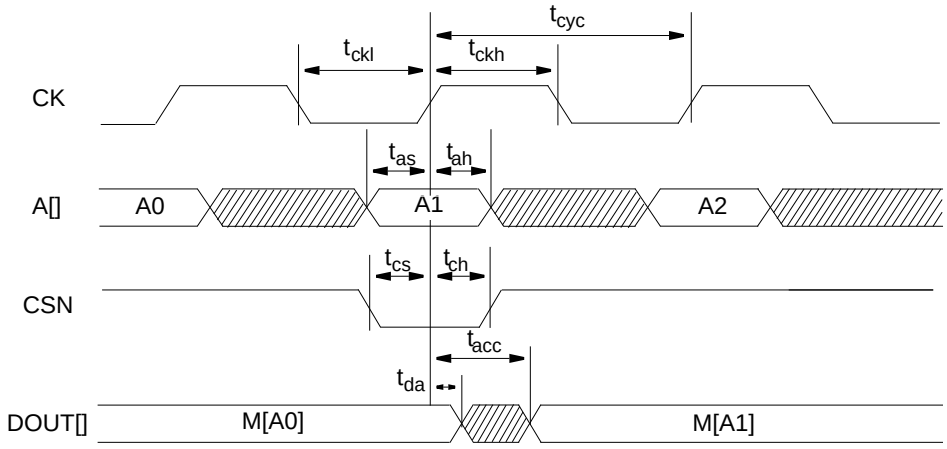
(CSN = low, OEN = low, DI = don't care)

Write Cycle



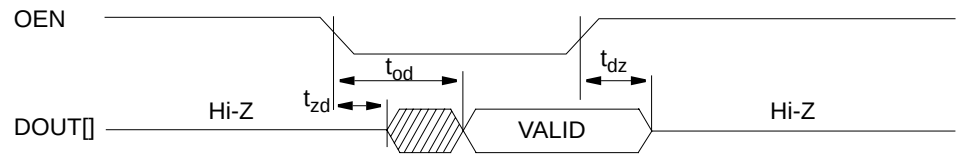
(CSN= low, OEN = don't care)

Read Cycle with CSN Controlled



(OEN = low, WEN = high, DI = don't care)

OEN Controlled Output Enable



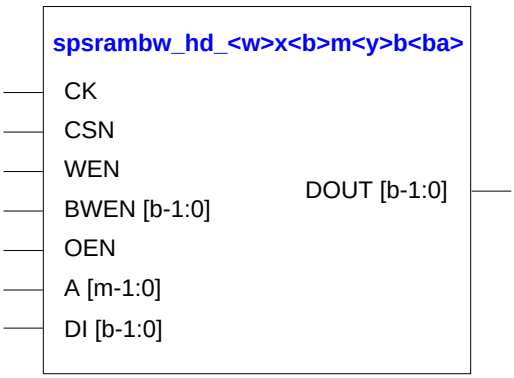
(CK, A, WEN, DI, CSN = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

SPSRAMBW_HD

High-Density Single-Port Synchronous Static RAM with Bit-Write

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Bit-Write capability
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tristate output
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512K bits capacity
- Up to 32K number of words
- Up to128 number of bit per word

Function Description

SPSRAMBW_HD is a single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMBW_HD is intended for use in high-density applications. Basically, its functionality is exactly same as SPSRAM_HD except a bit-write operation which is controlled by BWEN[], named bit-write enable signal bus. Each bit of BWEN[] enables or disables the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data bits in DI[], which their corresponding bit(s) in BWEN[] are low, are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM_HD. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAMBW_HD Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

Parameter Description

SPSRAMBW_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba)

Parameters			Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux =(y) 32
Words (w)	ba = 1	Min	32	64	128	256
		Max	2048	4096	8192	16384
		Step	16	32	64	128
	ba = 2	Min	64	128	256	512
		Max	4096	8192	16384	32768
		Step	32	64	128	256
Bpw (b)		Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
BWEN[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A[]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI[]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT[]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

Unit: [SL]

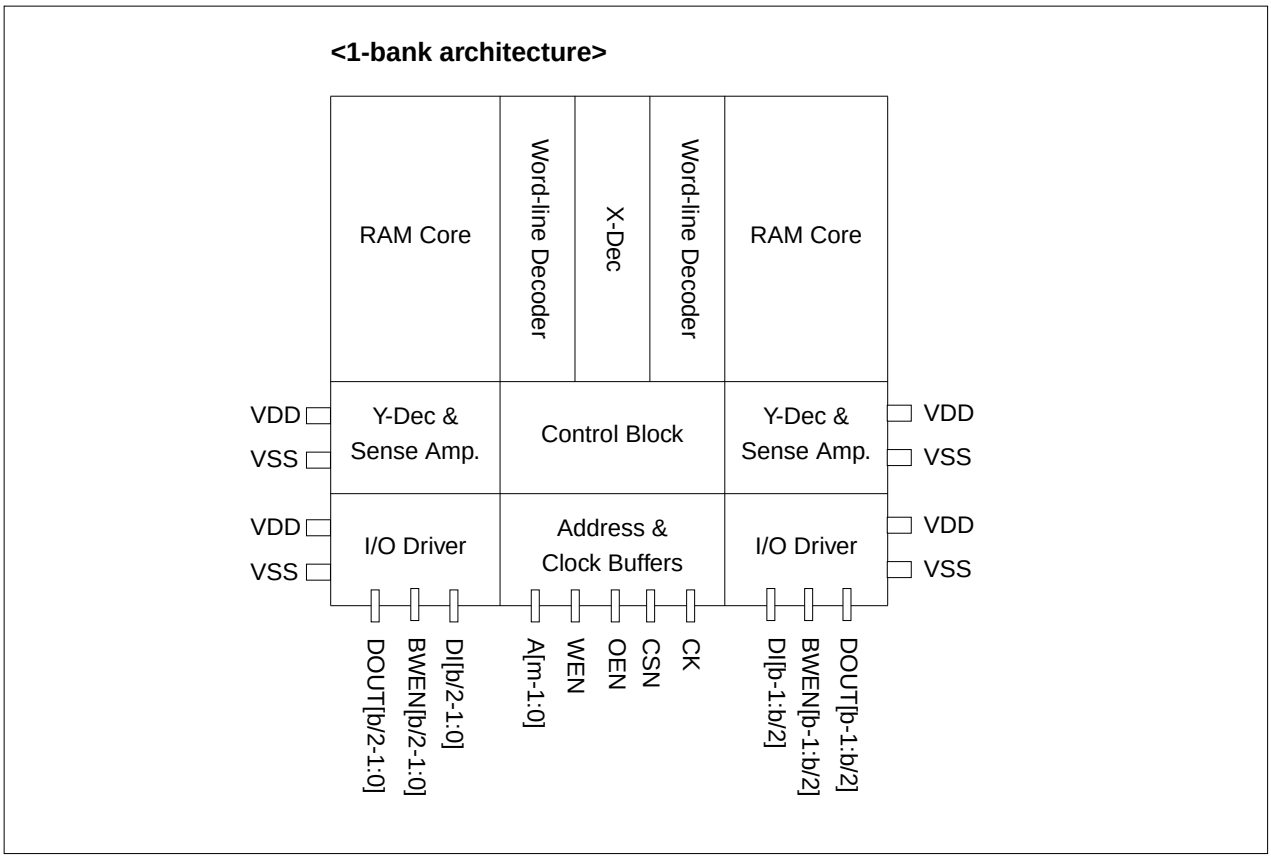
CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
10.83	6.39	4.45	4.45	4.45	4.45	4.45	16.06

NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

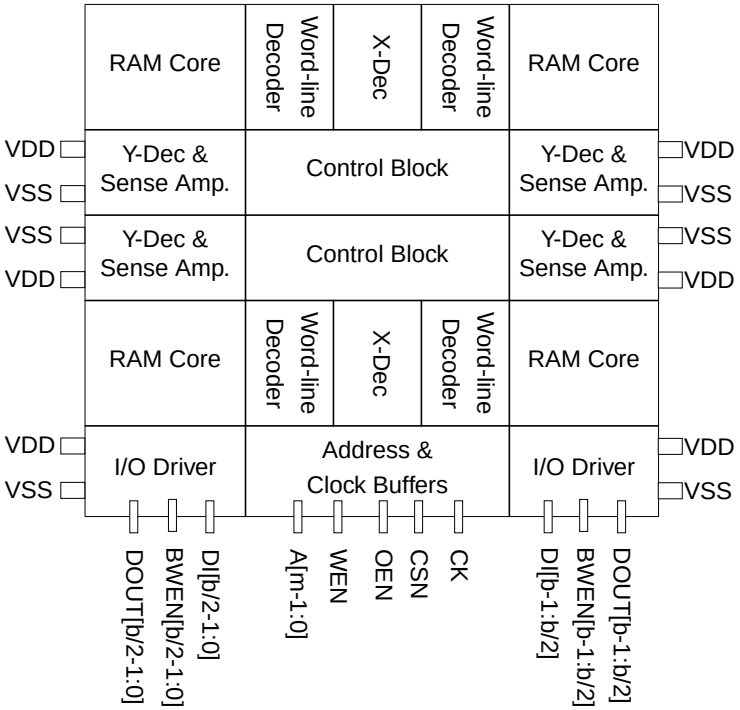
Block Diagrams

SPSRAMBW_HD has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPSRAMBW_HD compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the middle-edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>



<2-bank architecture >



Application Notes

1. Permitting Over-the-cell routing
In chip-level layout, over-the-cell routing in SPSRAMBW_HD is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAMBW_HD.

4. A byte-write or word-write operation with SPSRAMBW_HD.
Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPSRAM_HD. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

5. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{bws}	BWEN setup time
t_{bwh}	BWEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**256**	**256**	**512**	**512**	**768**	**768**
bpw	**32**	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	1.92	1.92	1.98	1.96	2.08	2.03	2.18	2.10
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.66	0.68	0.66	0.68	0.67	0.68	0.68	0.69
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.40	0.40	0.38	0.39	0.37	0.37	0.37	0.37
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.53
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.37	0.38	0.36	0.37	0.35	0.36	0.34	0.36
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.56	1.56	1.61	1.60	1.70	1.66	1.79	1.72
t_{da}	1.15	1.14	1.20	1.17	1.29	1.22	1.37	1.28
t_{dz}	0.10	0.10	0.11	0.11	0.12	0.12	0.13	0.13
t_{zd}	0.13	0.13	0.14	0.14	0.16	0.16	0.17	0.17
t_{od}	0.58	0.58	0.60	0.60	0.62	0.62	0.65	0.65
Power (µW/MHz)								
Power_read	157.48	163.31	219.68	227.61	284.46	325.52	353.63	366.12
Power_write	172.17	174.63	246.45	246.30	334.14	294.53	433.27	413.05
Power_standby	53.81	57.95	73.45	79.33	93.10	101.37	113.19	124.29
Area (µm)								
Width	494.08	579.84	686.08	814.72	878.08	1049.60	1090.68	1305.08
Height	178.42	259.68	225.58	306.84	319.90	401.16	414.22	495.48

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.26	2.16	2.48	2.27	2.51	2.37	2.64
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.68	0.69	0.69	0.68	0.70	0.68	0.67
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.36	0.36	0.35	0.35	0.35	0.35	0.35
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.53	0.54	0.53	0.54	0.53	0.51
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.33	0.36	0.33	0.36	0.32	0.36	0.38
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.87	1.78	2.07	1.87	2.10	1.96	2.21
t_{da}	1.44	1.32	1.63	1.40	1.65	1.47	1.70
t_{dz}	0.13	0.13	0.14	0.14	0.14	0.14	0.14
t_{zd}	0.18	0.18	0.18	0.18	0.19	0.19	0.19
t_{od}	0.67	0.67	0.70	0.70	0.72	0.72	0.72
Power (µW/MHz)							
Power_read	421.51	436.46	501.16	515.06	569.39	597.00	649.35
Power_write	538.10	502.70	683.61	614.11	835.34	735.04	876.66
Power_standby	133.36	147.70	153.78	173.19	174.26	199.55	214.28
Area (µm)							
Width	1282.68	1539.96	1474.68	1774.84	1666.68	2009.72	2009.72
Height	508.54	589.80	697.18	778.44	885.82	967.08	1721.64

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**512**	**512**	**1024**	**1024**	**1536**	**1536**
bpw	**16**	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	1.92	1.92	1.98	1.97	2.08	2.03	2.18	2.10
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.66	0.68	0.66	0.68	0.67	0.68	0.68	0.68
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.40	0.40	0.39	0.39	0.38	0.38	0.38	0.38
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.53
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.38	0.38	0.37	0.38	0.36	0.37	0.35	0.37
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.56	1.56	1.61	1.60	1.71	1.66	1.79	1.72
t_{da}	1.16	1.14	1.21	1.17	1.29	1.23	1.37	1.28
t_{dz}	0.09	0.09	0.10	0.10	0.11	0.11	0.11	0.11
t_{zd}	0.12	0.12	0.13	0.13	0.14	0.14	0.15	0.15
t_{od}	0.57	0.57	0.59	0.59	0.60	0.60	0.62	0.62
Power (µW/MHz)								
Power_read	127.53	131.30	174.82	179.30	224.78	229.48	278.95	283.56
Power_write	143.81	147.19	201.38	203.63	267.29	264.71	340.57	331.31
Power_standby	33.97	37.90	43.68	49.03	53.34	60.51	63.28	72.38
Area (µm)								
Width	494.08	536.96	686.08	750.40	878.08	963.84	1090.68	1197.88
Height	178.42	259.68	225.58	306.84	319.90	401.16	414.22	495.48

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.26	2.17	2.48	2.27	2.51	2.37	2.64
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.68	0.68	0.68	0.68	0.70	0.68	0.67
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.37	0.37	0.37	0.37	0.36	0.36	0.36
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.53	0.54	0.53	0.54	0.53	0.51
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.35	0.37	0.34	0.37	0.34	0.37	0.40
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.87	1.78	2.07	1.87	2.10	1.96	2.21
t_{da}	1.44	1.32	1.63	1.40	1.65	1.47	1.70
t_{dz}	0.12	0.12	0.12	0.12	0.13	0.13	0.13
t_{zd}	0.16	0.16	0.16	0.16	0.17	0.17	0.17
t_{od}	0.64	0.64	0.66	0.66	0.67	0.67	0.67
Power (µW/MHz)							
Power_read	331.78	336.04	396.20	394.46	449.45	455.18	494.97
Power_write	416.35	398.54	517.95	478.72	617.05	564.19	647.66
Power_standby	73.21	84.43	83.33	97.64	93.58	111.30	119.57
Area (µm)							
Width	1282.68	1411.32	1474.68	1624.76	1666.68	1838.20	1838.20
Height	508.54	589.80	697.18	778.44	885.82	967.08	1721.64

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**1024**	**1024**	**2048**	**2048**	**3072**	**3072**
bpw	**8**	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	1.94	1.96	2.00	2.00	2.10	2.06	2.20	2.14
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.66	0.66	0.66	0.68	0.67	0.68	0.68	0.68
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.40	0.40	0.40	0.40	0.39	0.39	0.39	0.39
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.53
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.38	0.38	0.38	0.39	0.37	0.39	0.37	0.39
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.57	1.57	1.63	1.62	1.72	1.68	1.81	1.75
t_{da}	1.16	1.16	1.21	1.17	1.29	1.23	1.37	1.28
t_{dz}	0.09	0.09	0.10	0.10	0.10	0.10	0.11	0.11
t_{zd}	0.12	0.12	0.13	0.13	0.13	0.13	0.14	0.14
t_{od}	0.57	0.57	0.58	0.58	0.59	0.59	0.61	0.61
Power (µW/MHz)								
Power_read	98.20	101.88	130.75	134.91	165.98	169.75	205.12	208.08
Power_write	107.31	111.32	144.95	148.68	188.25	189.21	237.29	234.18
Power_standby	25.31	29.61	30.49	36.16	35.63	42.90	40.92	49.78
Area (µm)								
Width	494.08	515.52	686.08	718.24	878.08	920.96	1090.68	1144.28
Height	178.42	259.68	225.58	306.84	319.90	401.16	414.22	495.48

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.28	2.20	2.50	2.50	2.53	2.40	2.68
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.68	0.68	0.69	0.68	0.70	0.68	0.67
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.38	0.38	0.38	0.38	0.37	0.37	0.37
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.53	0.54	0.53	0.54	0.53	0.51
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.36	0.39	0.36	0.39	0.35	0.39	0.41
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.89	1.80	2.08	1.90	2.11	1.99	2.24
t_{da}	1.44	1.32	1.63	1.40	1.65	1.47	1.70
t_{dz}	0.11	0.11	0.12	0.12	0.12	0.12	0.12
t_{zd}	0.15	0.15	0.15	0.15	0.16	0.16	0.16
t_{od}	0.62	0.62	0.63	0.63	0.65	0.65	0.65
Power (μW/MHz)							
Power_read	242.79	244.56	293.00	286.30	331.49	330.11	363.08
Power_write	286.67	278.46	355.19	331.39	416.48	387.85	441.04
Power_standby	46.23	56.77	51.74	64.39	57.27	72.22	76.97
Area (μm)							
Width	1282.68	1347.00	1474.68	1549.72	1666.68	1752.44	1752.44
Height	508.54	589.80	697.18	778.44	885.82	967.08	1721.64

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**1024**	**1024**	**2048**	**2048**	**4096**	**4096**	**6144**	**6144**
bpw	**4**	**4**	**6**	**6**	**8**	**8**	**10**	**10**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	1.97	2.02	2.03	2.06	2.13	2.13	2.23	2.20
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.66	0.68	0.66	0.68	0.67	0.68	0.68	0.68
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.41	0.41	0.40	0.40	0.39	0.39	0.39	0.39
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.53
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.40	0.42	0.39	0.42	0.38	0.41	0.38	0.41
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.60	1.64	1.65	1.68	1.74	1.73	1.83	1.80
t_{da}	1.16	1.14	1.21	1.17	1.29	1.23	1.37	1.28
t_{dz}	0.09	0.09	0.09	0.09	0.10	0.10	0.10	0.10
t_{zd}	0.11	0.11	0.12	0.12	0.13	0.13	0.14	0.14
t_{od}	0.56	0.56	0.57	0.57	0.59	0.59	0.60	0.60
Power (μW/MHz)								
Power_read	83.75	87.31	108.82	112.80	136.62	139.92	168.27	185.42
Power_write	89.01	93.83	116.50	121.33	148.32	151.24	184.76	170.84
Power_standby	20.91	25.81	23.58	29.81	26.22	33.90	28.96	38.06
Area (μm)								
Width	494.08	504.80	686.08	702.16	878.08	899.52	1090.68	1117.48
Height	178.42	259.68	225.58	306.84	319.90	401.16	414.22	495.48

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

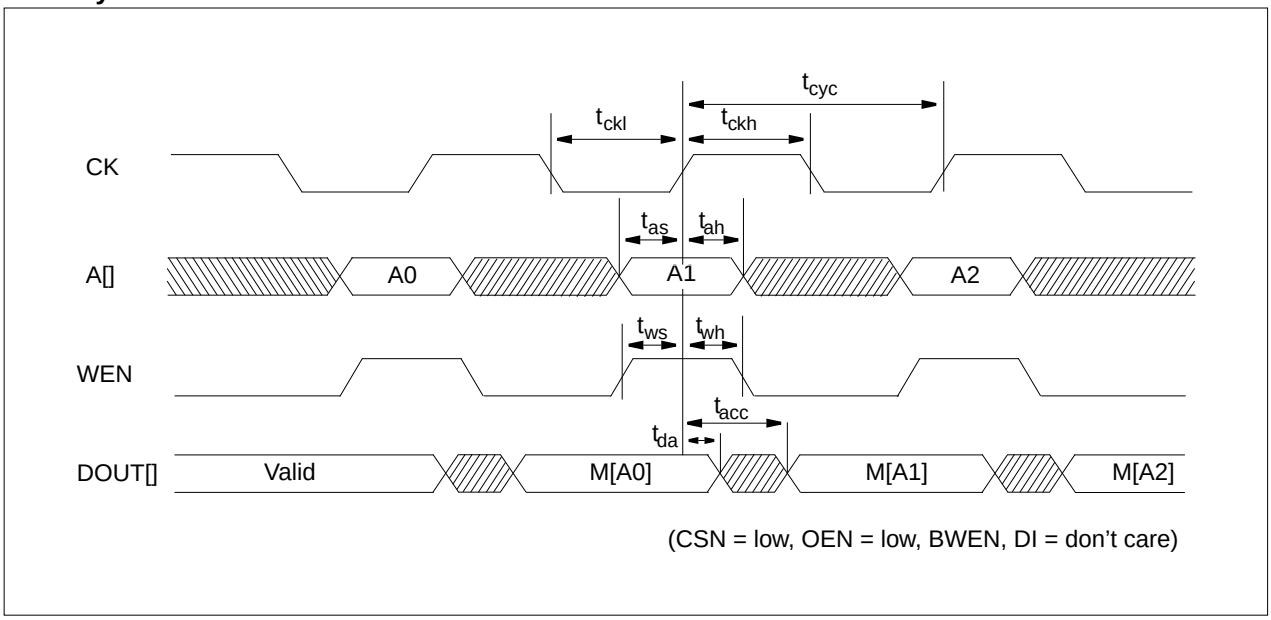
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**8192**	**8192**	**12288**	**12288**	**16384**	**16384**	**32768**
bpw	**12**	**12**	**14**	**14**	**16**	**16**	**16**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.32	2.26	2.53	2.36	2.56	2.46	2.74
t_{ckl}	0.61	0.61	0.61	0.61	0.61	0.61	0.61
t_{ckh}	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t_{as}	0.68	0.68	0.69	0.68	0.70	0.68	0.67
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.31	0.31	0.31	0.31	0.31	0.31	0.31
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.38	0.38	0.38	0.38	0.38	0.38	0.38
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.54	0.53	0.54	0.53	0.54	0.53	0.51
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.38	0.41	0.37	0.41	0.37	0.41	0.43
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.91	1.86	2.11	1.95	2.14	2.04	2.29
t_{da}	1.44	1.32	1.63	1.40	1.65	1.47	1.70
t_{dz}	0.11	0.11	0.11	0.11	0.12	0.12	0.12
t_{zd}	0.14	0.14	0.15	0.15	0.15	0.15	0.15
t_{od}	0.61	0.61	0.62	0.62	0.64	0.64	0.64
Power (µW/MHz)							
Power_read	198.48	199.52	241.02	232.80	272.30	267.82	297.00
Power_write	220.68	218.03	272.11	256.85	314.51	298.11	336.59
Power_standby	31.71	42.26	34.69	46.84	37.72	51.52	54.50
Area (µm)							
Width	1282.68	1314.84	1474.68	1512.20	1666.68	1709.56	1709.56
Height	508.54	589.80	697.18	778.44	885.82	967.08	1721.64

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

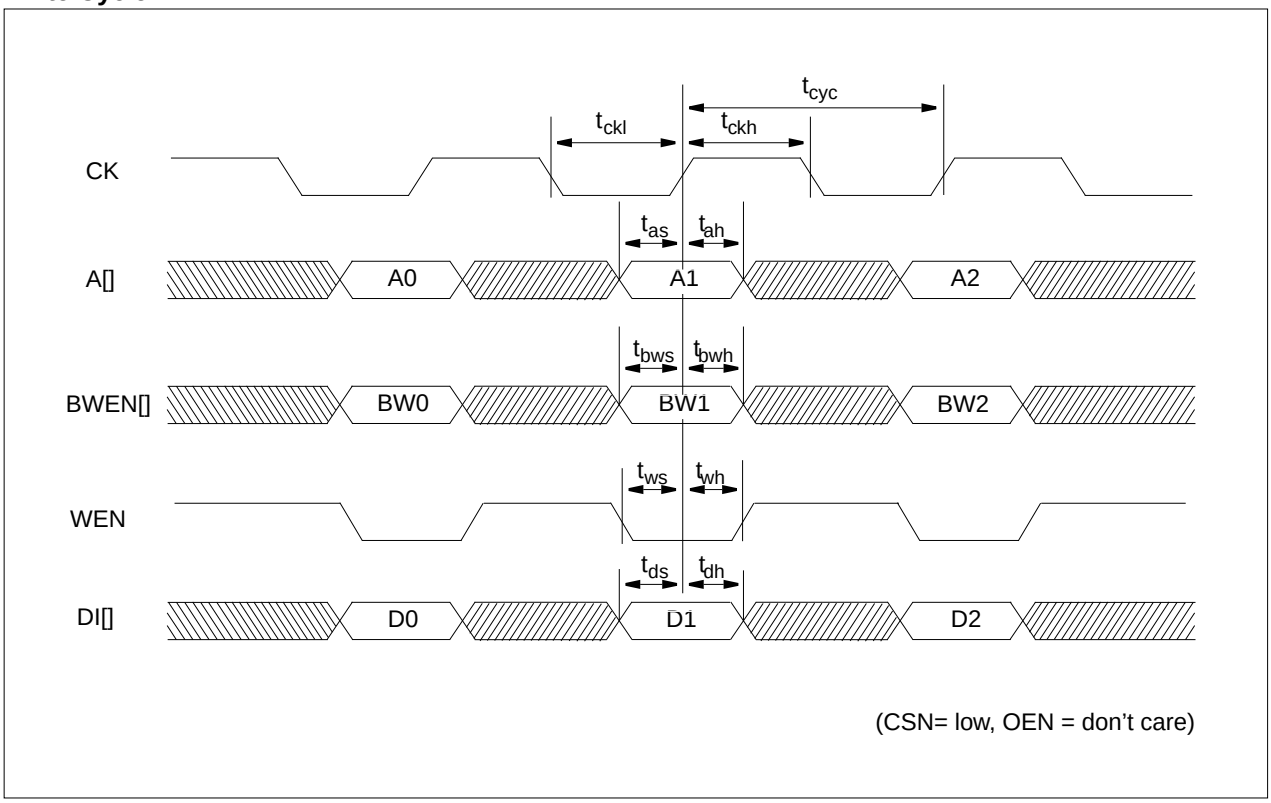
Timing Diagrams

Read Cycle



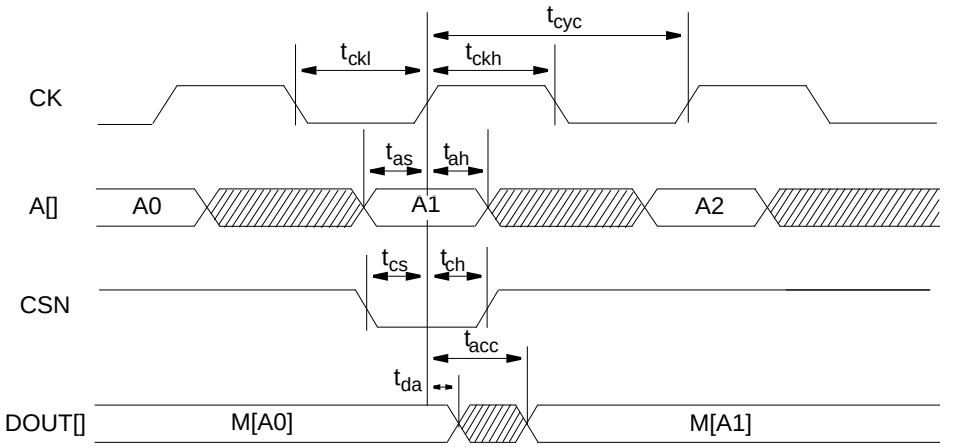
(CSN = low, OEN = low, BWEN, DI = don't care)

Write Cycle



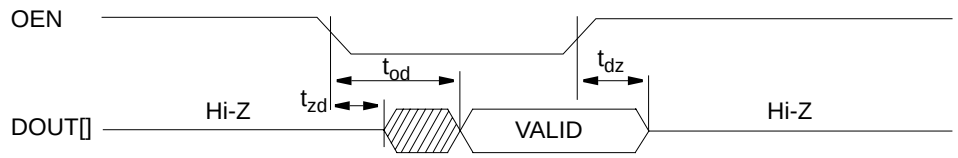
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



(OEN = low, WEN = high, BWEN, DI = don't care)

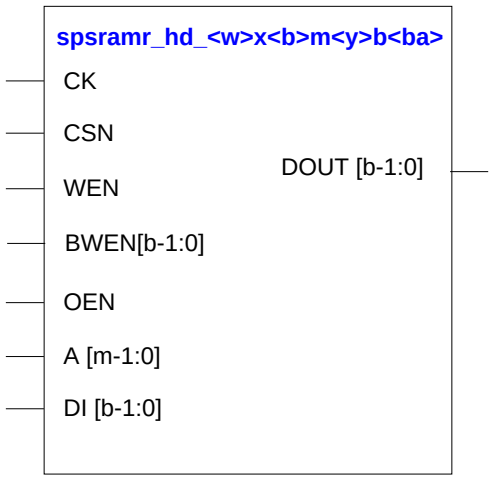
OEN-Controlled Output Enable



(CSN, CK, A, WEN, BWEN, DI = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words (w) is the number of words.
2. Bpw (b) is the number of bit per word.
3. Ymux (y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-capacity application
- Heuristic row-redundancy available
- Bit-write capability
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- 64Kbits ~ 1Mbits capacity
- 2K ~ 32K number of words
- 8 ~ 128 number of bits per word

Function Description

SPSRAMR_HD is a repairable single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMR_HD is intended for use in high-capacity applications. Basically, its functionality is exactly same as SPSRAMBW_HD. Each bit of BWEN[] enables or disable the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data bytes or bits in DI[], which their corresponding bit(s) in BWEN[] are low, are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM_HD. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAMR_HD Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L/H	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

SPSRAMR_HD

Single-Port Synchronous Static RAM with Redundancy

Parameter Description

SPSRAMR_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	ba = 1	Min	2048	4096	8192
		Max	4096	8192	16384
		Step	64	128	256
	ba = 2	Min	4096	8192	16384
		Max	8192	16384	32768
		Step	128	256	512
Bpw (b)		Min	32	16	8
		Max	128	64	32
		Step	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A[]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI[]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT[]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

(Unit = SL)

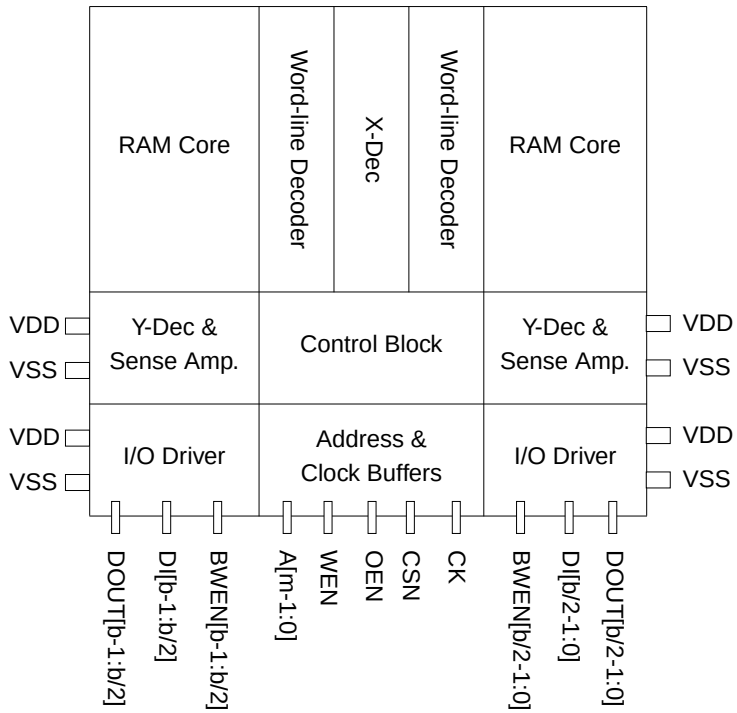
CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
12.0309	2.7273	2.8433	3.1528	4.7002	2.9594	3.0754	11.2573

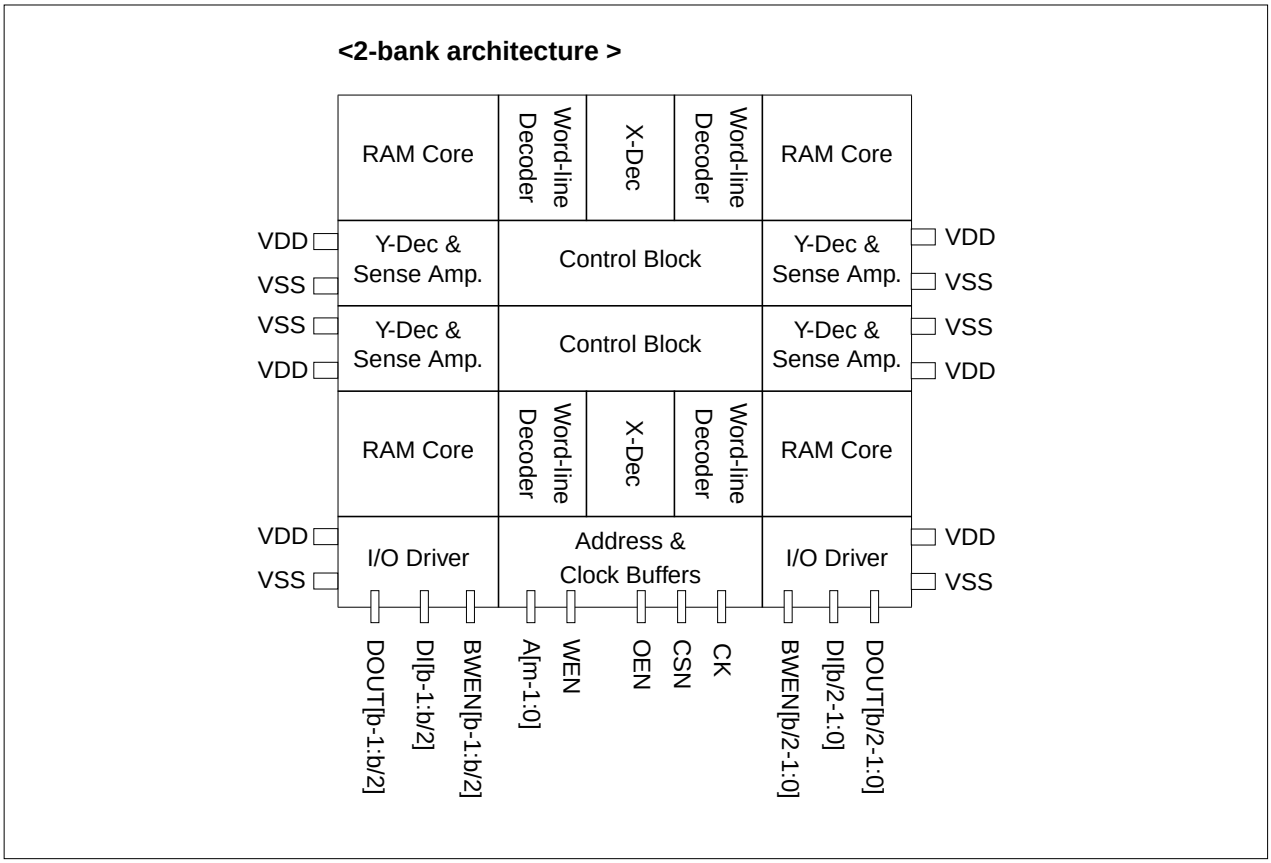
NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank

Block Diagrams

SPSRAMR_HD has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPSRAMR_HD compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the middle-edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the top-edge, the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>





Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in SPSRAMR_HD is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAMR_HD.

4. A byte-write or word-write operation with SPSRAMR_HD. Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPSRAM_HD. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

5. Power reduction during standby mode. The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{bws}	BWEN setup time
t_{bwh}	BWEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**2048**	**4096**	**2048**	**4096**	**4096**	**8192**	**4096**	**8192**
bpw	**32**	**32**	**64**	**64**	**64**	**64**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.80	2.86	2.84	2.91	3.04	3.06	3.19	3.24
t_{ckl}	0.46	0.46	0.46	0.46	0.46	0.46	0.46	0.46
t_{ckh}	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27
t_{as}	0.41	0.43	0.41	0.43	0.41	0.44	0.41	0.44
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.48	0.48	0.47	0.47	0.47	0.47	0.47	0.47
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.52	0.52	0.51	0.51	0.51	0.51	0.50	0.50
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.66	2.73	2.70	2.77	2.71	2.83	2.83	2.95
t_{da}	2.39	2.41	2.40	2.43	2.40	2.46	2.41	2.47
t_{dz}	0.24	0.24	0.25	0.25	0.25	0.25	0.26	0.26
t_{zd}	0.38	0.38	0.40	0.40	0.40	0.40	0.40	0.40
t_{od}	0.61	0.60	0.67	0.66	0.67	0.66	0.82	0.81
Power (µW/MHz)								
Power_read	277.12	386.29	483.65	675.99	491.41	702.04	914.21	1312.40
Power_write	334.47	452.57	597.93	807.05	667.45	890.56	1282.10	1704.30
Power_standby	61.78	80.26	108.30	138.09	109.03	147.26	203.89	273.41
Area (µm)								
Width	998.96	1084.72	1766.96	1938.48	1766.96	1938.48	3302.96	3646.00
Height	521.58	991.64	521.58	991.64	912.54	1773.56	926.22	1800.92

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**4096**	**8192**	**4096**	**8192**	**8192**	**16384**	**8192**	**16384**
bpw	**16**	**16**	**32**	**32**	**32**	**32**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.81	2.89	2.86	2.94	3.03	3.06	3.24	3.23
t_{ckl}	0.46	0.46	0.46	0.46	0.46	0.46	0.46	0.46
t_{ckh}	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27
t_{as}	0.42	0.43	0.41	0.43	0.41	0.44	0.41	0.44
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.48	0.48	0.47	0.47	0.47	0.47	0.47	0.47
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.52	0.52	0.51	0.51	0.51	0.51	0.51	0.51
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.68	2.76	2.72	2.80	2.73	2.86	2.84	2.97
t_{da}	2.39	2.41	2.40	2.43	2.40	2.46	2.41	2.47
t_{dz}	0.24	0.24	0.25	0.25	0.25	0.25	0.26	0.26
t_{zd}	0.38	0.38	0.40	0.39	0.39	0.39	0.40	0.40
t_{od}	0.60	0.60	0.64	0.64	0.64	0.64	0.76	0.76
Power (µW/MHz)								
Power_read	260.05	376.36	450.22	655.49	456.53	675.58	846.09	1261.50
Power_write	288.84	414.41	506.58	732.14	545.08	779.81	1028.90	1475.50
Power_standby	49.71	74.36	84.16	126.45	84.94	132.21	155.73	243.85
Area (µm)								
Width	998.96	1041.84	1766.96	1852.72	1766.96	1852.72	3302.96	3474.48
Height	521.58	991.64	521.58	991.64	912.54	1773.56	926.22	1800.92

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

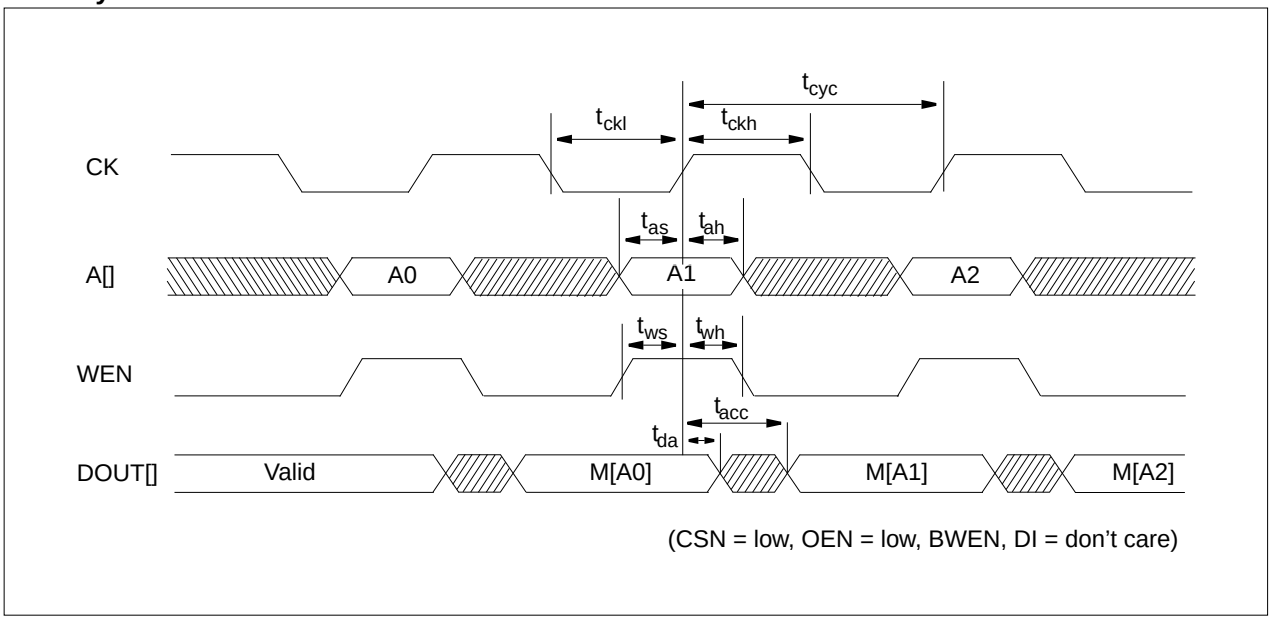
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**8192**	**16384**	**8192**	**16384**	**16384**	**32768**	**16384**	**32768**
bpw	**8**	**8**	**16**	**16**	**16**	**16**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.84	2.95	2.89	3.00	3.38	3.41	3.23	3.22
t_{ckl}	0.46	0.46	0.46	0.46	0.46	0.46	0.46	0.46
t_{ckh}	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27
t_{as}	0.41	0.43	0.41	0.43	0.41	0.44	0.41	0.44
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.48	0.48	0.48	0.48	0.48	0.48	0.47	0.47
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.52	0.52	0.51	0.51	0.51	0.61	0.51	0.51
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.71	2.81	2.75	2.85	2.79	2.94	2.87	3.03
t_{da}	2.39	2.41	2.40	2.43	2.41	2.47	2.41	2.47
t_{dz}	0.23	0.23	0.25	0.25	0.25	0.24	0.25	0.25
t_{zd}	0.38	0.38	0.39	0.39	0.39	0.39	0.39	0.39
t_{od}	0.59	0.59	0.63	0.63	0.63	0.63	0.74	0.74
Power (µW/MHz)								
Power_read	246.92	362.59	423.44	625.55	429.95	644.95	792.78	1198.40
Power_write	261.59	385.51	451.63	674.63	474.24	706.05	881.78	1322.70
Power_standby	39.67	63.33	63.98	104.32	64.81	108.28	115.27	195.47
Area (µm)								
Width	998.96	1020.40	1766.96	1809.84	1766.96	1809.84	3302.96	3388.72
Height	521.58	991.64	521.58	991.64	912.54	1773.56	926.22	1800.92

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode.

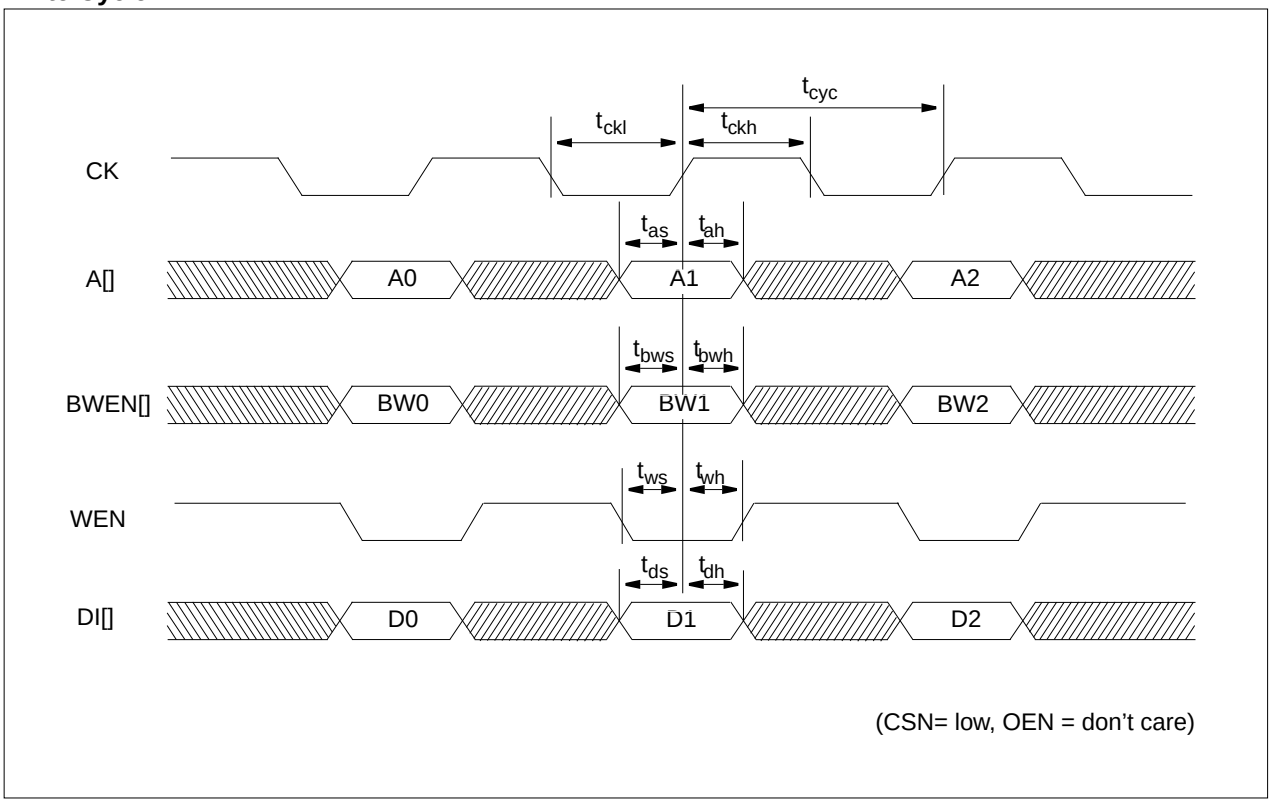
Timing Diagrams

Read Cycle



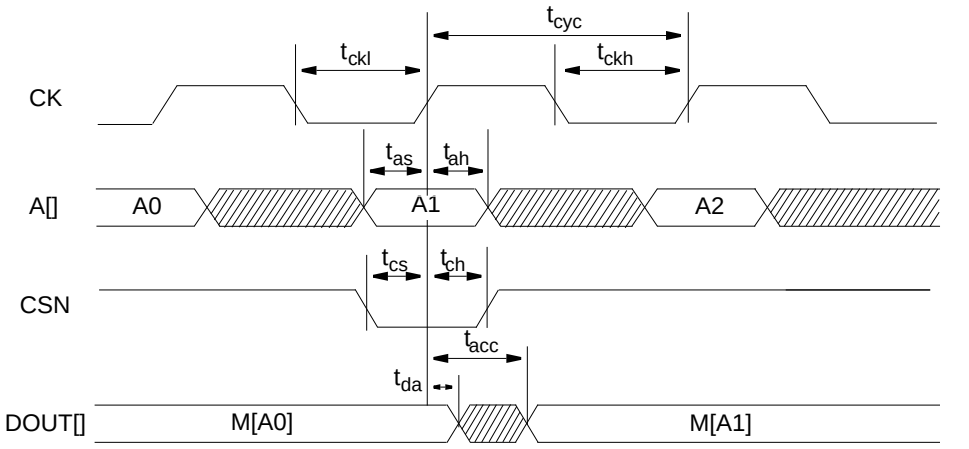
(CSN = low, OEN = low, BWEN, DI = don't care)

Write Cycle

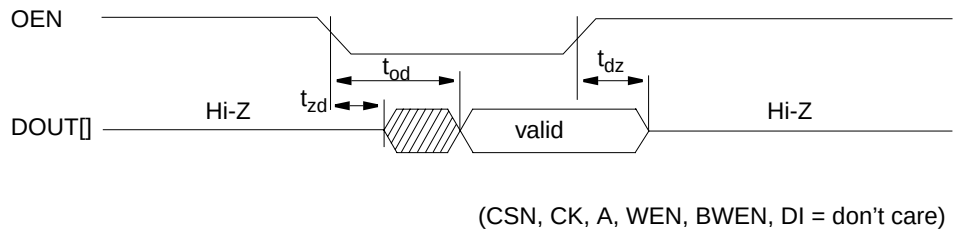


(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled

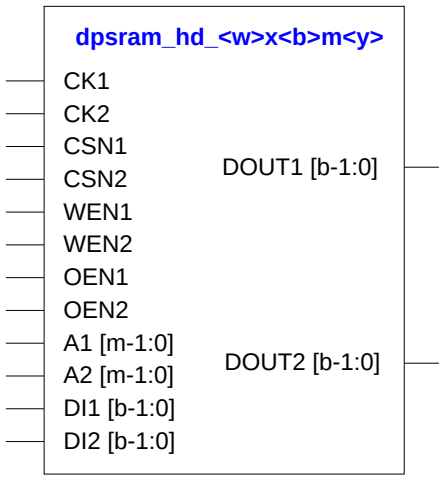


OEN-Controlled Output Enable



NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 256K bits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DPSRAM_HD is a dual-port synchronous static RAM which is provided as a compiler. DPSRAM_HD is intended for use in high-density applications. Each port is fully independent. On the rising edge of CK1(CK2), the write cycle is initiated when WEN1 (WEN2) is low and CSN1 (CSN2) is low. The data on DI1[] (DI2[]) is written into the memory location specified on A1[](A2[]). During the write cycle, DOUT1[] (DOUT2[]) remains stable. On the rising edge of CK, the read cycle is initiated when WEN1 (WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[] (DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[](A2[]) and DI1[] (DI2[]) are disabled, data stored in the memory is retained and DOUT1[] (DOUT2[]) remains stable. When OEN1 (OEN2) is high, DOUT1[] (DOUT2[]) is placed in a high-impedance state.

DPSRAM_HD Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

DPSRAM_HD

High-Density Dual-Port Synchronous Static RAM

Parameter Description

DPSRAM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	32	64	128	256
	Max	2048	4096	8192	16384
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode.
CSN1 CSN2	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [ ] A2 [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [ ] DI2 [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [ ] DOUT2 [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

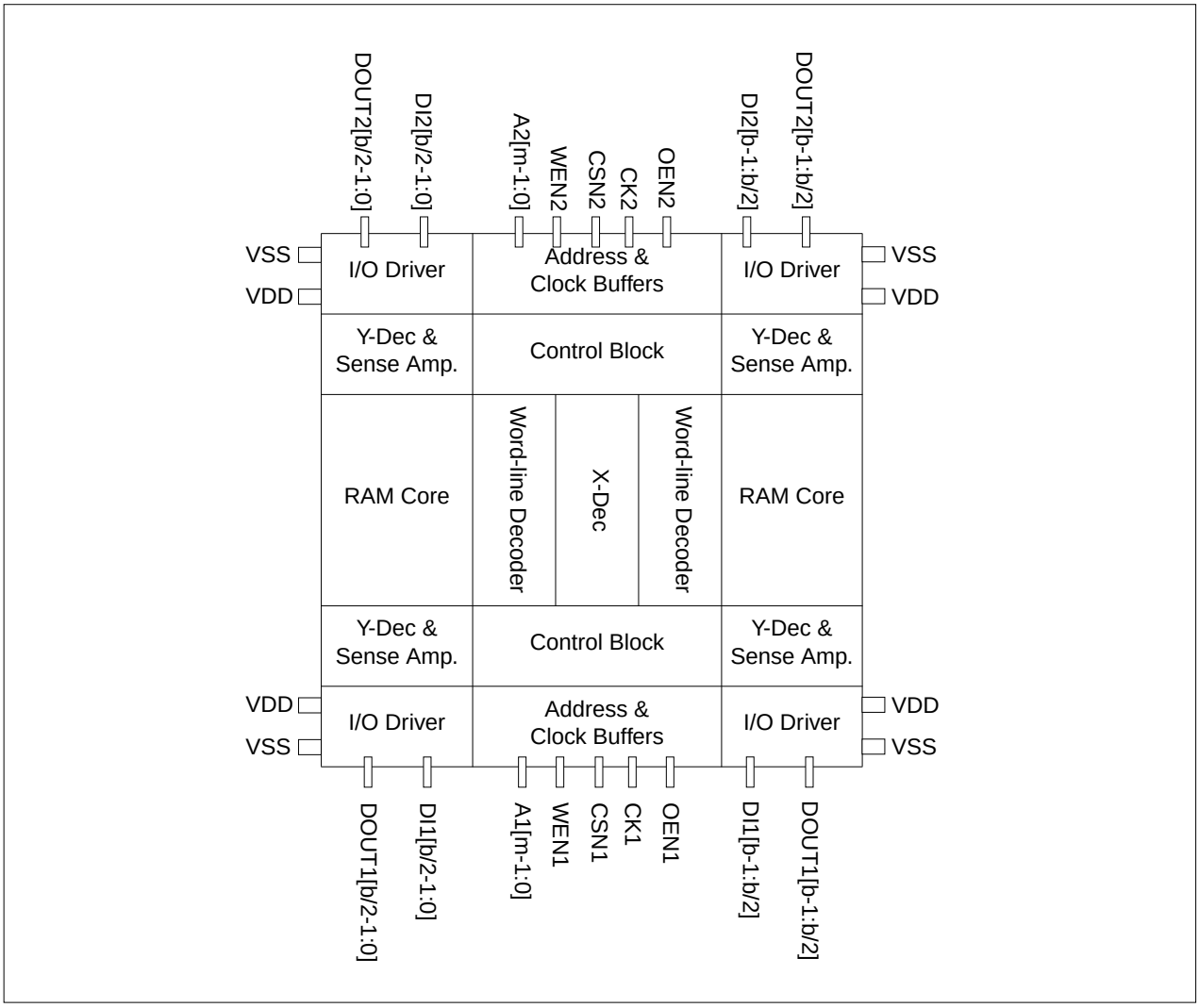
(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT
31.43	4.55	4.55	10.97	4.55	5.16	33.58

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagram

DPSRAM_HD supports only 1-bank architecture. The power ports are located on the top edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAM_HD has two symmetrical ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



Application Notes

1. Permitting over-the-cell routing
   In chip-level layout, over-the-cell routing in DPSRAM_HD is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAM_HD.

4. Contention mode in same address access
   In DPSRAM_HD, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAM_HD has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

5. Power reduction during standby mode.
   The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock-to-clock setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**128**	**256**	**512**	**768**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**	**80**	**96**	**112**	**128**
Timing (ns)								
t_{cyc}	1.79	1.84	1.91	2.03	2.15	2.28	2.44	2.52
t_{ckl}	0.66	0.64	0.61	0.58	0.61	0.60	0.59	0.60
t_{ckh}	0.27	0.27	0.27	0.27	0.28	0.28	0.28	0.28
t_{cc}	0.71	0.76	0.84	0.97	1.06	1.20	1.44	1.54
t_{as}	0.38	0.38	0.38	0.39	0.36	0.36	0.36	0.36
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.37	0.40	0.39	0.38	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.58	0.55	0.52	0.50	0.48	0.47	0.45	0.44
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.36	0.36	0.37	0.38	0.34	0.33	0.35	0.35
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.56	1.61	1.68	1.80	1.93	2.05	2.22	2.29
t_{da}	1.55	1.58	1.63	1.76	1.86	1.96	2.15	2.17
t_{dz}	0.42	0.45	0.48	0.51	0.52	0.55	0.58	0.60
t_{zd}	0.45	0.51	0.56	0.61	0.62	0.65	0.68	0.70
t_{od}	0.52	0.58	0.64	0.71	0.72	0.75	0.77	0.80
Power (µW/MHz)								
Power_read	86.57	145.15	206.80	275.22	352.35	428.99	522.52	602.97
Power_write	93.87	162.77	238.31	329.22	433.18	541.78	692.24	844.24
Power_standby	32.22	50.80	70.69	93.20	117.23	140.72	169.47	198.71
Area (µm)								
Width	548.20	893.80	1239.40	1585.00	2008.60	2354.20	2699.80	3045.40
Height	194.12	217.72	264.92	359.32	453.60	547.86	736.38	925.16

NOTES:

1. In power consumption of DPSRAM_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**256**	**512**	**1024**	**1536**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**	**40**	**48**	**56**	**64**
Timing (ns)								
t_{cyc}	1.81	1.85	1.92	2.05	2.17	2.29	2.48	2.54
t_{ckl}	0.69	0.66	0.63	0.61	0.61	0.59	0.60	0.56
t_{ckh}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.27
t_{cc}	0.72	0.77	0.85	0.97	1.07	1.20	1.45	1.52
t_{as}	0.40	0.39	0.38	0.38	0.38	0.38	0.36	0.36
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.57	0.54	0.52	0.49	0.49	0.47	0.46	0.45
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.35	0.35	0.35	0.36	0.36	0.36	0.37	0.37
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.58	1.62	1.69	1.82	1.94	2.06	2.26	2.31
t_{da}	1.56	1.59	1.64	1.78	1.87	1.97	2.17	2.18
t_{dz}	0.42	0.45	0.48	0.50	0.52	0.55	0.57	0.60
t_{zd}	0.45	0.50	0.55	0.60	0.62	0.65	0.67	0.70
t_{od}	0.52	0.58	0.64	0.70	0.72	0.75	0.77	0.79
Power (µW/MHz)								
Power_read	79.56	131.01	185.55	246.88	317.25	384.80	469.11	540.44
Power_write	80.16	134.69	194.05	264.44	345.51	427.28	538.42	644.00
Power_standby	27.67	41.76	57.15	75.12	94.56	113.48	137.79	162.28
Area (µm)								
Width	548.20	893.80	1239.40	1585.00	2008.60	2354.20	2699.80	3045.40
Height	194.12	217.72	264.92	359.32	453.60	547.86	736.38	925.16

NOTES:

1. In power consumption of DPSRAM_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DPSRAM_HD

High-Density Dual-Port Synchronous Static RAM

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**512**	**1024**	**2048**	**3072**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**	**20**	**24**	**28**	**32**
Timing (ns)								
t_{cyc}	1.81	1.87	1.96	2.10	2.19	2.32	2.51	2.58
t_{ckl}	0.68	0.66	0.63	0.61	0.61	0.61	0.60	0.60
t_{ckh}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{cc}	0.70	0.76	0.84	0.97	1.07	1.19	1.46	1.56
t_{as}	0.37	0.37	0.37	0.38	0.37	0.36	0.36	0.33
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.56	0.54	0.52	0.49	0.49	0.49	0.48	0.47
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.35	0.33	0.33	0.36	0.33	0.33	0.34	0.35
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.61	1.65	1.73	1.87	1.98	2.09	2.31	2.35
t_{da}	1.58	1.62	1.69	1.81	1.90	1.99	2.19	2.19
t_{dz}	0.42	0.45	0.47	0.50	0.52	0.54	0.57	0.59
t_{zd}	0.43	0.49	0.54	0.60	0.62	0.64	0.67	0.69
t_{od}	0.51	0.57	0.64	0.70	0.72	0.74	0.77	0.79
Power (µW/MHz)								
Power_read	76.17	123.87	174.58	231.92	298.86	362.11	442.21	509.19
Power_write	73.15	119.65	170.12	229.53	298.73	366.36	457.35	538.52
Power_standby	24.96	36.26	48.85	64.01	80.75	96.46	117.52	138.75
Area (µm)								
Width	548.20	893.80	1239.40	1585.00	2008.60	2354.20	2699.80	3045.40
Height	194.12	217.72	264.92	359.32	453.60	547.86	736.38	925.16

NOTES:

1. In power consumption of DPSRAM_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

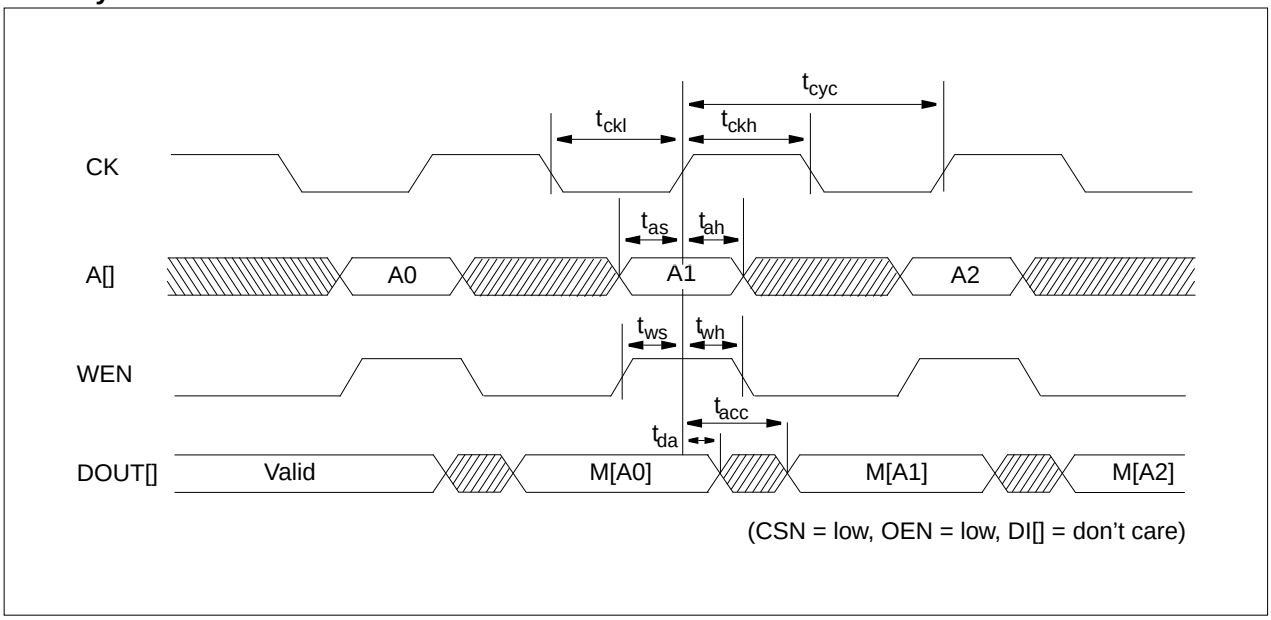
Parameters								
words	**512**	**1024**	**2048**	**4096**	**6144**	**8192**	**12288**	**16384**
bpw	**2**	**4**	**6**	**8**	**10**	**12**	**14**	**16**
Timing (ns)								
t_{cyc}	1.87	1.93	2.01	2.12	2.24	2.35	2.55	2.62
t_{ckl}	0.68	0.66	0.65	0.64	0.64	0.64	0.63	0.63
t_{ckh}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{cc}	0.69	0.75	0.84	0.98	1.06	1.20	1.46	1.53
t_{as}	0.37	0.37	0.37	0.38	0.37	0.36	0.34	0.34
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.56	0.54	0.53	0.52	0.52	0.52	0.51	0.51
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.28	0.30	0.33	0.36	0.36	0.37	0.37	0.38
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.63	1.68	1.76	1.89	2.02	2.13	2.33	2.38
t_{da}	1.62	1.64	1.70	1.85	1.96	2.05	2.24	2.25
t_{dz}	0.43	0.45	0.48	0.50	0.52	0.54	0.57	0.59
t_{zd}	0.53	0.54	0.56	0.60	0.62	0.64	0.67	0.69
t_{od}	0.63	0.64	0.65	0.70	0.72	0.74	0.77	0.79
Power (µW/MHz)								
Power_read	74.46	120.29	169.15	224.65	290.25	351.11	428.95	493.53
Power_write	70.27	112.47	158.24	212.03	275.64	335.98	416.64	485.50
Power_standby	26.63	33.47	44.60	58.31	73.82	87.94	107.34	127.04
Area (µm)								
Width	548.20	893.80	1239.40	1585.00	2008.60	2354.20	2699.80	3045.40
Height	194.12	217.72	264.92	359.32	453.60	547.86	736.38	925.16

NOTES:

1. In power consumption of DPSRAM_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

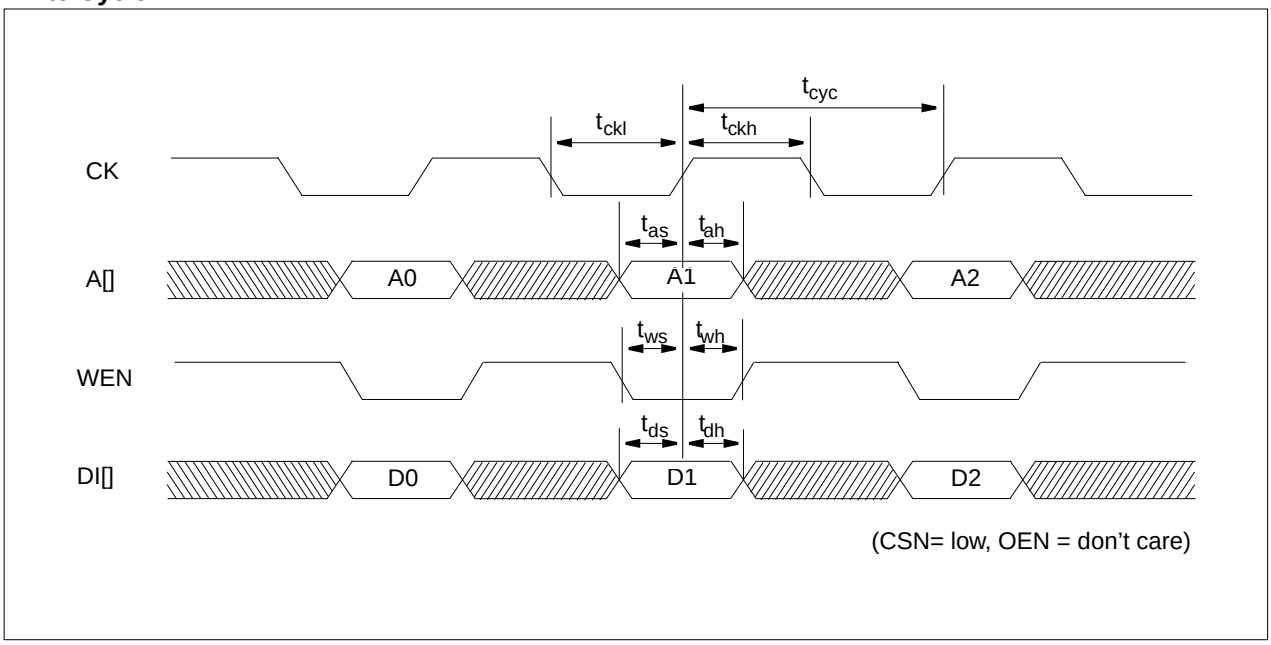
Timing Diagrams

Read Cycle



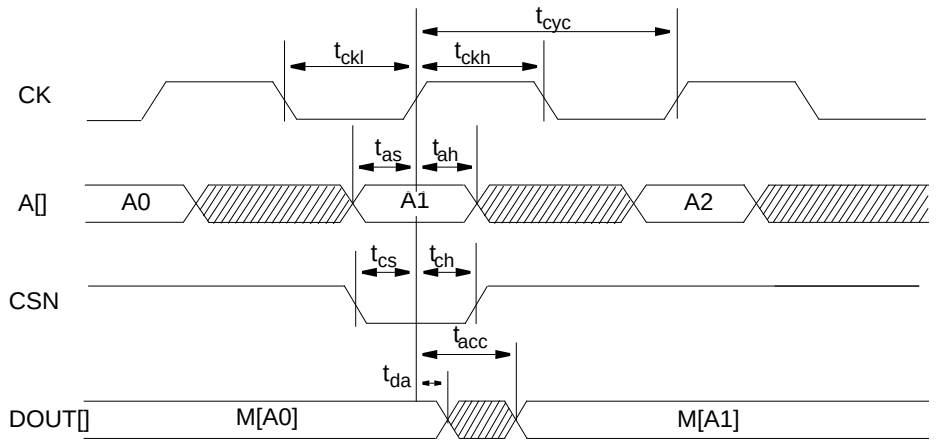
(CSN = low, OEN = low, DI[] = don't care)

Write Cycle



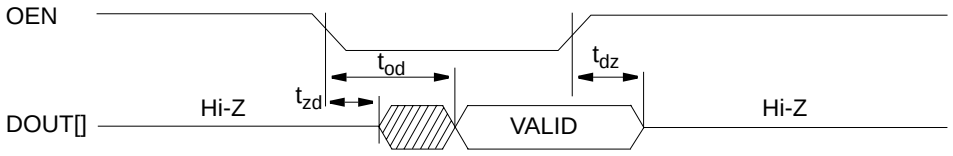
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



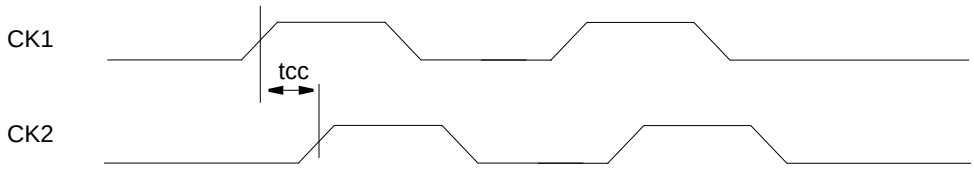
(OEN = low, WEN = high, DI[] = don't care)

OEN-Controlled Output Enable



(CSN, CK, A[], WEN, DI[] = don't care)

Contention Mode



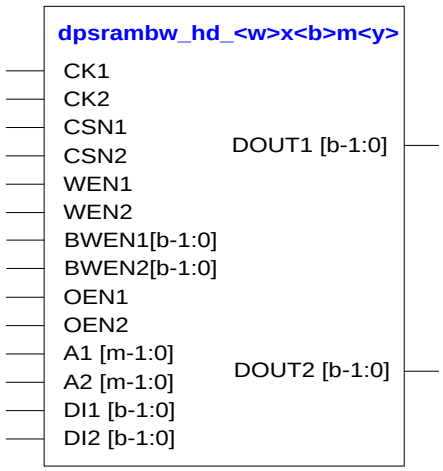
(A1[] = A2[])

NOTE: "don't care" means the condition that these pins are in normal operation mode.

DPSRAMBW_HD

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 256K bits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DPSRAMBW_HD is a dual-port synchronous static RAM with bit-write capability which is provided as a compiler. DPSRAMBW_HD is intended for use in high-density applications. Each port is fully independent. Basically, its functionality is exactly same as DPSRAM_HD except a bit-write operation which is controlled by BWEN1[](BWEN2[]), named bit-write enable signal bus. Each bit of BWEN1[](BWEN2[]) enables or disable the write operation of its corresponding bit in DI1[](DI2[]). On the rising edge of CK1(CK2), the write cycle is initiated when WEN1(WEN2) is low and CSN1(CSN2) is low. The data bits in DI1[](DI2[]), which their corresponding bit(s) in BWEN1[](BWEN2[]) are low, are written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEN2[]) are high, any data in DI1[](DI2[]) are not written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEM2[]) are low, the data in DI1[](DI2[]) are written into the memory location specified on A1[](A2[]), which is exactly same as the write operation in DPSRAMBW_HD. During the write cycle, DOUT1[](DOUT2[]) remains stable. On the rising edge of CK1(CK2), the read cycle is initiated when WEN1(WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[](DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[](A2[]) and DI1[](DI2[]) are disabled, data stored in the memory is retained and DOUT1[](DOUT2[]) remains stable. When OEN1(OEN2) is high, DOUT1[](DOUT2[]) is placed in a high-impedance state.

DPSRAMBW_HD Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	BWEN1 BWEN2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	All L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	All H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

Parameter Description

DPSRAMBW_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	32	64	128	256
	Max	2048	4096	8192	16384
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
BWEN1[ ] BWEN2[ ]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [ ] A2 [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [ ] DI2 [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [ ] DOUT2 [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT
31.43	4.55	4.55	10.97	4.55	5.16	5.16	33.58

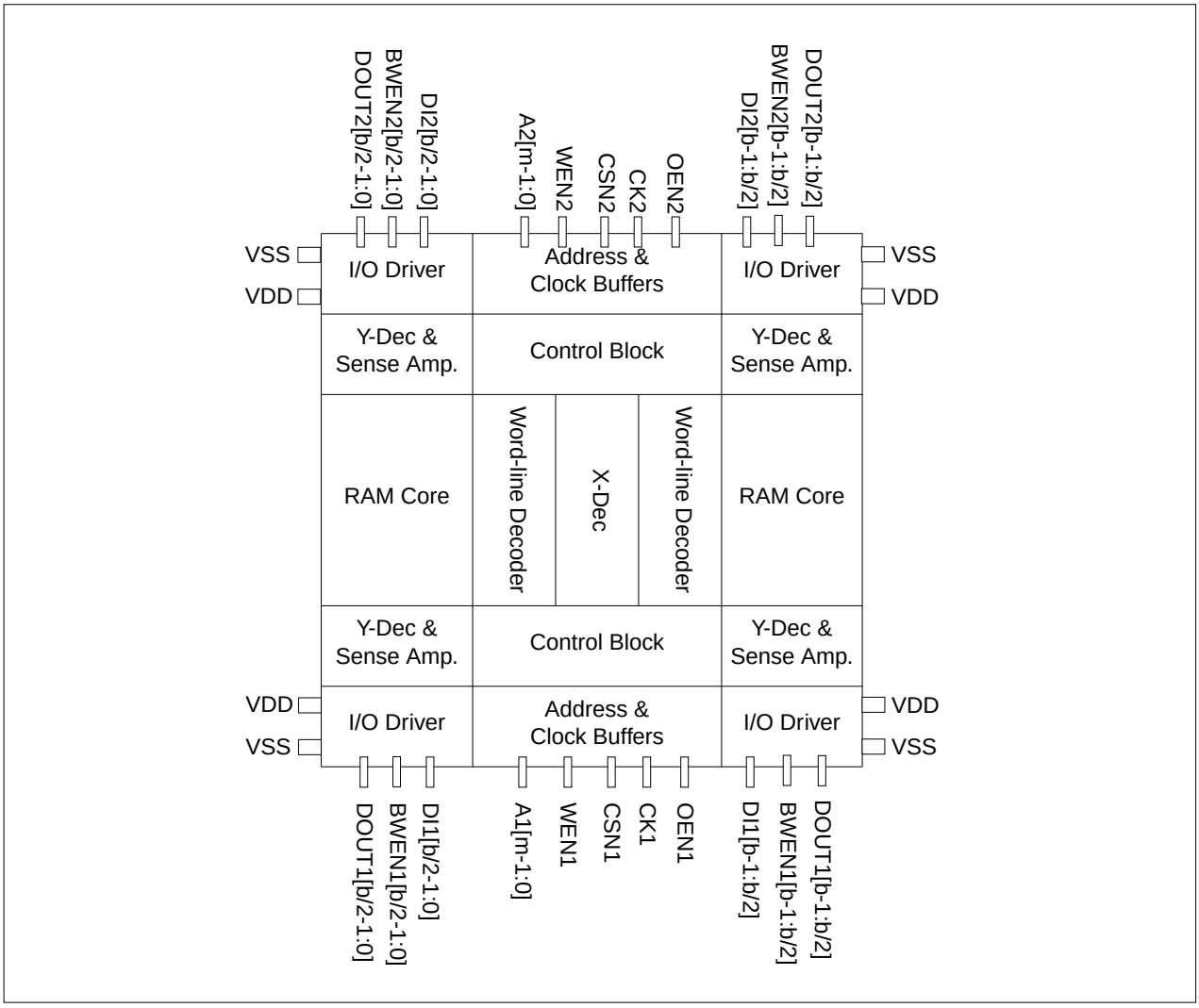
NOTE: Each pin's capacitance is exactly same regardless of available mux types.

DPSRAMBW_HD

High-Density Dual-Port Synchronous Static RAM Bit-Write

Block Diagram

DPSRAMBW_HD supports only 1-bank architecture. The power ports are located on the top edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAMBW_HD has two symmetrical ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



Application Notes

1. Permitting over-the-cell routing
In chip-level layout, over-the-cell routing in DPSRAMBW_HD is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAMBW_HD.

4. Contention mode in same address access
In DPSRAMBW_HD, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAMBW_HD has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

5. A byte-write or word-write operation with DPSRAMBW_HD
Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as DPSRAM_HD. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

6. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

DPSRAMBW_HD

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock-to-clock setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{bws}	BWEN setup time	t_{bwh}	BWEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (µW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations.		
Definition for Area (µm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**128**	**256**	**512**	**768**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**	**80**	**96**	**112**	**128**
Timing (ns)								
t_{cyc}	1.79	1.84	1.91	2.03	2.15	2.28	2.44	2.52
t_{ckl}	0.66	0.64	0.61	0.58	0.61	0.60	0.59	0.60
t_{ckh}	0.27	0.27	0.27	0.27	0.28	0.28	0.28	0.28
t_{cc}	0.71	0.76	0.84	0.97	1.06	1.20	1.44	1.54
t_{as}	0.38	0.38	0.38	0.39	0.36	0.36	0.36	0.36
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.37	0.40	0.39	0.38	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.58	0.55	0.52	0.50	0.48	0.47	0.45	0.44
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.36	0.36	0.37	0.38	0.34	0.33	0.35	0.35
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.55	0.52	0.50	0.47	0.44	0.42	0.39	0.36
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.56	1.61	1.68	1.80	1.93	2.05	2.22	2.29
t_{da}	1.55	1.58	1.63	1.76	1.86	1.96	2.15	2.17
t_{dz}	0.42	0.45	0.48	0.51	0.52	0.55	0.58	0.60
t_{zd}	0.45	0.51	0.56	0.61	0.62	0.65	0.68	0.70
t_{od}	0.52	0.58	0.64	0.71	0.72	0.75	0.77	0.80
Power (µW/MHz)								
Power_read	91.12	154.23	220.42	293.39	375.06	456.18	554.19	639.15
Power_write	98.41	171.85	251.94	347.39	455.89	568.97	723.90	880.42
Power_standby	36.77	59.89	84.32	111.37	139.94	167.91	201.14	234.89
Area (µm)								
Width	548.20	893.80	1239.40	1585.00	2008.60	2354.20	2699.80	3045.40
Height	194.12	217.72	264.92	359.32	453.60	547.86	736.38	925.16

NOTES:

1. In power consumption of DPSRAMBW_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DPSRAMBW_HD

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**256**	**512**	**1024**	**1536**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**	**40**	**48**	**56**	**64**
Timing (ns)								
t_{cyc}	1.81	1.85	1.92	2.05	2.17	2.29	2.48	2.54
t_{ckl}	0.69	0.66	0.63	0.61	0.61	0.59	0.60	0.56
t_{ckh}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.27
t_{cc}	0.72	0.77	0.85	0.97	1.07	1.20	1.45	1.52
t_{as}	0.40	0.39	0.38	0.38	0.38	0.38	0.36	0.36
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.57	0.54	0.52	0.49	0.49	0.47	0.46	0.45
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.35	0.35	0.35	0.36	0.36	0.37	0.37	0.37
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.54	0.52	0.49	0.46	0.45	0.42	0.40	0.37
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.58	1.62	1.69	1.82	1.94	2.06	2.26	2.31
t_{da}	1.56	1.59	1.64	1.78	1.87	1.97	1.17	2.18
t_{dz}	0.42	0.45	0.48	0.50	0.52	0.55	0.57	0.60
t_{zd}	0.45	0.50	0.55	0.60	0.62	0.65	0.67	0.70
t_{od}	0.52	0.58	0.64	0.70	0.72	0.75	0.77	0.79
Power (µW/MHz)								
Power_read	81.83	135.56	192.36	255.97	328.59	398.39	484.95	558.54
Power_write	82.44	139.23	200.86	273.53	356.85	440.87	554.26	662.10
Power_standby	29.94	46.31	63.97	84.21	105.90	127.07	153.63	180.38
Area (µm)								
Width	548.20	893.80	1239.40	1585.00	2008.60	2354.20	2699.80	3045.40
Height	194.12	217.72	264.92	359.32	453.60	547.86	736.38	925.16

NOTES:

1. In power consumption of DPSRAMBW_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**512**	**1024**	**2048**	**3072**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**	**20**	**24**	**28**	**32**
Timing (ns)								
t_{cyc}	1.81	1.87	1.96	2.10	2.19	2.32	2.51	2.58
t_{ckl}	0.68	0.66	0.63	0.61	0.61	0.61	0.60	0.60
t_{ckh}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{cc}	0.70	0.76	0.84	0.97	1.07	1.19	1.46	1.56
t_{as}	0.37	0.37	0.37	0.38	0.37	0.36	0.36	0.33
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.56	0.54	0.52	0.49	0.49	0.49	0.48	0.47
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.35	0.33	0.33	0.36	0.33	0.33	0.34	0.35
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.54	0.51	0.49	0.46	0.45	0.42	0.40	0.37
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.61	1.65	1.73	1.87	1.98	2.09	2.31	2.35
t_{da}	1.58	1.62	1.69	1.81	1.90	1.99	2.19	2.19
t_{dz}	0.42	0.45	0.47	0.50	0.52	0.54	0.57	0.59
t_{zd}	0.43	0.49	0.54	0.60	0.62	0.64	0.67	0.69
t_{od}	0.51	0.57	0.64	0.70	0.72	0.74	0.77	0.79
Power (µW/MHz)								
Power_read	77.31	126.14	177.99	236.46	304.40	368.91	450.15	518.24
Power_write	74.29	121.92	173.52	234.07	304.40	373.15	465.28	547.56
Power_standby	26.09	38.53	52.26	68.56	86.42	103.26	125.45	147.80
Area (µm)								
Width	548.20	893.80	1239.40	1585.00	2008.60	2354.20	2699.80	3045.40
Height	194.12	217.72	264.92	359.32	453.60	547.86	736.38	925.16

NOTES:

1. In power consumption of DPSRAMBW_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DPSRAMBW_HD

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

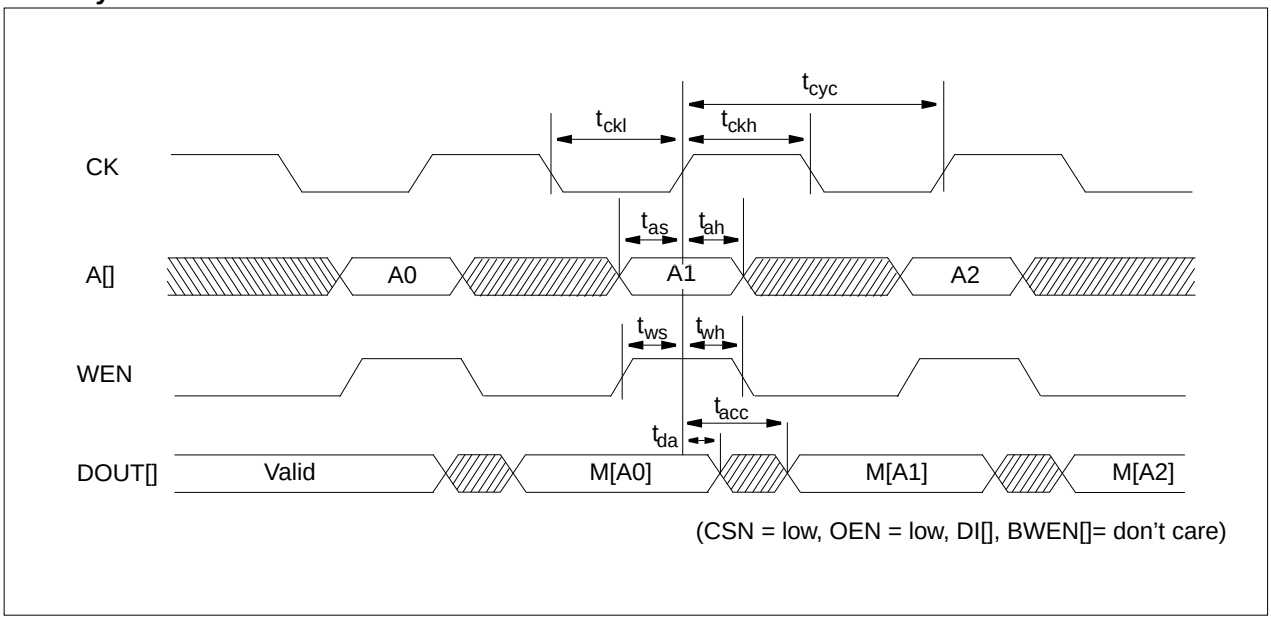
Parameters								
words	**512**	**1024**	**2048**	**4096**	**6144**	**8192**	**12288**	**16384**
bpw	**2**	**4**	**6**	**8**	**10**	**12**	**14**	**16**
Timing (ns)								
t_{cyc}	1.87	1.93	2.01	2.12	2.24	2.35	2.55	2.62
t_{ckl}	0.68	0.66	0.65	0.64	0.64	0.64	0.63	0.63
t_{ckh}	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
t_{cc}	0.69	0.75	0.84	0.98	1.06	1.20	1.46	1.53
t_{as}	0.37	0.37	0.37	0.38	0.37	0.36	0.34	0.34
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.56	0.54	0.53	0.52	0.52	0.52	0.51	0.51
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.28	0.30	0.33	0.36	0.36	0.37	0.37	0.38
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.55	0.52	0.49	0.46	0.44	0.42	0.40	0.37
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.63	1.68	1.76	1.89	2.02	2.13	2.33	2.38
t_{da}	1.62	1.64	1.70	1.85	1.96	2.05	2.24	2.25
t_{dz}	0.43	0.45	0.48	0.50	0.52	0.54	0.57	0.59
t_{zd}	0.53	0.54	0.56	0.60	0.62	0.64	0.67	0.69
t_{od}	0.63	0.64	0.65	0.70	0.72	0.74	0.77	0.79
Power (µW/MHz)								
Power_read	75.03	121.43	170.85	226.91	293.08	354.51	432.91	498.06
Power_write	70.84	113.61	159.95	214.30	278.48	339.39	420.60	490.03
Power_standby	24.20	34.61	46.31	60.58	76.65	91.34	111.30	131.56
Area (µm)								
Width	548.20	893.80	1239.40	1585.00	2008.60	2354.20	2699.80	3045.40
Height	194.12	217.72	264.92	359.32	453.60	547.86	736.38	925.16

NOTES:

1. In power consumption of DPSRAMBW_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

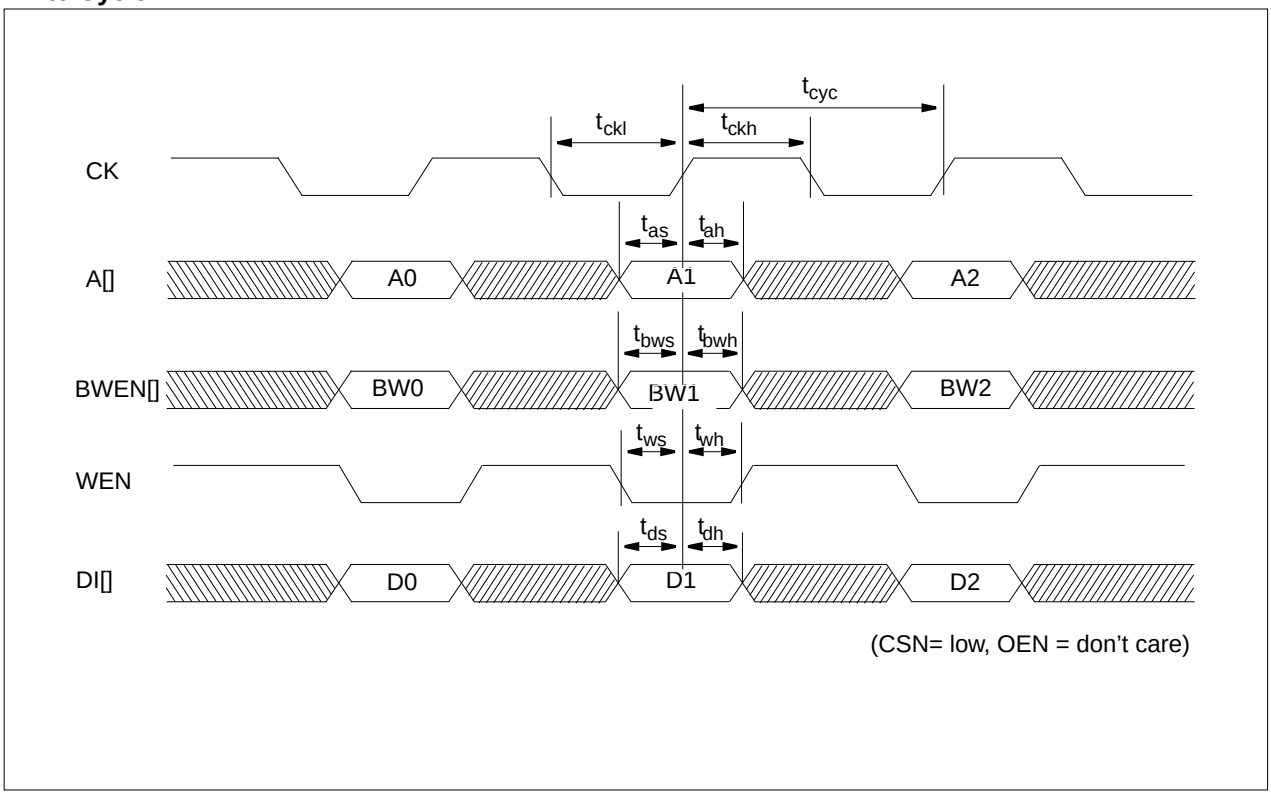
Timing Diagrams

Read Cycle



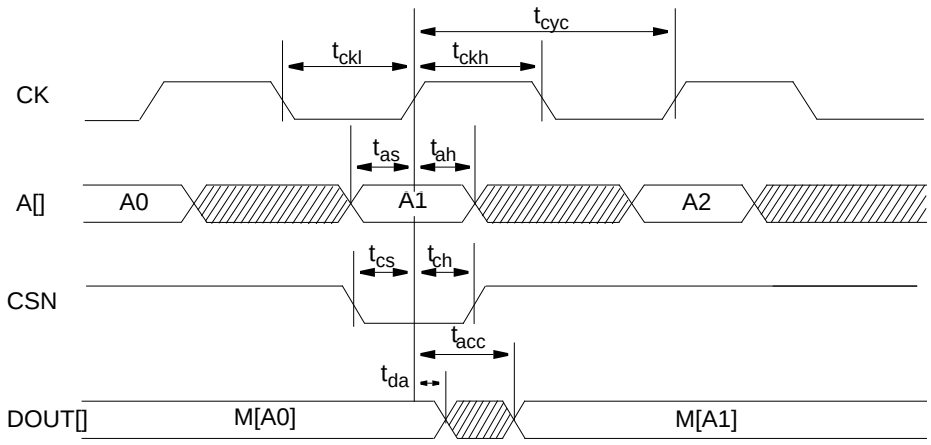
(CSN = low, OEN = low, DI[], BWEN[]= don't care)

Write Cycle



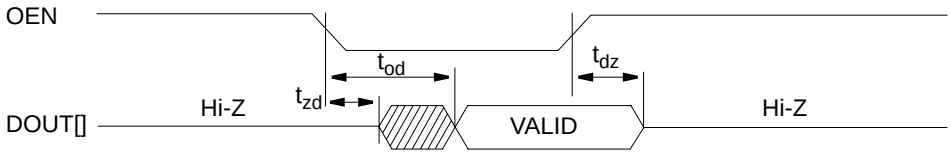
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



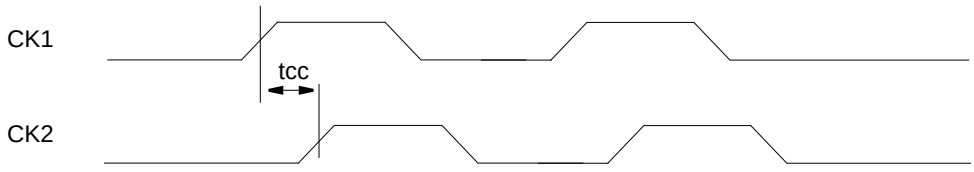
(OEN = low, WEN = high, DI[], BWEN[] = don't care)

OEN-Controlled Output Enable



(CSN, CK, A[], WEN, DI[], BWEN[] = don't care)

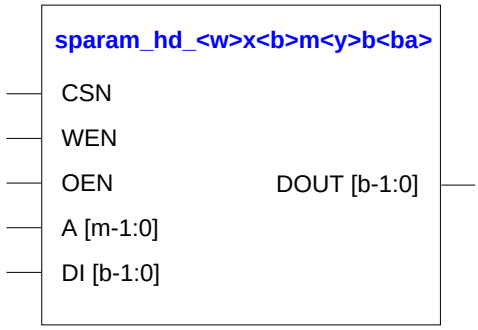
Contention Mode



(A1[] = A2[])

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Asynchronous operation
- Asynchronous tri-state output
- Address transition detector
- Write-enable transition detector
- Chip-select transition detector
- Bank-select transition detector
- Automatic power-down mode available
- Low noise output optimization
- Zero standby current
- Zero hold time for DI
- Flexible aspect ratio
- Dual bank scheme available
- Up to 512K bits capacity
- Up to 32K number of words
- Up to 128 number of bit per word

Function Description

SPARAM_HD is a single-port asynchronous static RAM which is provided as a compiler. SPARAM_HD is intended for use in high-density applications. At the falling edge of WEN, the write cycle is initiated. At the rising edge of WEN, the write cycle is ended. During the write cycle, the data on DI[] is written into the memory location specified on A[]. The read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay whenever A[] transition is detected. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPARAM_HD Function Table

CSN	WEN	OEN	A	DI	DOUT	Comment
X	X	H	X	X	Z	Unconditional tri-state output
H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
L	↓	L	Valid	Valid	DOUT(t-1)	Write cycle starts
L	↑	L	Valid	Valid	MEM(A)	Write cycle ends and read cycle starts
L	L	L	Stable	Valid	DOUT(t-1)	Write cycle
L	H	L	Toggle	X	MEM(A)	Read cycle

SPARAM_HD

High-Density Single-Port Asynchronous Static RAM

Parameter Description

SPARAM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux = 4	Ymux = 8	Ymux = 16	Ymux = 32
Words(w)	ba = 1	Min	64	128	256	512
		Max	2048	4096	8192	16384
		Step	16	32	64	128
	ba = 2	Min	128	256	512	1024
		Max	4096	8192	16384	32768
		Step	32	64	128	256
Bpw(b)		Min	1	1	1	1
		Max	128	64	32	16
		Step	1	1	1	1

Pin Descriptions

Name	I/O	Description
CSN	Chip Enable	Chip select input. The chip select signal acts as the memory enable signal for selections of multiple blocks. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if low, a read or write access can occur. When CSN falls, an access is initiated.
WEN	Read/Write Enable	Write enable input. The write enable signal selects the type of memory access. The high state for a read access and the low state for a write access. Upon the rising edge of WEN, a write access completed and a read access initiated.
OEN	Data Output Enable	Output enable input. The output enable signal controls the output drivers from driven to tri-state condition unconditionally.
A [ ]	Address	Address input bus. A[] should be stable when WEN is low. The address selects the location to be accessed. When the address changes, the transition is detected and the internal clock pulse is generated.
DI [ ]	Data Input	Data input bus. The data input is written to the accessed location when WEN is low.
DOUT [ ]	Data Output	Data output bus. The data output is data stored in the accessed location during a read access. Data output driver has tri-state logic. When OEN is low, the driver drives a certain value. Otherwise, data output keeps Hi-Z state. During a write access, data on DOUT is predictable.

Pin Capacitance

Unit: [SL]

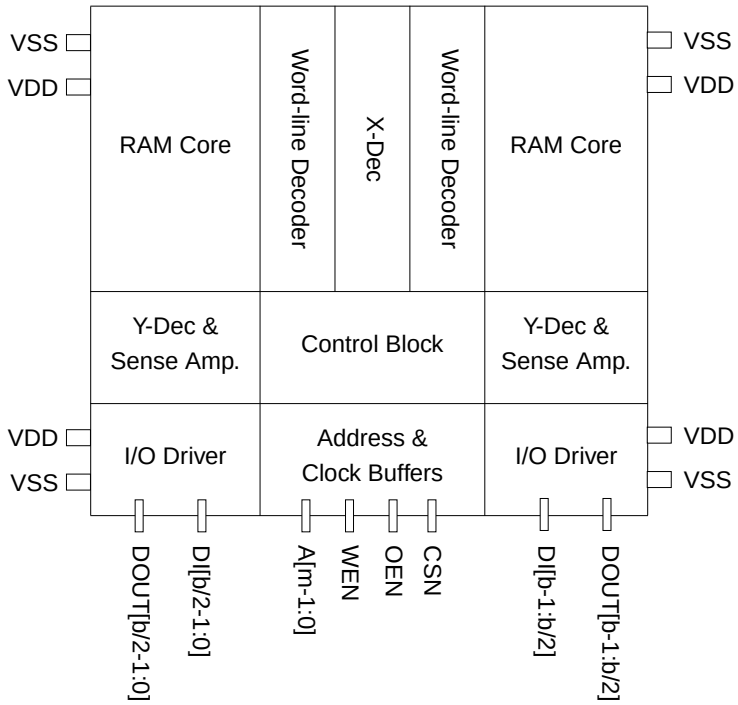
CSN	WEN	OEN	A	DI	DOUT
4.1567	3.9632	3.9632	3.9632	3.1644	16.5880

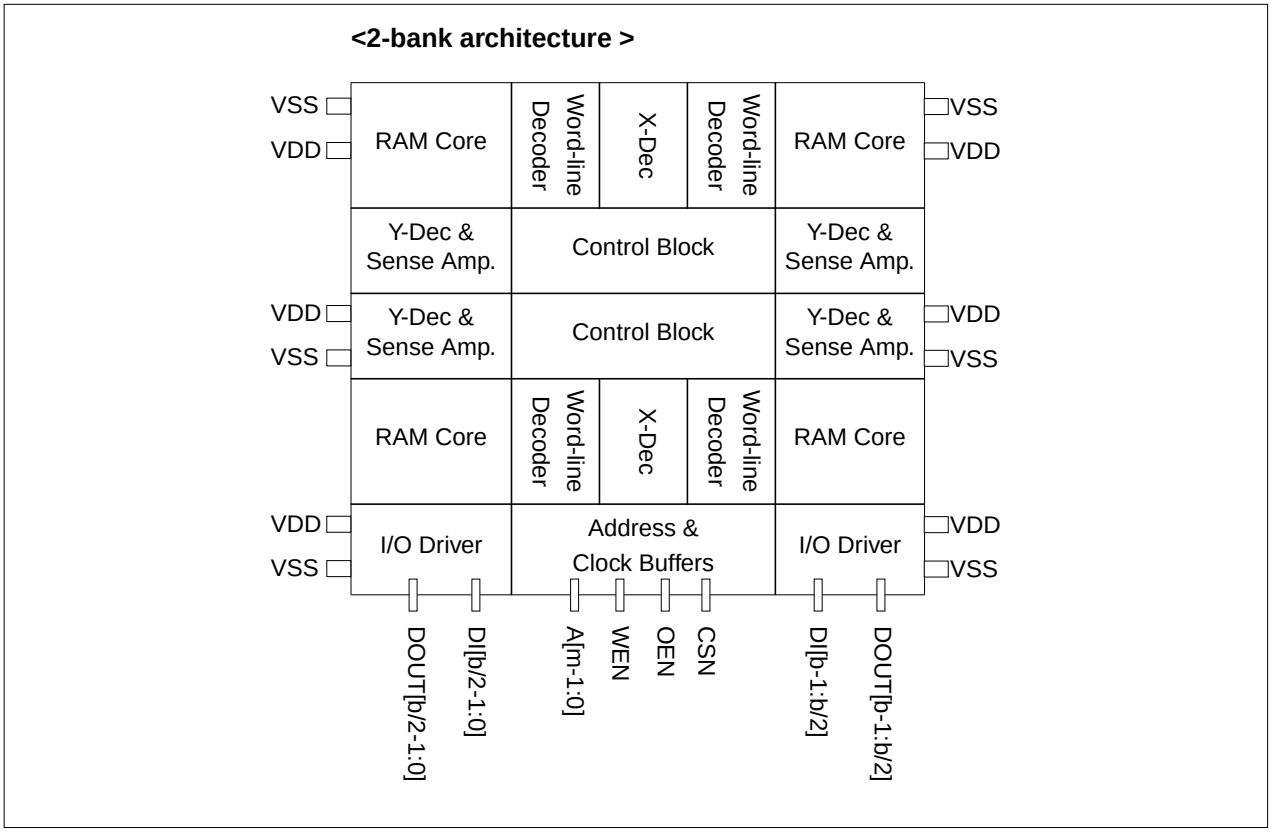
NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

Block Diagrams

SPARAM_HD has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPARAM_HD compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the top edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the top-edge, the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>





Application Notes

1. Permitting over-the-cell routing
   In chip-level layout, over-the-cell routing in SPARAM_HD is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPARAM_HD.

4. Avoiding short transition on the address bus
   In SPARAM_HD, rather than the write operation which is synchronously performed by WEN signal, the read operation is asynchronously performed whenever the address transition is occurred. In this case, if the short transition on the address, called a skew, is happened, since SPARAM_HD recognizes the short address transition as the stable address transition and do perform a read operation. At that time, while in the read operation, the data stored in the memory may be corrupted due to the short transition. To prevent such fail, the stable address cycle time (tcyc) is required. The essential requirement to recognize valid address transition is that at least minimum address period should be equal or greater than tacc (access time).

5. Power reduction during standby mode.
   The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Address cycle time	t_{as}	Address setup time
t_{cas}	Address setup time for CSN rise	t_{ah}	Address hold time
t_{wh}	WEN hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{wen}	WEN pulse width low
t_{acc}	Data access time for read cycle	t_{wacc}	Data access time for WEN rise
t_{da}	De-access time	t_{wda}	De-access time for WEN rise
t_{zd}	DOUT high-Z to drive time	t_{dz}	DOUT drive to high-Z time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**256**	**256**	**512**	**512**	**768**	**768**
bpw	**32**	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.53	2.55	2.60	2.60	2.69	2.67	2.79	2.75
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	2.71	2.73	2.78	2.78	2.87	2.85	2.97	2.93
t_{ah}	0.39	0.38	0.45	0.42	0.56	0.49	0.68	0.57
t_{wh}	2.71	2.73	2.78	2.78	2.87	2.85	2.97	2.93
t_{ds}	0.31	0.29	0.33	0.30	0.37	0.32	0.43	0.34
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.04	1.09	1.06	1.11	1.08	1.14	1.11	1.17
t_{wen}	1.67	1.67	1.70	1.69	1.77	1.73	1.85	1.78
t_{acc}	2.53	2.55	2.60	2.60	2.69	2.67	2.79	2.75
t_{da}	2.25	2.28	2.32	2.33	2.41	2.40	2.51	2.48
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.86	0.91	0.88	0.94	0.90	0.96	0.93	0.99
t_{dz}	0.38	0.38	0.41	0.41	0.44	0.44	0.47	0.47
t_{zd}	0.26	0.26	0.30	0.30	0.33	0.33	0.36	0.36
t_{od}	0.44	0.45	0.48	0.48	0.51	0.51	0.55	0.55
Power (µW/MHz)								
Power_read	98.59	96.80	135.96	131.05	181.51	169.54	234.70	214.91
Power_write	138.80	133.21	211.54	193.33	322.35	273.68	455.01	370.13
Power_standby	18.06	37.68	25.68	53.16	34.24	70.38	42.69	88.86
Area (µm)								
Width	574.72	654.20	773.00	895.36	971.28	1136.52	1166.42	1374.54
Height	203.34	337.54	250.50	384.70	344.82	479.02	439.14	573.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parametersy							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.90	2.83	3.06	2.95	3.23	3.06	3.36
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	3.07	3.01	3.24	3.13	3.41	3.24	3.54
t_{ah}	0.80	0.65	1.01	0.77	1.22	0.89	1.24
t_{wh}	3.07	3.01	3.24	3.13	3.41	3.24	3.54
t_{ds}	0.48	0.36	0.60	0.42	0.72	0.47	0.73
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.13	1.20	1.16	1.24	1.18	1.28	1.35
t_{wen}	1.93	1.83	2.09	1.91	2.25	1.99	2.35
t_{acc}	2.90	2.83	3.06	2.95	3.23	3.06	3.36
t_{da}	2.62	2.56	2.78	2.68	2.95	2.79	3.09
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.95	1.02	0.98	1.06	1.00	1.10	1.17
t_{dz}	0.50	0.50	0.53	0.53	0.56	0.56	0.56
t_{zd}	0.40	0.40	0.44	0.43	0.47	0.47	0.47
t_{od}	0.58	0.59	0.62	0.62	0.66	0.65	0.66
Power (µW/MHz)							
Power_read	291.21	262.07	369.21	319.11	454.12	379.47	458.92
Power_write	605.25	478.95	839.12	639.83	1113.90	823.84	1139.20
Power_standby	51.16	107.74	60.97	129.61	70.78	152.40	179.14
Area (µm)							
Width	1361.57	1612.56	1556.71	1850.58	1751.85	2088.61	2094.89
Height	533.46	667.66	722.10	856.30	910.74	1044.94	1799.50

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**512**	**512**	**1024**	**1024**	**1536**	**1536**
bpw	**16**	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.52	2.54	2.58	2.59	2.67	2.65	2.76	2.72
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	2.70	2.72	2.76	2.76	2.85	2.83	2.94	2.90
t_{ah}	0.40	0.39	0.47	0.44	0.57	0.50	0.70	0.59
t_{wh}	2.70	2.72	2.76	2.76	2.85	2.83	2.94	2.90
t_{ds}	0.34	0.32	0.35	0.32	0.40	0.34	0.46	0.37
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.03	1.08	1.04	1.09	1.06	1.11	1.07	1.14
t_{wen}	1.69	1.70	1.73	1.71	1.80	1.75	1.88	1.80
t_{acc}	2.52	2.54	2.58	2.59	2.67	2.65	2.76	2.72
t_{da}	2.24	2.27	2.30	2.32	2.39	2.38	2.48	2.45
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.85	0.90	0.87	0.92	0.88	0.94	0.90	0.96
t_{dz}	0.36	0.36	0.38	0.38	0.40	0.40	0.42	0.42
t_{zd}	0.24	0.24	0.27	0.27	0.29	0.29	0.32	0.31
t_{od}	0.43	0.43	0.45	0.45	0.47	0.47	0.50	0.50
Power (µW/MHz)								
Power_read	88.29	86.52	120.24	115.36	160.31	148.42	207.54	187.78
Power_write	118.03	112.98	177.51	161.55	269.46	226.92	382.03	305.64
Power_standby	12.26	25.48	16.87	34.45	22.44	44.89	27.63	55.88
Area (µm)								
Width	574.72	611.32	773.00	831.04	971.28	1050.76	1166.42	1267.34
Height	203.34	337.54	250.50	384.70	344.82	479.02	439.14	573.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.86	2.79	3.01	2.90	3.17	3.00	3.30
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	3.03	2.97	3.19	3.07	3.35	3.18	3.48
t_{ah}	0.82	0.67	1.03	0.79	1.24	0.91	1.27
t_{wh}	3.03	2.97	3.19	3.07	3.35	3.18	3.48
t_{ds}	0.51	0.39	0.63	0.44	0.75	0.50	0.76
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.09	1.16	1.10	1.19	1.12	1.22	1.29
t_{wen}	1.96	1.84	2.12	1.93	2.28	2.02	2.37
t_{acc}	2.86	2.79	3.01	2.90	3.17	3.00	3.30
t_{da}	2.57	2.52	2.73	2.63	2.89	2.73	3.03
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.91	0.98	0.93	1.01	0.94	1.04	1.11
t_{dz}	0.45	0.45	0.47	0.47	0.49	0.49	0.49
t_{zd}	0.34	0.34	0.36	0.37	0.39	0.39	0.39
t_{od}	0.52	0.52	0.55	0.55	0.57	0.57	0.57
Power (µW/MHz)							
Power_read	258.12	228.88	330.17	279.98	409.15	334.43	414.11
Power_write	513.46	396.11	707.38	528.54	931.41	681.49	944.44
Power_standby	32.84	67.11	39.39	80.35	45.96	94.07	114.26
Area (µm)							
Width	1361.57	1483.92	1556.71	1700.50	1751.85	1917.09	1923.37
Height	533.46	667.66	722.10	856.30	910.74	1044.94	1799.50

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**1024**	**1024**	**2048**	**2048**	**3072**	**3072**
bpw	**8**	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.52	2.56	2.60	2.61	2.68	2.67	2.78	2.74
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	2.71	2.74	2.77	2.79	2.86	2.85	2.95	2.92
t_{ah}	0.40	0.39	0.47	0.44	0.57	0.50	0.70	0.59
t_{wh}	2.71	2.74	2.77	2.79	2.86	2.85	2.95	2.92
t_{ds}	0.35	0.35	0.37	0.35	0.41	0.37	0.47	0.39
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.04	1.10	1.06	1.12	1.07	1.14	1.09	1.16
t_{wen}	1.71	1.72	1.74	1.74	1.81	1.78	1.89	1.83
t_{acc}	2.54	2.56	2.60	2.61	2.68	2.67	2.78	2.74
t_{da}	2.26	2.29	2.32	2.34	2.40	2.40	2.50	2.47
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.87	0.92	0.88	0.94	0.89	0.96	0.91	0.98
t_{dz}	0.36	0.36	0.38	0.38	0.40	0.40	0.42	0.42
t_{zd}	0.24	0.24	0.27	0.27	0.29	0.29	0.32	0.32
t_{od}	0.43	0.43	0.45	0.45	0.47	0.47	0.50	0.50
Power (µW/MHz)								
Power_read	84.60	82.81	114.65	109.77	152.82	140.94	198.11	178.35
Power_write	105.74	100.94	157.78	141.64	239.54	198.20	340.56	269.54
Power_standby	12.26	20.23	13.15	26.49	17.45	34.06	21.36	41.97
Area (µm)								
Width	574.72	589.88	773.00	789.88	971.28	1007.88	1166.42	1213.74
Height	203.34	337.54	250.50	384.70	344.82	479.02	439.14	573.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.87	2.81	3.03	2.92	3.18	3.03	3.32
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	3.05	2.99	3.20	3.10	3.36	3.20	3.50
t_{ah}	0.82	0.67	1.03	0.79	1.24	0.91	1.27
t_{wh}	3.05	2.99	3.20	3.10	3.36	3.20	3.50
t_{ds}	0.52	0.42	0.64	0.47	0.76	0.53	0.79
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.10	1.18	1.12	1.21	1.13	1.24	1.31
t_{wen}	1.97	1.87	2.13	1.96	2.30	2.05	2.40
t_{acc}	2.87	2.81	3.03	2.92	3.18	3.03	3.32
t_{da}	2.59	2.54	2.75	2.65	2.91	2.76	3.05
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.93	1.00	0.94	1.04	0.96	1.07	1.13
t_{dz}	0.45	0.45	0.47	0.47	0.49	0.49	0.49
t_{zd}	0.34	0.34	0.36	0.36	0.39	0.39	0.39
t_{od}	0.52	0.52	0.55	0.55	0.57	0.57	0.57
Power (µW/MHz)							
Power_read	246.74	217.48	316.91	266.62	394.04	319.12	399.09
Power_write	458.86	349.81	634.87	468.92	838.44	605.40	845.82
Power_standby	25.27	50.03	39.39	59.60	35.75	69.43	86.31
Area (µm)							
Width	1361.57	1419.60	1556.71	1625.46	1751.85	1831.33	1837.61
Height	533.46	667.66	722.10	856.30	910.74	1044.94	1799.50

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**1024**	**1024**	**2048**	**2048**	**4096**	**4096**	**6144**	**6144**
bpw	**4**	**4**	**6**	**6**	**8**	**8**	**10**	**10**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.56	2.60	2.62	2.65	2.71	2.71	2.80	2.78
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	2.74	2.78	2.80	2.83	2.88	2.89	2.98	2.96
t_{ah}	0.40	0.39	0.47	0.44	0.57	0.50	0.70	0.59
t_{wh}	2.74	2.78	2.80	2.83	2.88	2.89	2.98	2.96
t_{ds}	0.37	0.39	0.39	0.40	0.44	0.42	0.49	0.45
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.07	1.14	1.08	1.16	1.09	1.18	1.11	1.20
t_{wen}	1.74	1.77	1.77	1.79	1.84	1.83	1.92	1.88
t_{acc}	2.56	2.60	2.62	2.65	2.71	2.71	2.80	2.78
t_{da}	2.28	2.34	2.34	2.38	2.43	2.45	2.52	2.52
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.89	0.96	0.90	0.98	0.92	1.00	0.93	1.02
t_{dz}	0.36	0.36	0.38	0.38	0.40	0.40	0.42	0.42
t_{zd}	0.24	0.24	0.27	0.27	0.29	0.29	0.32	0.32
t_{od}	0.43	0.43	0.45	0.45	0.47	0.47	0.50	0.50
Power (µW/MHz)								
Power_read	82.70	80.93	111.84	106.98	149.12	137.24	193.44	173.68
Power_write	99.72	95.05	147.99	133.66	224.67	186.56	319.08	252.24
Power_standby	8.52	17.56	11.27	22.49	14.99	28.65	18.23	35.05
Area (µm)								
Width	574.72	579.16	773.00	782.80	971.28	986.44	1166.42	1186.94
Height	203.34	337.54	250.50	384.70	344.82	479.02	439.14	573.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

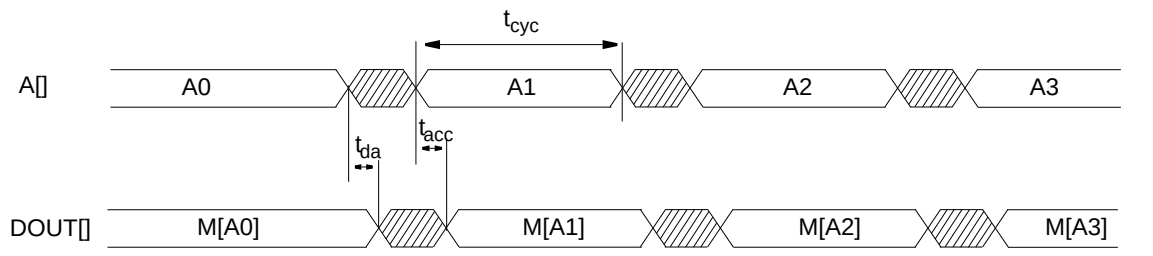
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**8192**	**8192**	**12288**	**12288**	**16384**	**16384**	**32768**
bpw	**12**	**12**	**14**	**14**	**16**	**16**	**16**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.89	2.85	3.05	2.96	3.21	3.07	3.36
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	3.07	3.03	3.23	3.14	3.39	3.25	3.54
t_{ah}	0.82	0.67	1.03	0.79	1.24	0.91	1.27
t_{wh}	3.07	3.03	3.23	3.14	3.39	3.25	3.54
t_{ds}	0.55	0.47	0.66	0.53	0.78	0.58	0.86
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.13	1.22	1.14	1.25	1.16	1.29	1.35
t_{wen}	2.00	1.93	2.16	2.01	2.33	2.11	2.47
t_{acc}	2.89	2.85	3.05	2.96	3.21	3.07	3.36
t_{da}	2.61	2.59	2.77	2.69	2.93	2.80	3.10
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.95	1.05	0.97	1.08	0.98	1.11	1.17
t_{dz}	0.45	0.45	0.47	0.47	0.49	0.49	0.49
t_{zd}	0.34	0.34	0.36	0.36	0.39	0.39	0.39
t_{od}	0.52	0.52	0.55	0.55	0.58	0.57	0.57
Power (µW/MHz)							
Power_read	241.13	211.86	310.37	260.07	386.58	311.66	391.66
Power_write	430.44	326.80	598.39	438.96	792.18	567.63	796.75
Power_standby	21.50	41.55	26.10	49.32	30.74	57.24	72.46
Area (µm)							
Width	1361.57	1387.44	1556.71	1587.94	1751.85	1788.45	1794.73
Height	533.46	667.66	722.10	856.30	910.74	1044.94	1799.50

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

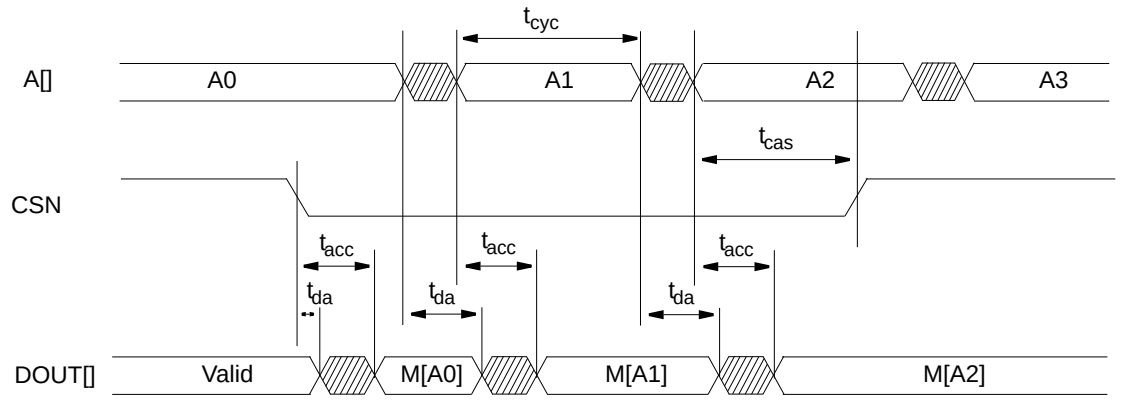
Timing Diagrams

Read Cycle



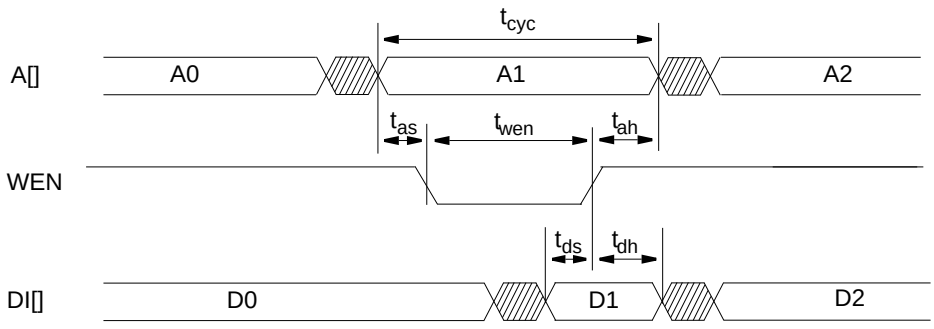
(WEN = high, CSN = low, OEN = low, DI[] = don't care)

Read Cycle with CSN-Controlled



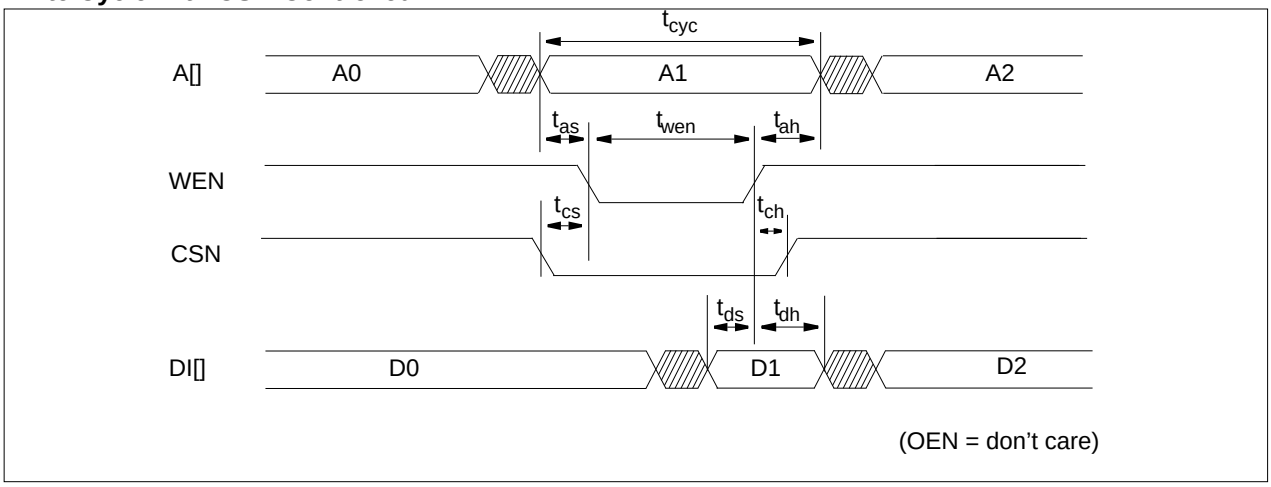
(OEN = low, WEN = high, DI[] = don't care)

Basic Write Cycle

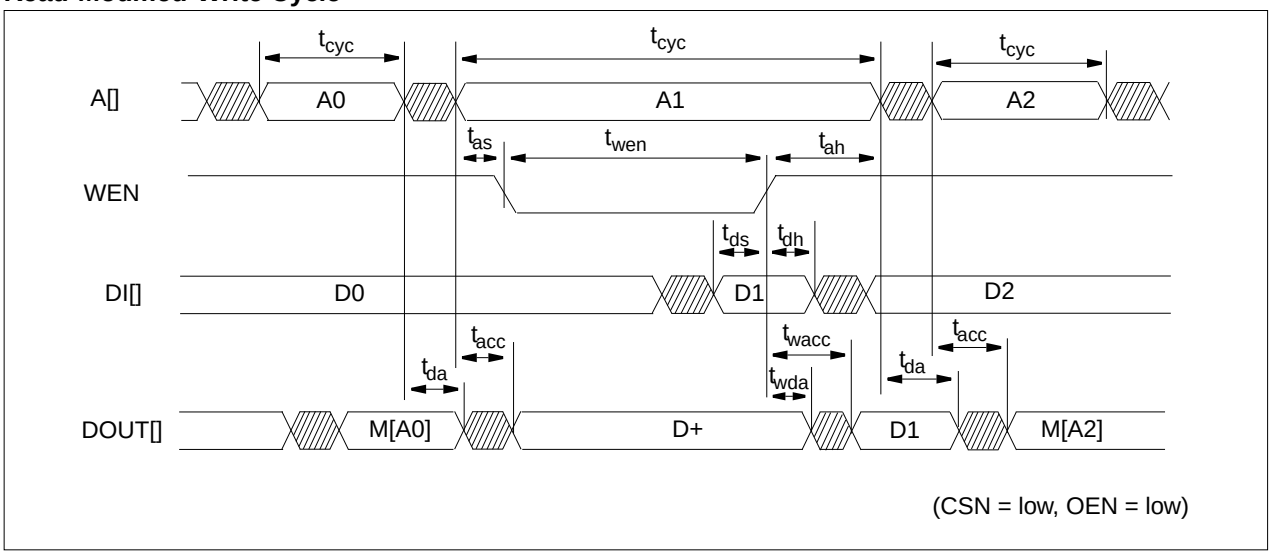


(CSN = low, OEN = don't care)

Write Cycle with CSN-Controlled



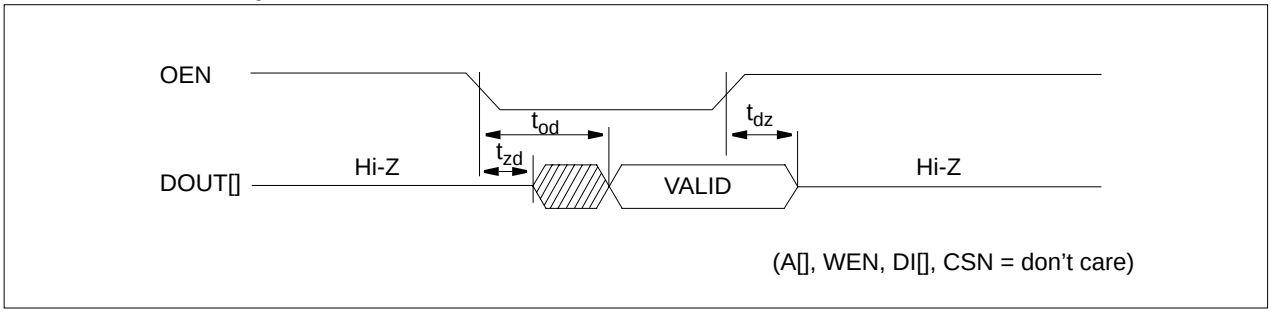
Read-Modified-Write Cycle



NOTES:

1. When the WEN hold time after the last address bit transition is satisfied, D+ will toggle in response to a successful read of the initial contents of address A1. When the WEN hold time after the last address bit transition is not satisfied, D+ will go to unknown state.
2. Address bits are not allowed to change while WEN is low. If they do change, then the data for one or more addresses in the memory array may be corrupted.

OEN Controlled Output Enable

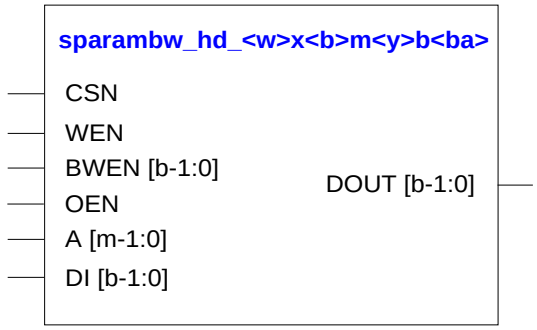


NOTE: "don't care" means the condition that these pins are in normal operation mode.

SPARAMBW_HD

High-Density Single-Port Asynchronous Static RAM with Bit-Write

Logic Symbol



NOTES:
1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Bit-Write capability
- Separated data I/O
- Asynchronous operation
- Asynchronous tri-state output
- Address transition detector
- Write-enable transition detector
- Chip-select transition detector
- Bank-select transition detector
- Automatic power-down mode available
- Low noise output optimization
- Zero standby current
- Zero hold time for DI and BWEN
- Flexible aspect ratio
- Dual bank scheme available
- Up to 512K bits capacity
- Up to 32K number of words
- Up to 128 number of bit per word

Function Description

SPARAMBW_HD is a single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPARAMBW_HD is intended for use in high-density applications. Basically, its functionality is exactly same as SPARAM_HD except a bit-write operation which is controlled by BWEN[], named bit-write enable signal bus. Each bit of BWEN[] enables or disable the write operation of its corresponding bit in DI[]. At the falling edge of WEN, the write cycle is initiated when CSN is low. The data bytes or bits in DI[], which their corresponding bit(s) in BWEN[] are low, are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPARAM_HD. At the rising edge of WEN, th write cycle is ended. The read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay whenever A[] transition is detected. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPARAMBW_HD Function Table

CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	H	X	X	X	Z	Unconditional tri-state output
H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
L	↓	L	Valid	All L	Valid	DOUT(t-1)	Word-write cycle starts
L	↓	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle starts
L	↑	L	Valid	All L	Valid	MEM(A)	Word-write cycle ends and Read cycle starts
L	↑	L	Valid	L	Valid	MEM(A)	Bit-write cycle ends and Read cycle starts
L	L	L	Stable	All L	Valid	DOUT(t-1)	Word-write cycle
L	L	L	Stable	L	Valid	DOUT(t-1)	Bit-write cycle
L	H	L	Toggle	X	X	MEM(A)	Read cycle

Parameter Description

SPARAMBW_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux = 4	Ymux = 8	Ymux = 16	Ymux = 32
Words(w)	ba = 1	Min	64	128	256	512
		Max	2048	4096	8192	16384
		Step	16	32	64	128
	ba = 2	Min	128	256	512	1024
		Max	4096	8192	16384	32768
		Step	32	64	128	256
Bpw(b)		Min	1	1	1	1
		Max	128	64	32	16
		Step	1	1	1	1

Pin Descriptions

Name	I/O	Description
CSN	Chip Enable	Chip select input. The chip select signal acts as the memory enable signal for selections of multiple blocks. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if low, a read or write access can occur. When CSN falls, an access is initiated.
WEN	Read/Write Enable	Write enable input. The write enable signal selects the type of memory access. The high state for a read access and the low state for a write access. Upon the rising edge of WEN, a write access completed and a read access initiated.
BWEN[ ]	Bit-Write Enable	Bit-write enable input bus. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. IF WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Output enable input. The output enable signal controls the output drivers from driven to tri-state condition unconditionally.
A [ ]	Address	Address input bus. A[] should be stable when WEN is low. The address selects the location to be accessed. When the address changes, the transition is detected and the internal clock pulse is generated.
DI [ ]	Data Input	Data input bus. The data input is written to the accessed location when WEN is low.
DOUT [ ]	Data Output	Data output bus. The data output is data stored in the accessed location during a read access. Data output driver has tri-state logic. When OEN is low, the driver drives a certain value. Otherwise, data output keeps Hi-Z state. During a write access, data on DOUT is predictable.

Pin Capacitance

Unit: [SL]

CSN	WEN	BWEN	OEN	A	DI	DOUT
4.1567	3.9632	3.1644	3.9632	3.9632	3.1644	16.5880

NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

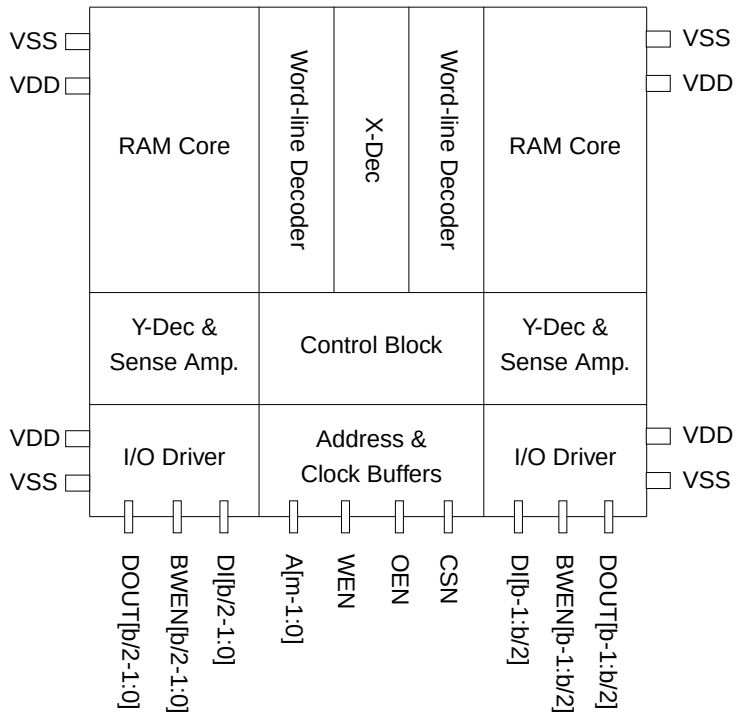
SPARAMBW_HD

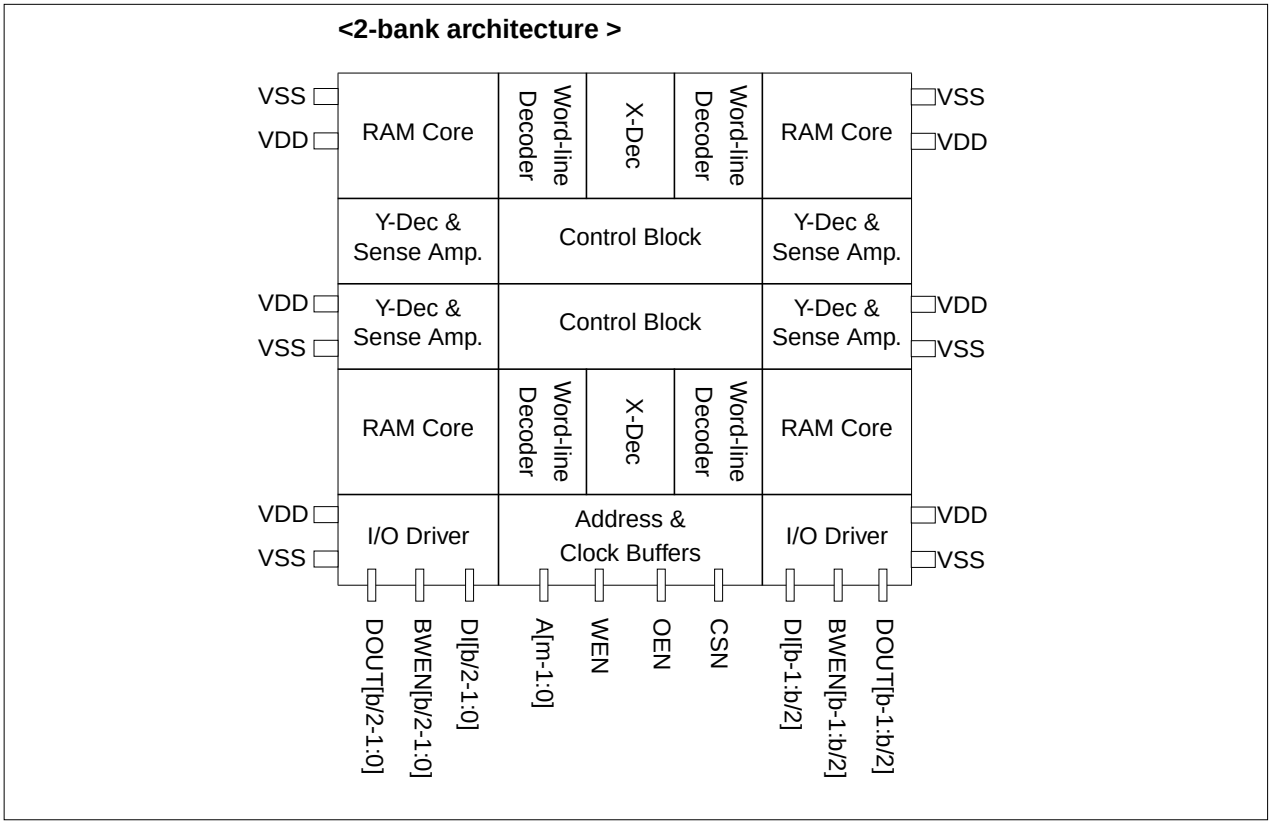
High-Density Single-Port Asynchronous Static RAM with Bit-Write

Block Diagrams

SPARAMBW_HD has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPARAMBW_HD compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the top edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the top-edge, the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>





Application Notes

1. Permitting over-the-cell routing
In chip-level layout, over-the-cell routing in SPARAMBW_HD is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPARAMBW_HD.

4. Avoiding short transition on the address bus
In SPARAMBW_HD, rather than the write operation which is synchronously performed by WEN signal, the read operation is asynchronously performed whenever the address transition is occurred. In this case, if the short transition on the address, called a skew, is happened, since SPARAMBW_HD recognizes the short address transition as the stable address transition and do perform a read operation. At that time, while in the read operation, the data stored in the memory may be corrupted due to the short transition. To prevent such fail, the stable address cycle time (tcyc) is required. The essential requirement to recognize valid address transition is that at least minimum address period should be equal or greater than tacc (access time).

5. A byte-write or word-write operation with SPARAMBW_HD
Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPARAM_HD. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

6. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Address cycle time	t_{as}	Address setup time
t_{cas}	Address setup time for CSN rise	t_{ah}	Address hold time
t_{bwh}	BWEN hold time	t_{bws}	BWEN setup time
t_{wh}	WEN hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{wen}	WEN pulse width low
t_{acc}	Data access time for read cycle	t_{wacc}	Data access time for WEN rise
t_{da}	De-access time	t_{wda}	De-access time for WEN rise
t_{zd}	DOUT high-Z to drive time	t_{dz}	DOUT drive to high-Z time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**256**	**256**	**512**	**512**	**768**	**768**
bpw	**32**	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.53	2.55	2.60	2.60	2.69	2.67	2.79	2.75
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	2.71	2.73	2.78	2.78	2.87	2.85	2.97	2.93
t_{ah}	0.39	0.38	0.45	0.42	0.56	0.49	0.68	0.57
t_{wh}	2.71	2.73	2.78	2.78	2.87	2.85	2.97	2.93
t_{ds}	0.31	0.29	0.33	0.30	0.37	0.32	0.43	0.34
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.04	1.09	1.06	1.11	1.08	1.14	1.11	1.17
t_{wen}	1.67	1.67	1.70	1.69	1.77	1.73	1.85	1.78
t_{acc}	2.53	2.55	2.60	2.60	2.69	2.67	2.79	2.75
t_{da}	2.25	2.28	2.32	2.33	2.41	2.40	2.51	2.48
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.86	0.91	0.88	0.94	0.90	0.96	0.93	0.99
t_{dz}	0.38	0.38	0.41	0.41	0.44	0.44	0.47	0.47
t_{zd}	0.26	0.26	0.30	0.30	0.33	0.33	0.36	0.36
t_{od}	0.44	0.45	0.48	0.48	0.51	0.51	0.55	0.55
Power (µW/MHz)								
Power_read	98.59	96.80	135.96	131.05	181.51	169.54	234.70	214.91
Power_write	138.80	133.21	211.54	193.33	322.35	273.68	455.01	370.13
Power_standby	18.06	37.68	25.68	53.16	34.24	70.38	42.69	88.86
Area (µm)								
Width	574.72	654.20	773.00	895.36	971.28	1136.52	1166.42	1374.54
Height	203.34	337.54	250.50	384.70	344.82	479.02	439.14	573.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parametersy							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.90	2.83	3.06	2.95	3.23	3.06	3.36
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	3.07	3.01	3.24	3.13	3.41	3.24	3.54
t_{ah}	0.80	0.65	1.01	0.77	1.22	0.89	1.24
t_{wh}	3.07	3.01	3.24	3.13	3.41	3.24	3.54
t_{ds}	0.48	0.36	0.60	0.42	0.72	0.47	0.73
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.13	1.20	1.16	1.24	1.18	1.28	1.35
t_{wen}	1.93	1.83	2.09	1.91	2.25	1.99	2.35
t_{acc}	2.90	2.83	3.06	2.95	3.23	3.06	3.36
t_{da}	2.62	2.56	2.78	2.68	2.95	2.79	3.09
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.95	1.02	0.98	1.06	1.00	1.10	1.17
t_{dz}	0.50	0.50	0.53	0.53	0.56	0.56	0.56
t_{zd}	0.40	0.40	0.44	0.43	0.47	0.47	0.47
t_{od}	0.58	0.59	0.62	0.62	0.66	0.65	0.66
Power (µW/MHz)							
Power_read	291.21	262.07	369.21	319.11	454.12	379.47	458.92
Power_write	605.25	478.95	839.12	639.83	1113.90	823.84	1139.20
Power_standby	51.16	107.74	60.97	129.61	70.78	152.40	179.14
Area (µm)							
Width	1361.57	1612.56	1556.71	1850.58	1751.85	2088.61	2094.89
Height	533.46	667.66	722.10	856.30	910.74	1044.94	1799.50

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**512**	**512**	**1024**	**1024**	**1536**	**1536**
bpw	**16**	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.52	2.54	2.58	2.59	2.67	2.65	2.76	2.72
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	2.70	2.72	2.76	2.76	2.85	2.83	2.94	2.90
t_{ah}	0.40	0.39	0.47	0.44	0.57	0.50	0.70	0.59
t_{wh}	2.70	2.72	2.76	2.76	2.85	2.83	2.94	2.90
t_{ds}	0.34	0.32	0.35	0.32	0.40	0.34	0.46	0.37
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.03	1.08	1.04	1.09	1.06	1.11	1.07	1.14
t_{wen}	1.69	1.70	1.73	1.71	1.80	1.75	1.88	1.80
t_{acc}	2.52	2.54	2.58	2.59	2.67	2.65	2.76	2.72
t_{da}	2.24	2.27	2.30	2.32	2.39	2.38	2.48	2.45
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.85	0.90	0.87	0.92	0.88	0.94	0.90	0.96
t_{dz}	0.36	0.36	0.38	0.38	0.40	0.40	0.42	0.42
t_{zd}	0.24	0.24	0.27	0.27	0.29	0.29	0.32	0.31
t_{od}	0.43	0.43	0.45	0.45	0.47	0.47	0.50	0.50
Power (µW/MHz)								
Power_read	88.29	86.52	120.24	115.36	160.31	148.42	207.54	187.78
Power_write	118.03	112.98	177.51	161.55	269.46	226.92	382.03	305.64
Power_standby	12.26	25.48	16.87	34.45	22.44	44.89	27.63	55.88
Area (µm)								
Width	574.72	611.32	773.00	831.04	971.28	1050.76	1166.42	1267.34
Height	203.34	337.54	250.50	384.70	344.82	479.02	439.14	573.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.86	2.79	3.01	2.90	3.17	3.00	3.30
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	3.03	2.97	3.19	3.07	3.35	3.18	3.48
t_{ah}	0.82	0.67	1.03	0.79	1.24	0.91	1.27
t_{wh}	3.03	2.97	3.19	3.07	3.35	3.18	3.48
t_{ds}	0.51	0.39	0.63	0.44	0.75	0.50	0.76
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.09	1.16	1.10	1.19	1.12	1.22	1.29
t_{wen}	1.96	1.84	2.12	1.93	2.28	2.02	2.37
t_{acc}	2.86	2.79	3.01	2.90	3.17	3.00	3.30
t_{da}	2.57	2.52	2.73	2.63	2.89	2.73	3.03
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.91	0.98	0.93	1.01	0.94	1.04	1.11
t_{dz}	0.45	0.45	0.47	0.47	0.49	0.49	0.49
t_{zd}	0.34	0.34	0.36	0.37	0.39	0.39	0.39
t_{od}	0.52	0.52	0.55	0.55	0.57	0.57	0.57
Power (µW/MHz)							
Power_read	258.12	228.88	330.17	279.98	409.15	334.43	414.11
Power_write	513.46	396.11	707.38	528.54	931.41	681.49	944.44
Power_standby	32.84	67.11	39.39	80.35	45.96	94.07	114.26
Area (µm)							
Width	1361.57	1483.92	1556.71	1700.50	1751.85	1917.09	1923.37
Height	533.46	667.66	722.10	856.30	910.74	1044.94	1799.50

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**1024**	**1024**	**2048**	**2048**	**3072**	**3072**
bpw	**8**	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.54	2.56	2.60	2.61	2.68	2.67	2.78	2.74
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	2.71	2.74	2.77	2.79	2.86	2.85	2.95	2.92
t_{ah}	0.40	0.39	0.47	0.44	0.57	0.50	0.70	0.59
t_{wh}	2.71	2.74	2.77	2.79	2.86	2.85	2.95	2.92
t_{ds}	0.35	0.35	0.37	0.35	0.41	0.37	0.47	0.39
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.04	1.10	1.06	1.12	1.07	1.14	1.09	1.16
t_{wen}	1.71	1.72	1.74	1.74	1.81	1.78	1.89	1.83
t_{acc}	2.54	2.56	2.60	2.61	2.68	2.67	2.78	2.74
t_{da}	2.26	2.29	2.32	2.34	2.40	2.40	2.50	2.47
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.87	0.92	0.88	0.94	0.89	0.96	0.91	0.98
t_{dz}	0.36	0.36	0.38	0.38	0.40	0.40	0.42	0.42
t_{zd}	0.24	0.24	0.27	0.27	0.29	0.29	0.32	0.32
t_{od}	0.43	0.43	0.45	0.45	0.47	0.47	0.50	0.50
Power (µW/MHz)								
Power_read	84.60	82.81	114.65	109.77	152.82	140.94	198.11	178.35
Power_write	105.74	100.94	157.78	141.64	239.54	198.20	340.56	269.54
Power_standby	9.78	20.23	13.15	26.49	17.45	34.06	21.36	41.97
Area (µm)								
Width	574.72	589.88	773.00	798.88	971.28	1007.88	1166.42	1213.74
Height	203.34	337.54	250.50	384.70	344.82	479.02	439.14	573.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.87	2.81	3.03	2.92	3.18	3.03	3.32
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	3.05	2.99	3.20	3.10	3.36	3.20	3.50
t_{ah}	0.82	0.67	1.03	0.79	1.24	0.91	1.27
t_{wh}	3.05	2.99	3.20	3.10	3.36	3.20	3.50
t_{ds}	0.52	0.42	0.64	0.47	0.76	0.53	0.79
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.10	1.18	1.12	1.21	1.13	1.24	1.31
t_{wen}	1.97	1.87	2.13	1.96	2.30	2.05	2.40
t_{acc}	2.87	2.81	3.03	2.92	3.18	3.03	3.32
t_{da}	2.59	2.54	2.75	2.65	2.91	2.76	3.05
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.93	1.00	0.94	1.04	0.96	1.07	1.13
t_{dz}	0.45	0.45	0.47	0.47	0.49	0.49	0.49
t_{zd}	0.34	0.34	0.36	0.36	0.39	0.39	0.39
t_{od}	0.52	0.52	0.55	0.55	0.57	0.57	0.57
Power (µW/MHz)							
Power_read	246.74	217.48	316.91	266.62	394.04	319.12	399.09
Power_write	458.86	349.81	634.87	468.92	838.44	605.40	845.82
Power_standby	25.27	50.03	30.50	59.60	35.75	69.43	86.31
Area (µm)							
Width	1361.57	1419.60	1556.71	1625.46	1751.85	1831.33	1837.61
Height	533.46	667.66	722.10	856.30	910.74	1044.94	1799.50

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**1024**	**1024**	**2048**	**2048**	**4096**	**4096**	**6144**	**6144**
bpw	**4**	**4**	**6**	**6**	**8**	**8**	**10**	**10**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.56	2.60	2.62	2.65	2.71	2.71	2.80	2.78
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	2.74	2.78	2.80	2.83	2.88	2.89	2.98	2.96
t_{ah}	0.40	0.39	0.47	0.44	0.57	0.50	0.70	0.59
t_{wh}	2.74	2.78	2.80	2.83	2.88	2.89	2.98	2.96
t_{ds}	0.37	0.39	0.39	0.40	0.44	0.42	0.49	0.45
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.07	1.14	1.08	1.16	1.09	1.18	1.11	1.20
t_{wen}	1.74	1.77	1.77	1.79	1.84	1.83	1.92	1.88
t_{acc}	2.56	2.60	2.62	2.65	2.71	2.71	2.80	2.78
t_{da}	2.28	2.34	2.34	2.38	2.43	2.45	2.52	2.52
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.89	0.96	0.90	0.98	0.92	1.00	0.93	1.02
t_{dz}	0.36	0.36	0.38	0.38	0.40	0.40	0.42	0.42
t_{zd}	0.24	0.24	0.27	0.27	0.29	0.29	0.32	0.32
t_{od}	0.43	0.43	0.45	0.45	0.47	0.47	0.50	0.50
Power (µW/MHz)								
Power_read	82.70	80.93	111.84	106.98	149.12	137.24	193.44	173.68
Power_write	99.72	95.05	147.99	133.66	224.67	186.56	319.08	252.24
Power_standby	8.52	17.56	11.27	22.49	14.99	28.65	18.23	35.05
Area (µm)								
Width	574.72	579.16	773.00	782.80	971.28	986.44	1166.42	1186.94
Height	203.34	337.54	250.50	384.70	344.82	479.02	439.14	573.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

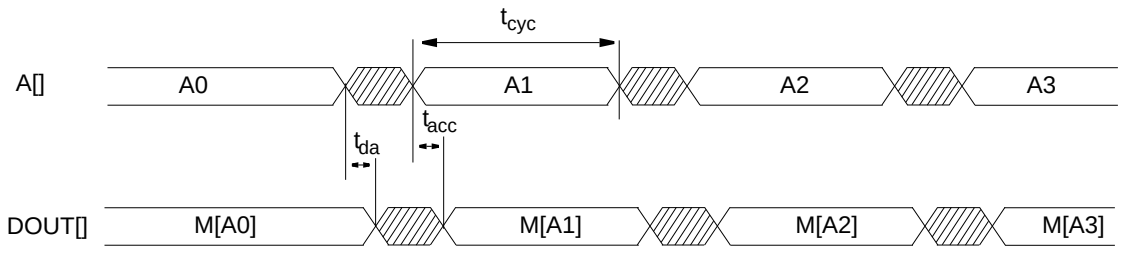
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters							
words	**8192**	**8192**	**12288**	**12288**	**16384**	**16384**	**32768**
bpw	**12**	**12**	**14**	**14**	**16**	**16**	**16**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.89	2.85	3.05	2.96	3.21	3.07	3.36
t_{as}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cas}	3.07	3.03	3.23	3.14	3.39	3.25	3.54
t_{ah}	0.82	0.67	1.03	0.79	1.24	0.91	1.27
t_{wh}	3.07	3.03	3.23	3.14	3.39	3.25	3.54
t_{ds}	0.55	0.47	0.66	0.53	0.78	0.58	0.86
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{ch}	1.13	1.22	1.14	1.25	1.16	1.29	1.35
t_{wen}	2.00	1.93	2.16	2.01	2.33	2.11	2.47
t_{acc}	2.89	2.85	3.05	2.96	3.21	3.07	3.36
t_{da}	2.61	2.59	2.77	2.69	2.93	2.80	3.10
t_{wda}	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t_{wacc}	0.95	1.05	0.97	1.08	0.98	1.11	1.17
t_{dz}	0.45	0.45	0.47	0.47	0.49	0.49	0.49
t_{zd}	0.34	0.34	0.36	0.36	0.39	0.39	0.39
t_{od}	0.52	0.52	0.55	0.55	0.58	0.57	0.57
Power (µW/MHz)							
Power_read	241.13	211.86	310.37	260.07	386.58	311.66	391.66
Power_write	430.44	326.80	598.39	438.96	792.18	567.63	796.75
Power_standby	21.50	41.55	26.10	49.32	30.74	57.24	72.46
Area (µm)							
Width	1361.57	1387.44	1556.71	1587.94	1751.85	1788.45	1794.73
Height	533.46	667.66	722.10	856.30	910.74	1044.94	1799.50

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

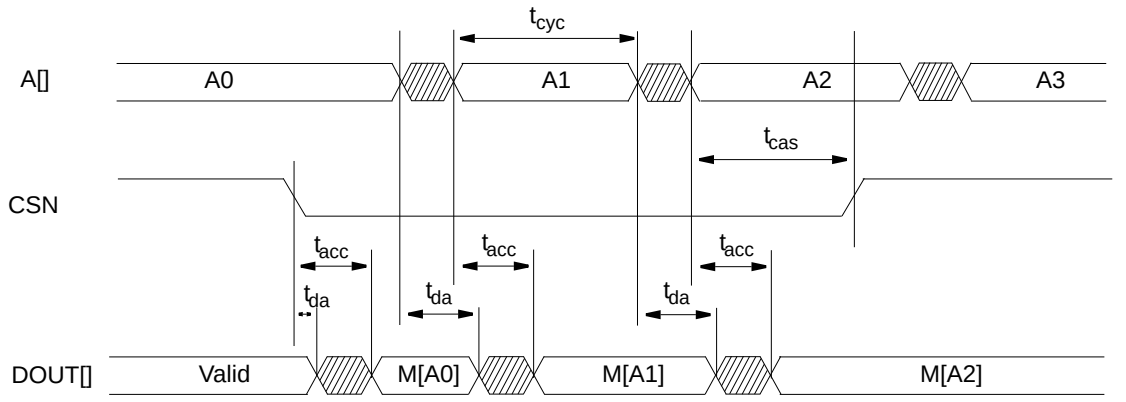
Timing Diagrams

Read Cycle



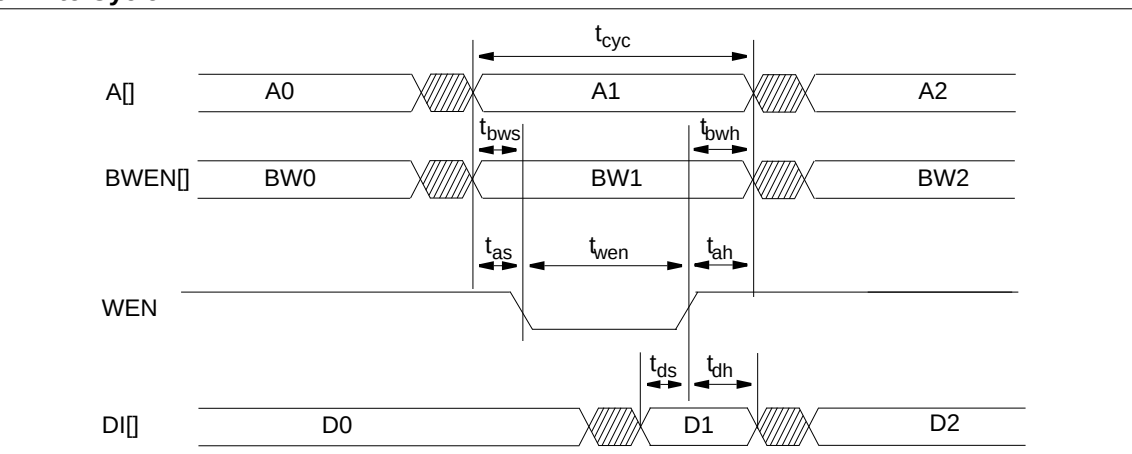
(WEN = high, CSN = low, OEN = low, BWEN[], DI[] = don't care)

Read Cycle with CSN-Controlled



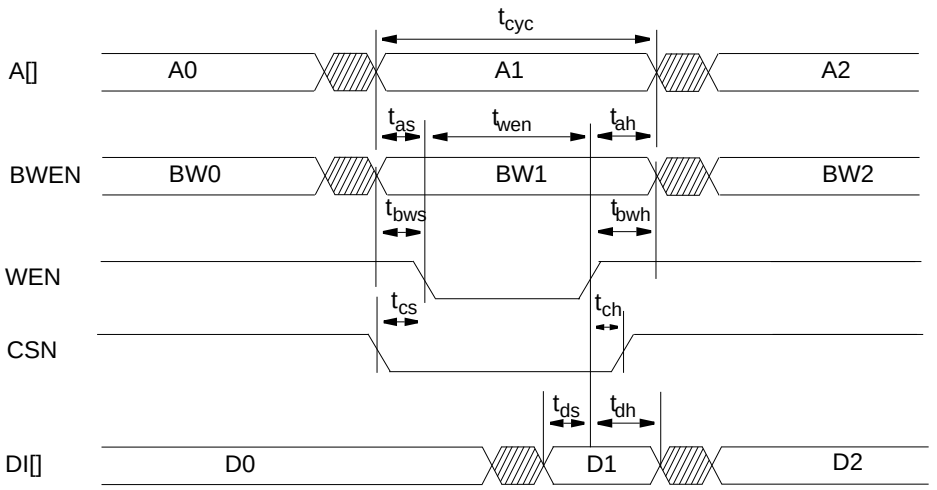
(OEN = low, WEN = high, BWEN[], DI[] = don't care)

Basic Write Cycle

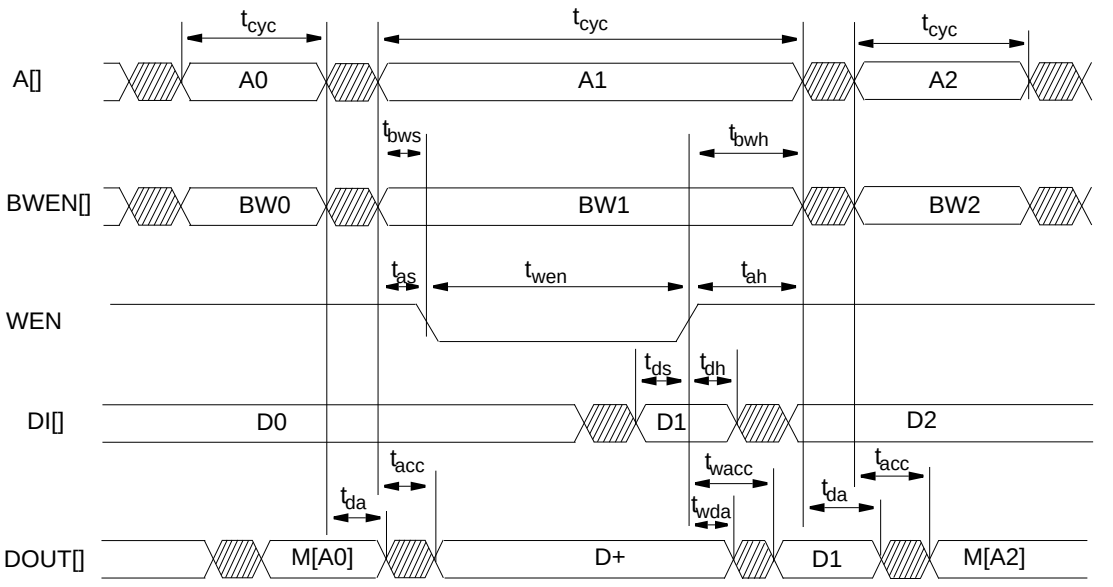


(CSN = low, OEN = don't care)

Write Cycle with CSN-Controlled



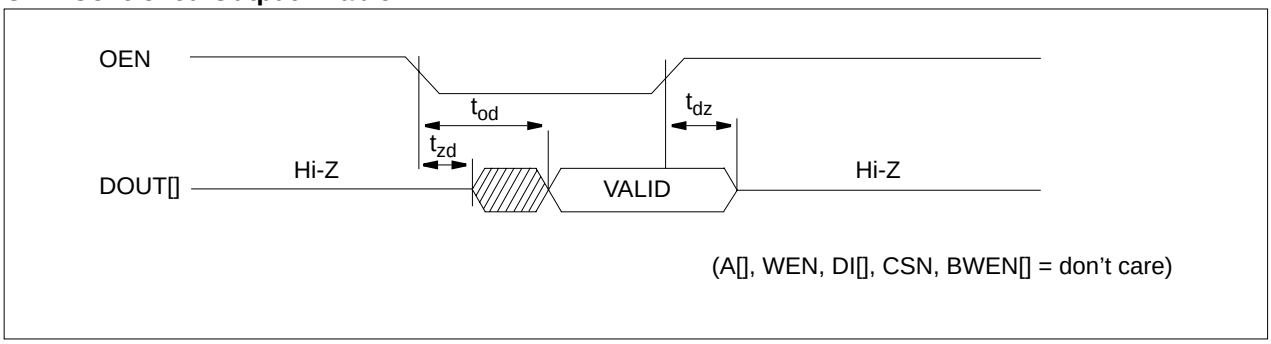
Read-Modified-Write Cycle



NOTES:

1. When the WEN hold time after the last address bit transition is satisfied, D+ will toggle in response to a successful read of the initial contents of address A1. When the WEN hold time after the last address bit transition is not satisfied, D+ will go to unknown state.
2. Address bits are not allowed to change while WEN is low. If they do change, then the data for one or more addresses in the memory array may be corrupted.

OEN-Controlled Output Enable

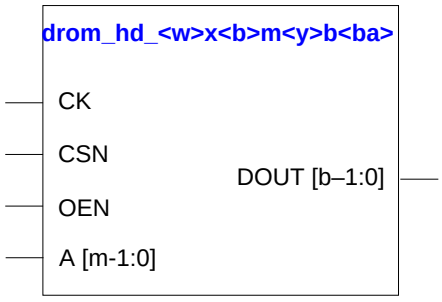


NOTE: “don't care” means the condition that these pins are in normal operation mode.

DROM_HD

High-Density Synchronous Diffusion Programmable ROM

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Banks (ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density applications
- Low-average power operation
- Diffusion-programmable code available
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down mode available
- Low noise output optimization
- Zero standby current
- Zero hold time
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512K bits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DROM_HD is a synchronous diffusion programmable ROM which is provided as a compiler. DROM_HD is intended for use in high-density applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

DROM_HD Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read cycle

Parameter Description

DROM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y) and Number of banks(ba).

Parameters			Ymux = 8	Ymux = 16	Ymux = 32
Words (w)	ba = 1	Min	64	128	256
		Max	2048	4096	8192
		Step	32	64	128
	ba = 2	Min	128	256	512
		Max	4096	8192	16384
		Step	64	128	256
Bpw (b)		Min	2	2	2
		Max	128	64	32
		Step	1	1	1

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT
ba = 1	6.21	2.40	2.56	2.58	10.25
ba = 2	4.04	2.40	2.56	2.58	10.25

NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

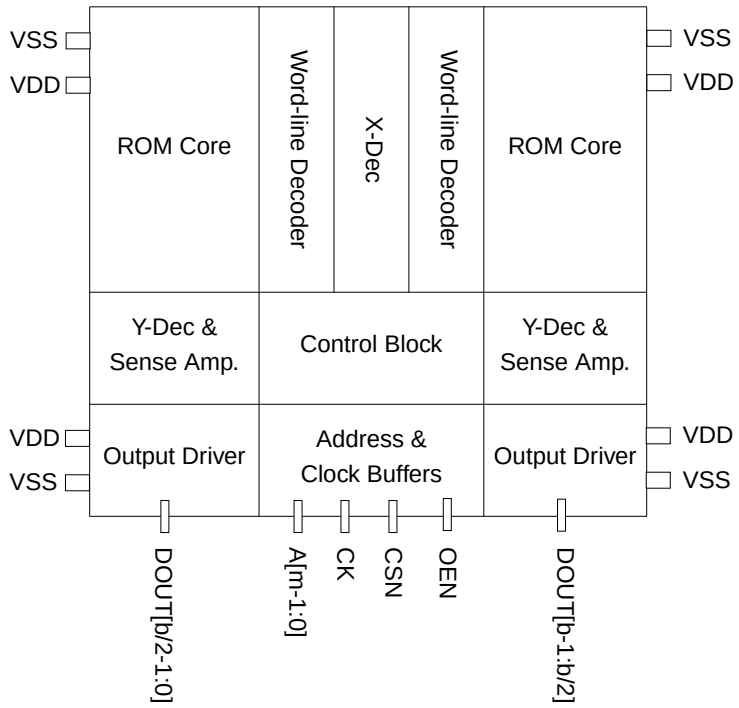
DROM_HD

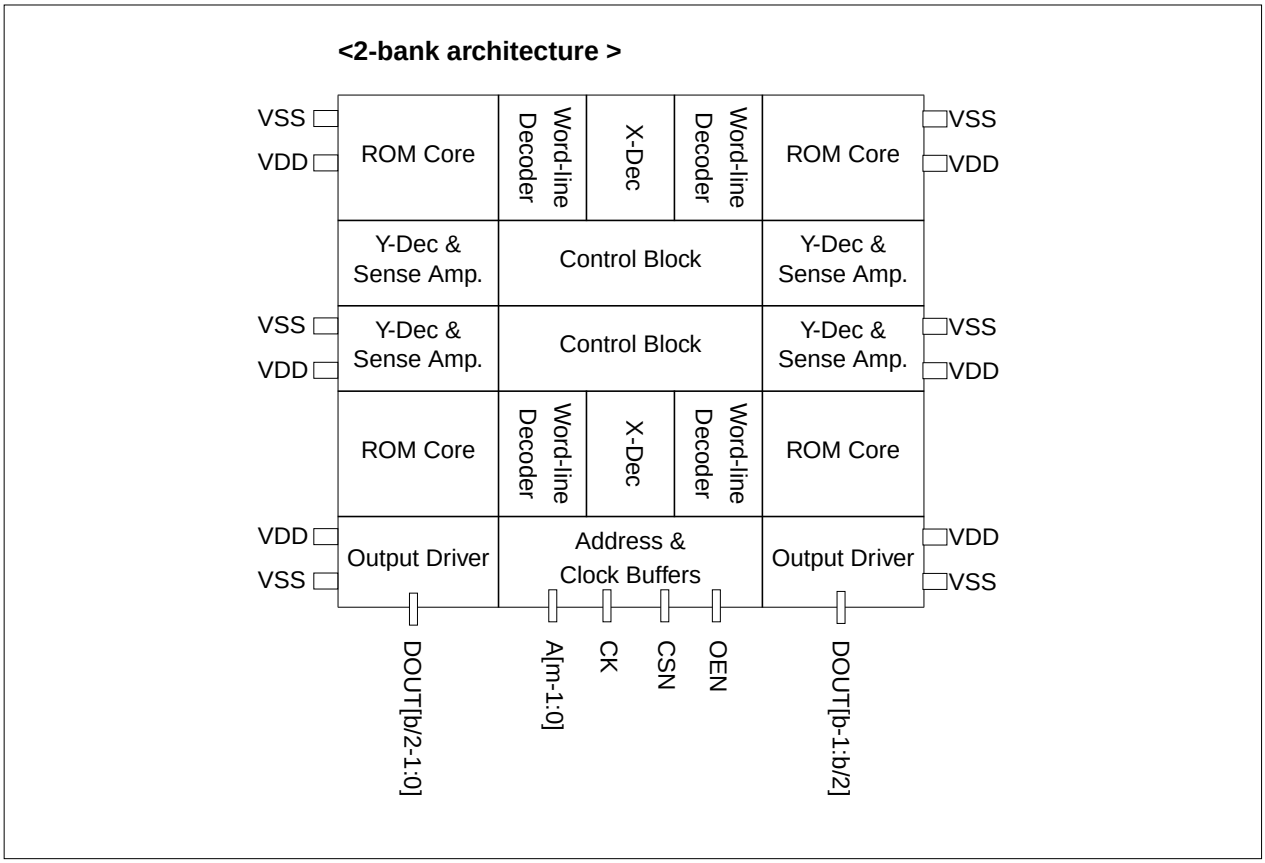
High-Density Synchronous Diffusion Programmable ROM

Block Diagrams

DROM_HD has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from DROM_HD compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the top edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the top-edge, the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>





Application Notes

1. Permitting over-the-cell routing
In chip-level layout, over-the-cell routing in DROM_HD is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DROM_HD.

4. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ch}	CSN hold time from CK rise
t_{ckl}	Clock pulse width low	t_{acc}	Data access time
t_{ckh}	Clock pulse width high	t_{da}	De-access time
t_{as}	Address setup time	t_{dz}	DOUT drive to high-Z time
t_{ah}	Address hold time	t_{zd}	DOUT high-Z to drive time
t_{cs}	CSN setup time	t_{od}	OEN to valid output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**64**	**128**	**128**	**256**	**256**	**512**	**512**
bpw	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	2.53	2.53	2.65	2.53	2.65	2.56	2.68
t_{ckl}	0.51	0.51	0.57	0.51	0.57	0.51	0.59
t_{ckh}	0.79	0.79	0.90	0.79	0.91	0.79	0.92
t_{as}	0.25	0.24	0.57	0.24	0.57	0.25	0.59
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.51	0.51	0.57	0.51	0.57	0.51	0.59
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.68	1.74	1.90	1.78	1.96	1.81	2.04
t_{da}	1.33	1.41	1.52	1.49	1.60	1.63	1.72
t_{dz}	0.34	0.38	0.38	0.41	0.41	0.45	0.45
t_{zd}	0.45	0.48	0.48	0.51	0.51	0.54	0.54
t_{od}	0.49	0.52	0.52	0.55	0.55	0.58	0.58
Power (µW/MHz)							
Power_read	119.11	163.12	211.30	214.40	262.48	290.63	329.18
Power_standby	21.83	24.07	63.67	27.35	68.64	32.70	76.10
Area (µm)							
Width	422.14	577.91	575.92	735.67	731.69	897.40	889.45
Height	162.02	171.22	316.02	185.62	330.42	214.42	359.22

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DROM_HD

High-Density Synchronous Diffusion Programmable ROM

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.64	2.73	2.78	2.81	2.95	2.91	3.19
t_{ckl}	0.51	0.61	0.51	0.64	0.51	0.66	0.76
t_{ckh}	0.79	0.94	0.79	0.96	0.79	0.98	1.06
t_{as}	0.27	0.61	0.29	0.64	0.32	0.66	0.76
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.51	0.61	0.51	0.64	0.51	0.66	0.76
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.99	2.11	2.17	2.26	2.36	2.41	2.69
t_{da}	1.78	1.88	1.95	2.02	2.13	2.17	2.41
t_{dz}	0.49	0.49	0.52	0.52	0.56	0.56	0.56
t_{zd}	0.58	0.58	0.61	0.61	0.65	0.65	0.65
t_{od}	0.62	0.62	0.65	0.65	0.69	0.69	0.69
Power (µW/MHz)							
Power_read	387.68	425.39	495.65	515.91	614.02	613.67	748.98
Power_standby	37.68	88.59	46.10	96.79	54.53	104.98	142.28
Area (µm)							
Width	1055.82	1051.18	1211.92	1207.28	1368.02	1363.38	1368.02
Height	272.02	416.82	329.62	474.42	387.22	532.02	762.42

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**128**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	2.53	2.53	2.65	2.52	2.65	2.56	2.68
t_{ckl}	0.51	0.51	0.57	0.51	0.57	0.51	0.59
t_{ckh}	0.79	0.79	0.90	0.79	0.91	0.79	0.92
t_{as}	0.25	0.24	0.57	0.24	0.57	0.25	0.59
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.51	0.51	0.57	0.51	0.57	0.51	0.59
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.71	1.76	1.95	1.80	2.01	1.84	2.09
t_{da}	1.34	1.41	1.53	1.50	1.61	1.63	1.73
t_{dz}	0.32	0.34	0.34	0.36	0.36	0.38	0.38
t_{zd}	0.43	0.45	0.45	0.47	0.47	0.49	0.49
t_{od}	0.47	0.49	0.49	0.51	0.51	0.53	0.53
Power (µW/MHz)							
Power_read	91.85	119.80	166.89	152.17	200.48	198.75	245.08
Power_standby	20.78	22.46	60.41	25.18	64.21	29.98	70.60
Area (µm)							
Width	422.14	577.91	575.92	735.67	731.69	897.40	889.45
Height	164.02	171.22	316.02	185.62	330.42	214.42	359.22

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DROM_HD

High-Density Synchronous Diffusion Programmable ROM

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.64	2.73	2.78	2.81	2.95	2.91	3.19
t_{ckl}	0.51	0.61	0.51	0.64	0.51	0.66	0.76
t_{ckh}	0.79	0.94	0.79	0.96	0.79	0.98	1.06
t_{as}	0.27	0.61	0.29	0.64	0.32	0.66	0.76
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.51	0.61	0.51	0.64	0.51	0.66	0.76
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.01	2.15	2.19	2.31	2.38	2.45	2.73
t_{da}	1.78	1.89	1.96	2.03	2.14	2.18	2.42
t_{dz}	0.41	0.41	0.43	0.43	0.46	0.46	0.46
t_{zd}	0.51	0.51	0.53	0.53	0.56	0.56	0.56
t_{od}	0.55	0.55	0.57	0.57	0.60	0.60	0.60
Power (µW/MHz)							
Power_read	256.85	304.64	322.46	360.88	393.59	420.89	512.91
Power_standby	31.41	82.03	42.28	89.14	50.14	96.24	133.53
Area (µm)							
Width	1055.82	1051.18	1211.92	1207.28	1368.02	1363.38	1368.02
Height	272.02	416.82	329.62	474.42	387.22	532.02	762.42

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**256**	**512**	**512**	**1024**	**1024**	**2048**	**2048**
bpw	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	2.53	2.53	2.65	2.53	2.65	2.56	2.68
t_{ckl}	0.51	0.51	0.57	0.51	0.57	0.51	0.59
t_{ckh}	0.79	0.79	0.90	0.79	0.91	0.79	0.92
t_{as}	0.25	0.24	0.57	0.24	0.57	0.25	0.59
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.51	0.51	0.57	0.51	0.57	0.51	0.59
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.75	1.81	2.03	1.85	2.09	1.88	2.17
t_{da}	1.35	1.42	1.54	1.51	1.62	1.64	1.74
t_{dz}	0.30	0.32	0.32	0.33	0.33	0.35	0.35
t_{zd}	0.42	0.43	0.43	0.44	0.44	0.46	0.46
t_{od}	0.45	0.47	0.47	0.48	0.49	0.50	0.50
Power (µW/MHz)							
Power_read	78.41	98.41	145.16	121.33	170.02	153.02	202.12
Power_standby	20.26	21.68	58.80	24.12	62.08	28.63	67.93
Area (µm)							
Width	422.14	577.91	575.92	735.67	731.69	897.40	889.45
Height	164.02	171.22	316.02	185.62	330.42	214.42	359.22

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DROM_HD

High-Density Synchronous Diffusion Programmable ROM

Reference Table

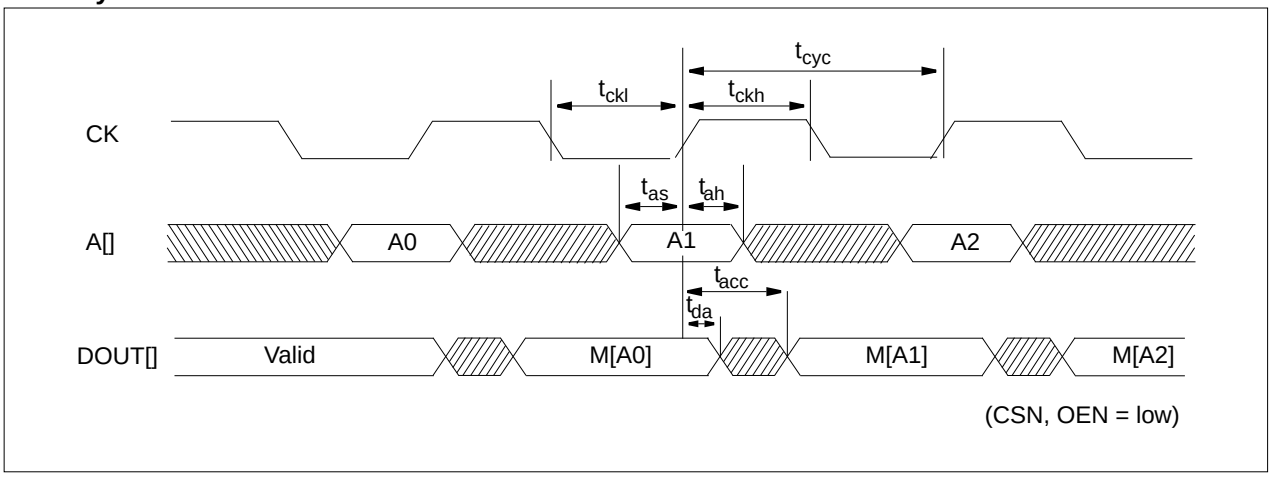
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.64	2.73	2.73	2.81	2.81	2.91	3.19
t_{ckl}	0.51	0.61	0.52	0.64	0.52	0.66	0.76
t_{ckh}	0.79	0.94	0.79	0.96	0.79	0.98	1.06
t_{as}	0.27	0.61	0.24	0.64	0.18	0.66	0.76
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.51	0.61	0.52	0.64	0.52	0.66	0.76
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.05	2.24	2.24	2.39	2.43	2.53	2.81
t_{da}	1.79	1.90	1.97	2.05	2.15	2.20	2.44
t_{dz}	0.37	0.37	0.39	0.39	0.40	0.40	0.40
t_{zd}	0.47	0.47	0.49	0.49	0.51	0.51	0.51
t_{od}	0.51	0.51	0.53	0.53	0.55	0.55	0.55
Power (µW/MHz)							
Power_read	191.69	244.80	236.14	283.91	283.69	325.05	395.20
Power_standby	32.79	78.80	40.38	85.34	47.96	91.89	129.18
Area (µm)							
Width	1055.82	1051.18	1211.92	1207.28	1368.02	1363.38	1368.02
Height	272.02	416.82	329.62	474.42	387.22	532.02	762.42

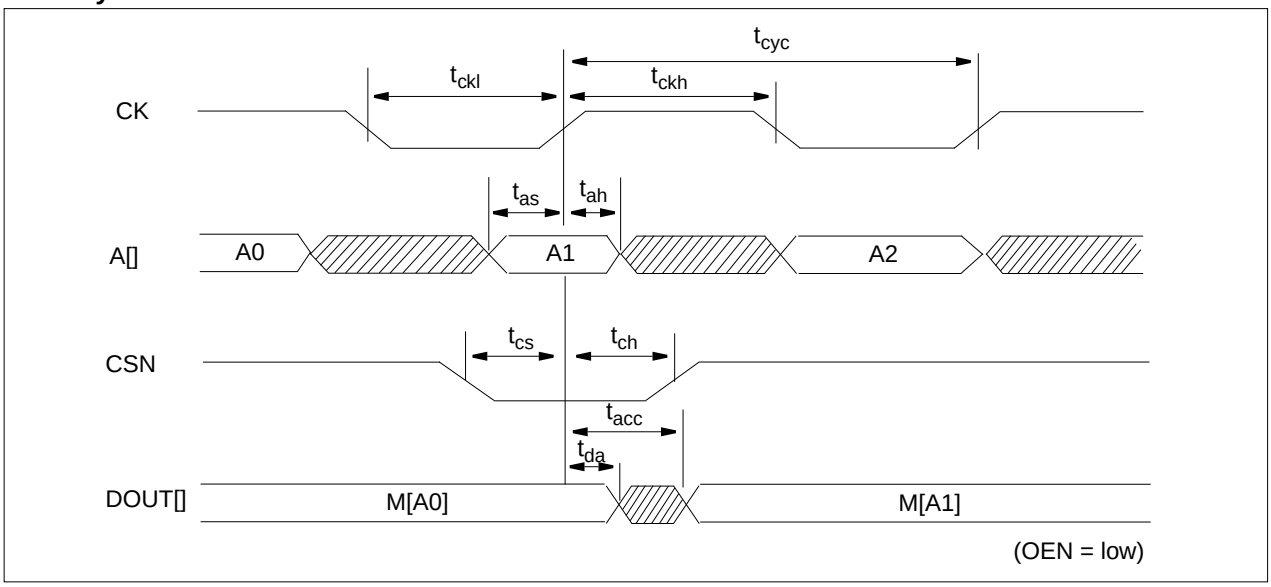
NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Timing Diagrams

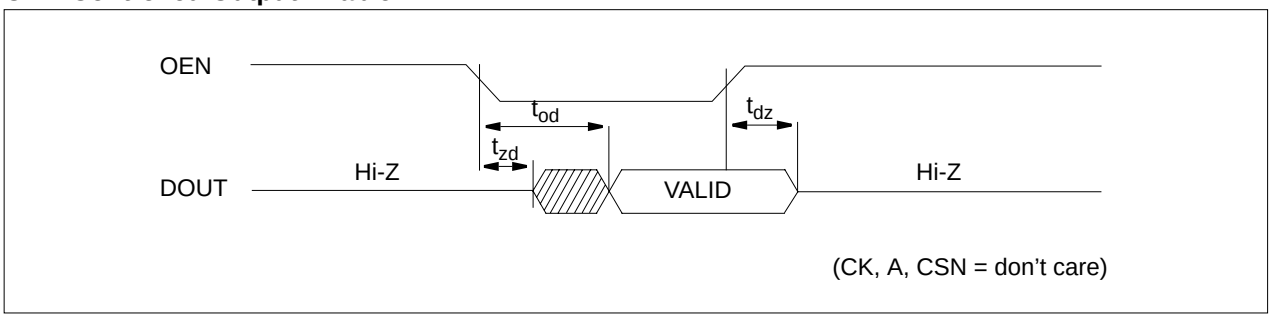
Read Cycle



Read Cycle with CSN Controlled



OEN-Controlled Output Enable

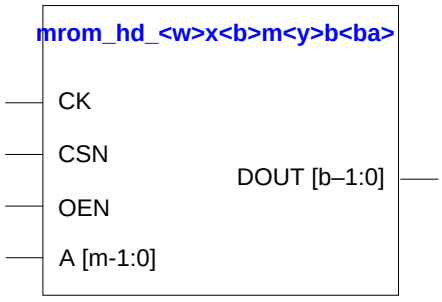


NOTE: "don't care" means the condition that these pins are in normal operation mode.

MROM_HD

High-Density Synchronous Metal-2 Programmable ROM

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Banks (ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density applications
- Low-average power/Low-voltage operation
- Metal2-programmable code available
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down mode available
- Low noise output optimization
- Zero standby current
- Zero hold time
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512K bits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

MROM_HD is a synchronous metal-2 programmable ROM which is provided as a compiler. MROM_HD is intended for use in high-density applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

MROM_HD Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read cycle

Parameter Description

MROM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux = 8	Ymux = 16	Ymux = 32
Words (w)	ba = 1	Min	64	128	256
		Max	2048	4096	8192
		Step	32	64	128
	ba = 2	Min	128	256	512
		Max	4096	8192	16384
		Step	64	128	256
Bpw (b)		Min	2	2	2
		Max	128	64	32
		Step	1	1	1

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT
ba = 1	5.94	1.76	1.97	1.76	7.84
ba = 2	3.24	1.76	1.97	1.76	7.84

NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

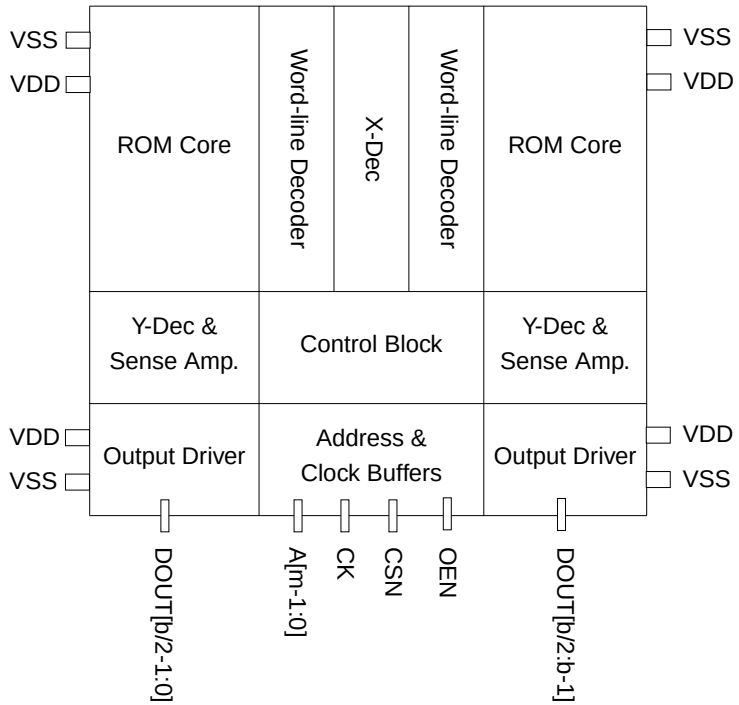
MROM_HD

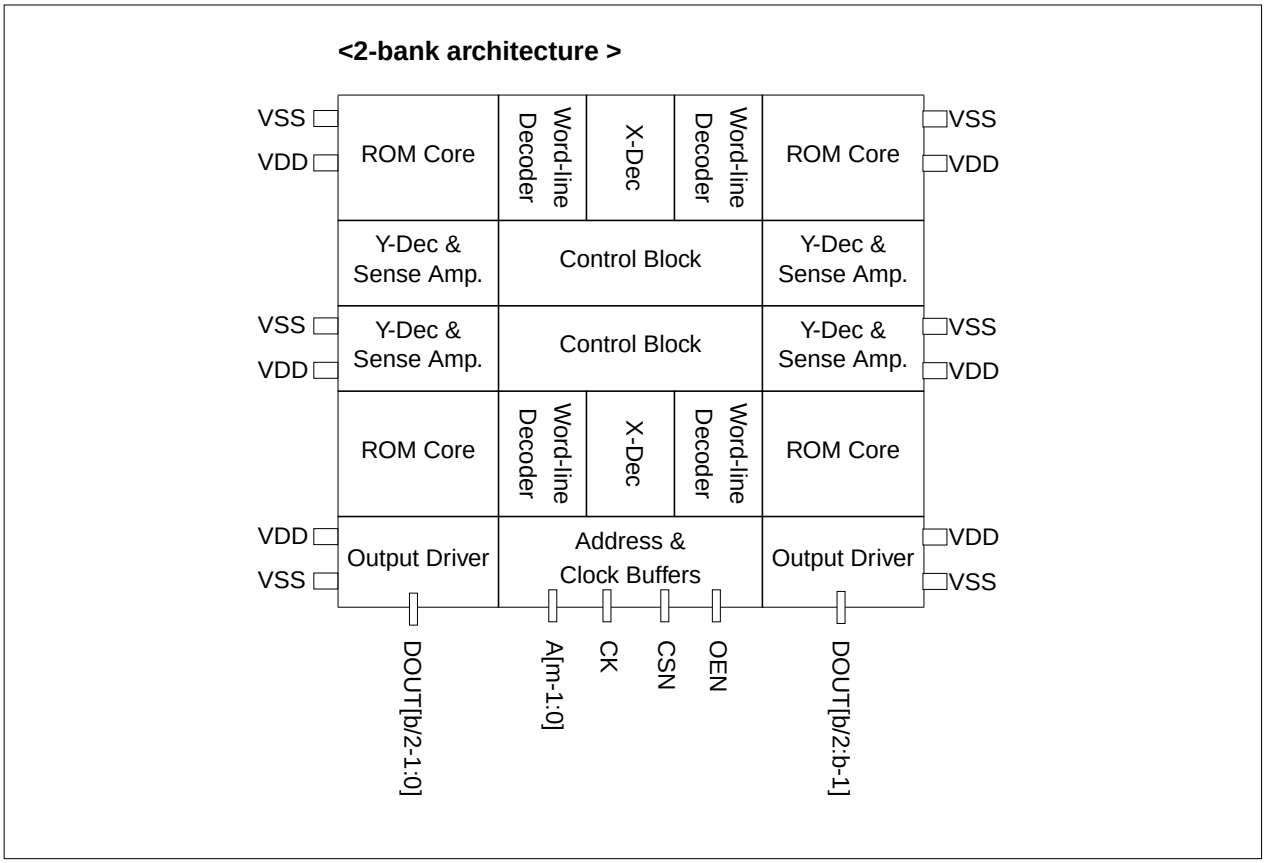
High-Density Synchronous Metal-2 Programmable ROM

Block Diagrams

MROM_HD has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from MROM_HD compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the top-edge, the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>





Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in MROM_HD is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of MROM_HD.

4. Power reduction during standby mode. The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are actived while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ch}	CSN hold time from CK rise
t_{ckl}	Clock pulse width low	t_{acc}	Data access time
t_{ckh}	Clock pulse width high	t_{da}	De-access time
t_{as}	Address setup time	t_{dz}	DOUT drive to high-Z time
t_{ah}	Address hold time	t_{zd}	DOUT high-Z to drive time
t_{cs}	CSN setup time	t_{od}	OEN to valid data output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**64**	**128**	**128**	**256**	**256**	**512**	**512**
bpw	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	2.61	2.61	2.71	2.61	2.71	2.68	1.79
t_{ckl}	0.63	0.63	0.62	0.63	0.62	0.63	0.63
t_{ckh}	0.79	0.79	0.91	0.79	0.91	0.79	0.91
t_{as}	0.34	0.34	0.62	0.33	0.62	0.31	0.63
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.63	0.63	0.62	0.63	0.62	0.63	0.63
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.80	1.91	2.07	1.98	2.17	2.05	2.27
t_{da}	1.43	1.55	1.66	1.68	1.78	1.85	1.93
t_{dz}	0.36	0.40	0.40	0.44	0.44	0.48	0.48
t_{zd}	0.47	0.50	0.50	0.54	0.54	0.58	0.58
t_{od}	0.50	0.54	0.54	0.58	0.58	0.62	0.62
Power (µW/MHz)							
Power_read	131.05	180.76	232.69	245.07	291.65	342.61	396.06
Power_standby	25.98	28.48	72.90	31.88	78.23	37.11	85.77
Area (µm)							
Width	423.48	598.23	596.24	779.09	775.11	961.63	953.68
Height	164.16	177.44	317.58	204.00	344.14	257.12	397.26

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.83	2.91	3.05	3.05	3.28	3.19	3.39
t_{ckl}	0.63	0.64	0.63	0.65	0.63	0.67	0.72
t_{ckh}	0.79	0.92	0.79	0.94	0.79	0.95	0.99
t_{as}	0.26	0.64	0.25	0.65	0.23	0.67	0.72
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.63	0.64	0.63	0.65	0.63	0.67	0.72
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.28	2.37	2.52	2.57	2.75	2.75	3.03
t_{da}	2.07	2.13	2.31	2.33	2.55	2.53	2.76
t_{dz}	0.53	0.53	0.57	0.57	0.61	0.61	0.61
t_{zd}	0.62	0.62	0.66	0.66	0.70	0.70	0.70
t_{od}	0.66	0.66	0.70	0.70	0.74	0.74	0.74
Power (μW/MHz)							
Power_read	477.52	491.26	632.30	606.80	810.61	734.51	948.55
Power_standby	41.53	97.70	48.76	105.14	55.99	112.58	141.78
Area (μm)							
Width	1136.41	1131.77	1308.86	1304.22	1481.32	1476.68	1481.32
Height	363.36	503.50	469.60	609.74	575.84	715.98	1140.94

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**128**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	2.61	2.61	2.71	2.61	2.71	2.68	2.78
t_{ckl}	0.63	0.63	0.62	0.63	0.62	0.63	0.63
t_{ckh}	0.79	0.79	0.90	0.79	0.91	0.79	0.91
t_{as}	0.34	0.34	0.62	0.33	0.62	0.31	0.63
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.63	0.63	0.62	0.63	0.62	0.63	0.63
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.83	1.93	2.12	2.01	2.21	2.07	2.31
t_{da}	1.43	1.56	1.67	1.69	1.79	1.85	1.94
t_{dz}	0.33	0.35	0.35	0.38	0.38	0.41	0.41
t_{zd}	0.44	0.46	0.46	0.49	0.49	0.51	0.51
t_{od}	0.48	0.50	0.50	0.53	0.53	0.55	0.55
Power (µW/MHz)							
Power_read	102.20	134.73	186.21	176.10	226.61	235.51	276.94
Power_standby	24.90	26.84	69.59	29.69	73.80	34.38	80.26
Area (µm)							
Width	423.48	598.59	596.60	779.09	775.11	961.38	953.43
Height	164.16	177.44	317.58	204.00	344.14	257.12	397.26

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.83	2.90	3.05	3.05	3.28	3.19	3.40
t_{ckl}	0.63	0.64	0.63	0.65	0.63	0.67	0.72
t_{ckh}	0.79	0.92	0.79	0.94	0.79	0.95	0.99
t_{as}	0.26	0.64	0.25	0.65	0.23	0.67	0.72
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.63	0.64	0.63	0.65	0.63	0.67	0.72
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.30	2.42	2.54	2.61	2.78	2.80	3.07
t_{da}	2.08	2.14	2.32	2.34	2.55	2.54	2.77
t_{dz}	0.44	0.44	0.46	0.46	0.49	0.49	0.49
t_{zd}	0.54	0.54	0.56	0.56	0.59	0.59	0.59
t_{od}	0.58	0.58	0.60	0.60	0.63	0.63	0.63
Power (µW/MHz)							
Power_read	315.10	352.12	406.44	422.50	510.21	499.10	630.56
Power_standby	38.23	91.12	44.92	97.46	51.60	103.80	133.03
Area (µm)							
Width	1136.24	1131.60	1308.78	130414	1481.32	1476.68	1481.32
Height	363.36	503.50	469.60	609.74	575.84	715.98	1140.94

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**256**	**512**	**512**	**1024**	**1024**	**2048**	**2048**
bpw	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	2.61	2.61	2.71	2.61	2.71	2.67	2.77
t_{ckl}	0.63	0.63	0.62	0.63	0.62	0.63	0.63
t_{ckh}	0.79	0.79	0.91	0.79	0.91	0.79	0.91
t_{as}	0.34	0.34	0.62	0.33	0.62	0.31	0.63
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.63	0.63	0.62	0.63	0.62	0.63	0.63
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	1.88	1.98	2.20	2.05	2.30	2.10	2.39
t_{da}	1.44	1.57	1.68	1.70	1.80	1.86	1.95
t_{dz}	0.31	0.33	0.33	0.35	0.35	0.37	0.37
t_{zd}	0.42	0.44	0.44	0.46	0.46	0.48	0.48
t_{od}	0.46	0.48	0.48	0.50	0.50	0.52	0.52
Power (µW/MHz)							
Power_read	87.98	112.37	163.66	141.91	193.97	181.95	230.55
Power_standby	24.37	26.02	67.97	28.59	71.63	33.00	77.50
Area (µm)							
Width	423.48	599.50	597.51	779.09	775.11	960.84	952.89
Height	164.16	177.44	317.58	204.00	344.14	257.12	397.26

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

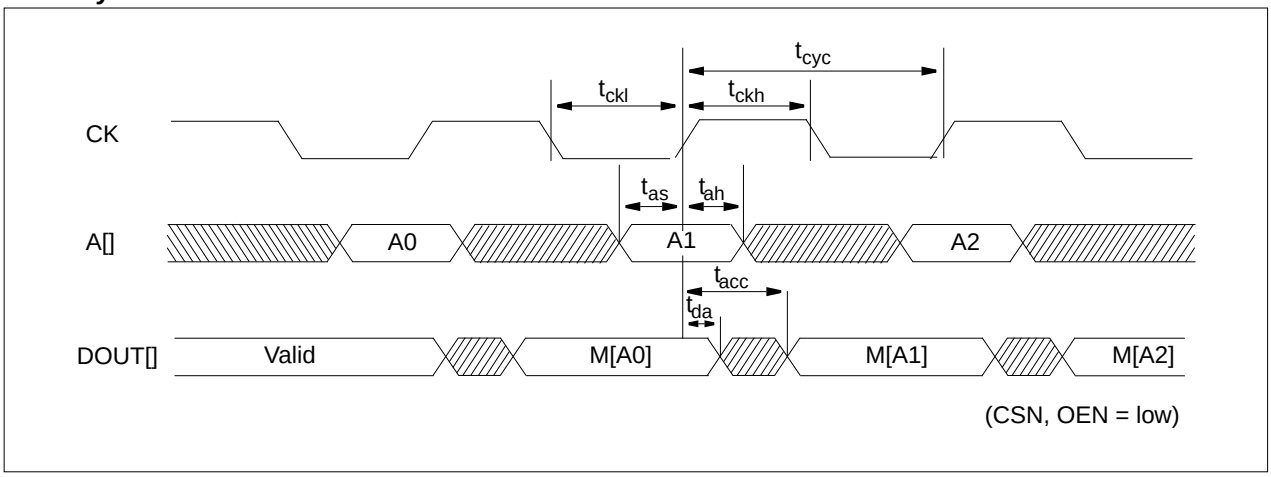
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	2.82	2.90	3.05	3.04	3.28	3.19	3.40
t_{ckl}	0.63	0.64	0.63	0.66	0.63	0.67	0.72
t_{ckh}	0.79	0.92	0.79	0.94	0.79	0.95	0.99
t_{as}	0.26	0.64	0.25	0.65	0.23	0.67	0.72
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.63	0.64	0.63	0.65	0.63	0.67	0.72
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.34	2.50	2.58	2.70	2.82	2.88	3.15
t_{da}	2.09	2.15	2.33	2.35	2.57	2.55	2.78
t_{dz}	0.39	0.39	0.41	0.41	0.43	0.43	0.43
t_{zd}	0.49	0.49	0.51	0.51	0.53	0.53	0.53
t_{od}	0.53	0.53	0.55	0.55	0.57	0.57	0.57
Power (µW/MHz)							
Power_read	234.07	282.72	293.74	330.65	360.35	381.92	471.71
Power_standby	36.59	87.79	43.00	93.61	49.42	99.41	128.69
Area (µm)							
Width	1135.88	1131.24	1308.60	1303.96	1481.32	1476.68	1481.32
Height	363.36	503.50	469.60	609.74	575.84	715.98	1140.94

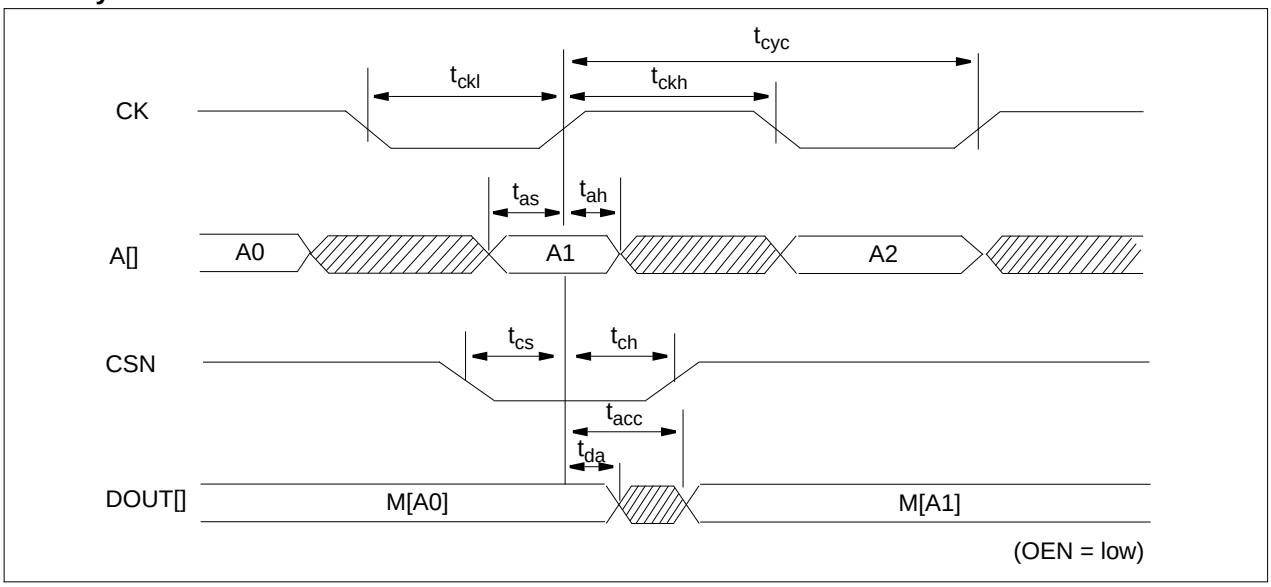
NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Timing Diagrams

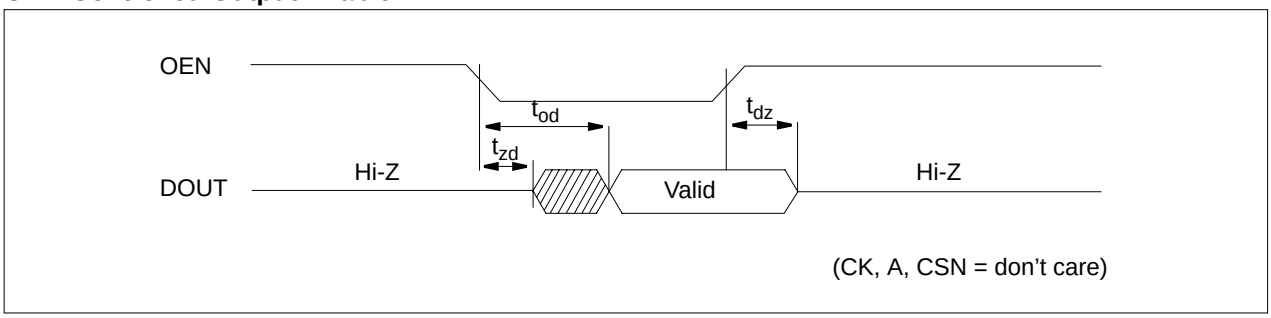
Read Cycle



Read Cycle with CSN Controlled



OEN-Controlled Output Enable

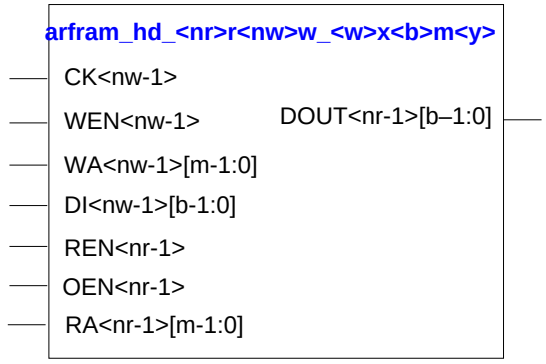


NOTE: "don't care" means the condition that these pins are in normal operation mode.

ARFRAM_HD

High-Density Multi-Port Asynchronous Register File

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. Writes(nw) is the number of write ports(1-to-2).
5. Reads(nr) is the number of read ports(1-to-2).
6. m = $\lceil \log_2 w \rceil$

Features

- High-density application
- Suitable for high-speed application
- Synchronous write operation
- Asynchronous read operation
- Fully independent port
- Latched input and output
- Separated data I/O
- Flexible aspect ratio
- Asynchronous tristate output
- Zero standby current
- Configurable 1-to-2 read ports
- Configurable 1-to-2 write ports
- Up to 16K bits capacity
- Up to 1024K number of words
- Up to 64 number of bits per word

Function Description

ARFRAM_HD is a multi-port asynchronous register file which is provided as a compiler. ARFRAM_HD is intended for use in high-density applications. It allows maximum 4 ports with configurable 1-to-2 read ports and 1-to-2 write ports. All read and write ports are fully independent. On the rising edge of CK, the write cycle is initiated when WEN is low. While CK is high, the data at DI[] is written into the memory location specified on WA[]. At the falling edge of CK, the write cycle is terminated. If WEN is high, WA[] and DI[] are disabled . It is called “write standby mode”. When REN and OEN are low, the data stored in the memory location specified on RA[] becomes valid through DOUT[] after a delay. If REN is high, RA[] is disabled and DOUT[] remains in the previous data output. It is called “read standby mode”. When OEN is high, DOUT[] is placed in a high-impedance state regardless of REN.

ARFRAM_HD Function Table

CK	WEN	WA	DI	RA	REN	OEN	DOUT	Comment
X	H	X	X	X	X	X	X	Write standby mode
↑	L	Valid	Valid	X	X	X	X	Write cycle starts
↓	L	X	X	X	X	X	X	Write cycle ends
X	X	X	X	X	X	H	Z	Unconditional tri-state output
X	X	X	X	X	H	L	DOUT(t-1)	Read standby mode
X	X	X	X	Toggle	L	L	MEM(RA)	Read cycle
X	X	X	X	Valid	↓	L	MEM(RA)	Read cycle with REN-controlled

Parameter Description

ARFRAM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y), Number of read ports(nr) and Number of write ports(nw).

Parameters		Ymux(y) = 2	Ymux(y) = 4	Ymux(y) = 8
Words (w)	Min	4	8	16
	Max	256	512	1024
	Step	2	4	8
Bpw (b)	Min	1	1	1
	Max	64	32	16
	Step	1	1	1
Write ports(nw)		1, 2		
Read ports(nr)		1, 2		

Pin Descriptions

Name	I/O	Description
CK<nw-1>	Write Clock	Write clock input on each write port. WEN, WA[] and DI[] are latched into the RAM on the rising edge of CK. If WEN is low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in write standby mode. At the falling edge of CK, the write-operation completes and the RAM is in a precharge state.
WEN<nw-1>	Write Enable	Write enable input on each write port. WEN is latched into the RAM on the rising edge of CK. When WEN is low, the write mode is enabled. When WEN is high, it prevents the write-operation. It is called “write standby mode”.
WA<nw-1> [ ]	Write Address	Write address bus on each write port. It specifies the location in which the data will be written in the write-operation. WA[] is latched at the rising edge of CK.
DI<nw-1> [ ]	Data Input	Data input bus on each write port. It contains data values to be written into the memory during the write-cycle. DI[] is latched at the rising edge of CK.
REN<nr-1>	Read Enable	Read enable input on each read port. When REN is low, read is enabled. When REN is high, read is disabled and DOUT[] remains in the previous state. It is called “read standby mode”
OEN<nr-1>	Data Output Enable	Output enable input on each read port. The low state enables output drivers and the high state disables output to go to the Hi-Z state.
RA<nr-1> [ ]	Read Address	Read address bus on each read port. It specifies the location to be read in the read-operation.
DOUT<nr-1> [ ]	Data Output	Data output bus on each read port. When REN and OEN are low, it presents the data word stored in the location specified by RA[]. When REN is high and OEN is low, DOUT[] remains in the previous state. When OEN is high, DOUT[] is in the high-impedance state regardless of REN.

ARFRAM_HD

High-Density Multi-Port Asynchronous Register File

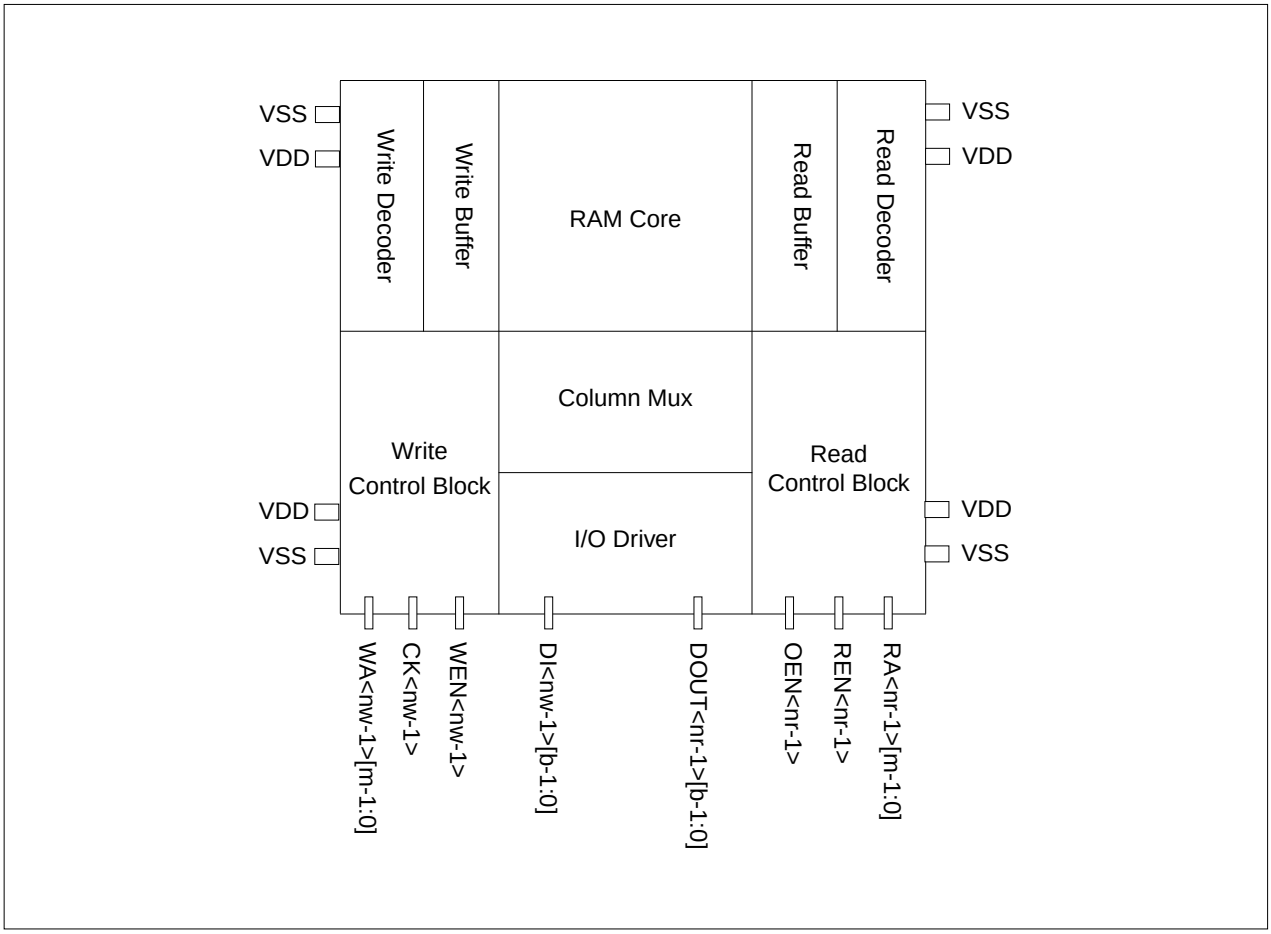
Pin Capacitance

(Unit = SL)

CK	WEN	DI	REN	OEN	WA	RA	DOUT
3.10	10.75	5.22	8.72	3.71	3.09	5.39	30.37

Block Diagrams

ARFRAM_HD supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



Application Notes

1. Permitting over-the-cell routing.
In ARFRAM_HD, the over-the-cell routing is permitted for Metal-4 or upper layers. Namely, while doing layout on the chip-level, any signals to be routed can be crossed over the area of register file generated by ARFRAM_HD compiler.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of ARFRAM_HD.

4. Contention mode under same addresses(RA[]=WA[] or WA0[] = WA1[]).
In ARFRAM_HD, simultaneous operations by both ports on the same address(RA[]=WA[] or WA0[] = WA1[]) such as read/write,write/read, write/write operation, cause a contention problem. Simultaneous operations are defined as the state in which both ports are enabled and both address buses are equal. ARFRAM_HD has no scheme preventing the contention mode. Due to the simultaneous operations, silicon will behave unpredictably. A write operation cannot completes and data appearing at outputs may not be valid.
Please refer to the timing diagrams if you want to avoid the contention mode between both ports.

5. Keeping the stable address cycle time in read mode.
In ARFRAM_HD, rather than the write operation which is synchronously performed by CK signal, the read operation is asynchronously performed whenever the address transition occures. So, in read mode if the another transition on the address occures after first transition within access time, read operation cannot completes. At that time, while in the read operation, the data stored in the memory may be corrupted due to the short transition. To prevent such fail, the stable read address cycle time (trcyc) is required. The essential requirement to recognize valid read address transition is that at least minimum address period should be equal or greater than tacc (access time).

6. Power reduction during standby mode.
ARFRAM_HD provides two types of standby modes – the write standby mode and the read standby mode. While in the write standby mode, WA[] and DI[] except CK are blocked even though the transitions of those signals occure. While in the read standby mode, RA[] is blocked even though its transition occures. So, you can reduce the power consumption in ARFRAM_HD by properly using two standby modes in your design.

Characteristics

Definition for AC Timing (ns)	
Symbol	**Description**
t_{wcyc}	Miminum write clock cycle time for write cycle
t_{ckl}	Mimimum CK pulse width low to guarantee write cycle
t_{ckh}	Mimimum CK pulse width high to guarantee write cycle
t_{was}	Write Address Setup time from WA[] to CK rise
t_{wah}	Write Address Hold time from CK rise to WA[]
t_{ws}	WEN Setup time from WEN fall to CK rise
t_{wh}	WEN Hold time from CK rise to WEN rise
t_{ds}	Data-in Setup time from DI[] to CK rise
t_{dh}	Data-in Hold time from CK rise to DI[]
t_{wwc}	Write-Write contention time from one CK to the other CK
t_{wda}	De-access time from CK rise to DOUT
t_{wacc}	Data Access time from CK fall
t_{rcyc}	Miminum RA[] Cycle time for read cycle
t_{acc}	Data ACCess time for read cycle
t_{ras}	Read Address Setup time from RA[] to REN rise
t_{rah}	Read Address Hold time from REN rise to RA[]
t_{da}	De-Access time from RA to DOUT
t_{zd}	DOUT high-Z to Drive time
t_{dz}	DOUT Drive to high-Z time
t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_w_standby	The write standby power consumption while WEN is high and other signals are in normal operations.
Power_r_standby	The read standby power consumption while REN is high, OEN is low and other signals are in normal operations.
Definition for Area (μm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

Reference Table

*** For Ymux=2(nr=1, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**32**	**64**	**128**	**256**
bpw	**8**	**16**	**32**	**64**
Timing (ns)				
t_{wcyc}	1.02	1.13	1.36	2.00
t_{ckl}	0.66	0.65	0.63	0.69
t_{ckh}	0.22	0.25	0.33	0.63
t_{was}	0.43	0.40	0.36	0.33
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.71	0.69	0.67	0.70
t_{wh}	0.30	0.30	0.30	0.30
t_{ds}	0.50	0.48	0.43	0.40
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.29	1.44	1.57	1.78
t_{wacc}	1.39	1.57	1.69	2.05
t_{rcyc}	1.44	1.61	1.81	2.29
t_{acc}	1.44	1.61	1.81	2.29
t_{ras}	0.25	0.25	0.25	0.25
t_{rah}	0.11	0.11	0.12	0.12
t_{da}	0.66	0.68	0.72	0.73
t_{zd}	0.21	0.22	0.26	0.28
t_{dz}	0.21	0.22	0.25	0.27
t_{od}	0.41	0.44	0.48	0.60
Power (µW/MHz)				
Power_read	14.68	29.55	78.20	174.39
Power_write	23.93	46.58	99.98	257.51
Power_w_standby	1.59	2.39	3.90	6.95
Power_r_standby	0.26	0.43	0.69	1.19
Area (µm)				
Width	174.54	256.82	408.58	708.18
Height	217.48	297.80	473.40	824.60

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=4(nr=1, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**64**	**128**	**256**	**512**
bpw	**4**	**8**	**16**	**32**
Timing (ns)				
t_{wcyc}	1.02	1.13	1.34	1.94
t_{ckl}	0.66	0.66	0.65	0.65
t_{ckh}	0.22	0.24	0.32	0.61
t_{was}	0.44	0.42	0.39	0.35
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.72	0.71	0.69	0.69
t_{wh}	0.30	0.30	0.30	0.30
t_{ds}	0.51	0.49	0.47	0.43
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.30	1.45	1.57	1.79
t_{wacc}	1.40	1.58	1.70	2.06
t_{rcyc}	1.45	1.62	1.82	2.31
t_{acc}	1.45	1.62	1.82	2.31
t_{ras}	0.25	0.25	0.25	0.25
t_{rah}	0.11	0.11	0.12	0.12
t_{da}	0.66	0.67	0.70	0.71
t_{zd}	0.20	0.21	0.24	0.25
t_{dz}	0.20	0.21	0.23	0.25
t_{od}	0.40	0.42	0.45	0.53
Power (µW/MHz)				
Power_read	12.79	25.31	69.17	154.65
Power_write	25.23	46.03	95.82	242.87
Power_w_standby	2.02	2.45	3.25	4.88
Power_r_standby	0.37	0.58	0.79	1.24
Area (µm)				
Width	174.54	256.82	408.58	708.18
Height	217.48	297.80	473.40	824.60

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=8(nr=1, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**128**	**256**	**512**	**1024**
bpw	**2**	**4**	**8**	**16**
Timing (ns)				
t_{wcyc}	1.04	1.13	1.34	1.91
t_{ckl}	0.67	0.66	0.66	0.66
t_{ckh}	0.23	0.23	0.30	0.57
t_{was}	0.44	0.43	0.41	0.38
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.72	0.72	0.70	0.71
t_{wh}	0.30	0.30	0.30	0.30
t_{ds}	0.52	0.50	0.48	0.46
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.33	1.48	1.60	1.82
t_{wacc}	1.42	1.60	1.72	2.09
t_{rcyc}	1.47	1.64	1.84	2.33
t_{acc}	1.47	1.64	1.84	2.33
t_{ras}	0.25	0.25	0.25	0.25
t_{rah}	0.11	0.11	0.12	0.12
t_{da}	0.66	0.68	0.70	0.71
t_{zd}	0.20	0.21	0.23	0.25
t_{dz}	0.20	0.21	0.22	0.24
t_{od}	0.40	0.41	0.44	0.50
Power (μW/MHz)				
Power_read	12.16	23.41	65.03	144.19
Power_write	27.86	47.98	96.95	239.34
Power_w_standby	2.62	2.88	3.33	4.23
Power_r_standby	0.49	0.72	0.94	1.45
Area (μm)				
Width	174.54	256.82	408.58	708.18
Height	217.48	297.80	473.40	824.60

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=2(nr=1, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**32**	**64**	**128**	**256**
bpw	**8**	**16**	**32**	**64**
Timing (ns)				
t_{wcyc}	1.11	1.27	1.61	2.59
t_{ckl}	0.36	0.37	0.52	1.09
t_{ckh}	0.20	0.24	0.34	0.73
t_{was}	0.55	0.52	0.48	0.43
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.84	0.83	0.82	0.85
t_{wh}	0.20	0.20	0.20	0.20
t_{ds}	0.63	0.60	0.55	0.51
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.20	0.24	0.34	0.73
t_{wda}	1.33	1.56	1.72	1.97
t_{wacc}	1.35	1.57	1.71	2.01
t_{rcyc}	1.44	1.61	1.81	2.29
t_{acc}	1.44	1.61	1.81	2.29
t_{ras}	0.25	0.25	0.25	0.25
t_{rah}	0.11	0.11	0.12	0.12
t_{da}	0.66	0.68	0.72	0.73
t_{zd}	0.21	0.22	0.26	0.28
t_{dz}	0.21	0.22	0.25	0.27
t_{od}	0.41	0.44	0.48	0.60
Power (µW/MHz)				
Power_read	14.68	29.55	78.20	174.39
Power_write	24.92	52.72	120.13	366.81
Power_w_standby	1.23	2.02	3.58	6.60
Power_r_standby	0.26	0.43	0.69	1.19
Area (µm)				
Width	264.44	392.38	672.52	1088.62
Height	208.86	297.80	469.42	824.78

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=4(nr=1, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**64**	**128**	**256**	**512**
bpw	**4**	**8**	**16**	**32**
Timing (ns)				
t_{wcyc}	1.11	1.28	1.61	2.58
t_{ckl}	0.37	0.37	0.52	1.09
t_{ckh}	0.21	0.25	0.34	0.70
t_{was}	0.56	0.54	0.51	0.47
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.85	0.84	0.84	0.85
t_{wh}	0.20	0.20	0.20	0.20
t_{ds}	0.63	0.62	0.59	0.55
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.21	0.25	0.34	0.70
t_{wda}	1.35	1.58	1.74	1.99
t_{wacc}	1.37	1.58	1.73	2.03
t_{rcyc}	1.45	1.62	1.82	2.31
t_{acc}	1.45	1.62	1.82	2.31
t_{ras}	0.25	0.25	0.25	0.25
t_{rah}	0.11	0.11	0.12	0.12
t_{da}	0.66	0.67	0.70	0.71
t_{zd}	0.20	0.21	0.24	0.25
t_{dz}	0.20	0.21	0.23	0.25
t_{od}	0.40	0.42	0.45	0.53
Power (µW/MHz)				
Power_read	12.79	25.31	69.17	154.65
Power_write	25.97	52.60	117.15	369.39
Power_w_standby	1.30	1.73	2.56	4.18
Power_r_standby	0.37	0.58	0.79	1.24
Area (µm)				
Width	264.44	392.38	672.52	1088.62
Height	208.86	297.80	469.42	824.78

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=8(nr=1, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**128**	**256**	**512**	**1024**
bpw	**2**	**4**	**8**	**16**
Timing (ns)				
t_{wcyc}	1.14	1.27	1.62	2.59
t_{ckl}	0.37	0.36	0.52	1.10
t_{ckh}	0.23	0.25	0.34	0.68
t_{was}	0.56	0.55	0.53	0.50
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.85	0.84	0.84	0.85
t_{wh}	0.20	0.20	0.20	0.20
t_{ds}	0.64	0.63	0.61	0.58
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.23	0.25	0.34	0.68
t_{wda}	1.39	1.62	1.77	2.03
t_{wacc}	1.40	1.61	1.76	2.06
t_{rcyc}	1.47	1.64	1.84	2.33
t_{acc}	1.47	1.64	1.84	2.33
t_{ras}	0.25	0.25	0.25	0.25
t_{rah}	0.11	0.11	0.12	0.12
t_{da}	0.66	0.68	0.70	0.71
t_{zd}	0.20	0.21	0.23	0.25
t_{dz}	0.20	0.21	0.22	0.24
t_{od}	0.40	0.41	0.44	0.50
Power (µW/MHz)				
Power_read	12.16	23.41	65.03	145.19
Power_write	28.53	50.52	116.46	369.94
Power_w_standby	1.52	1.77	2.24	3.16
Power_r_standby	0.49	0.72	0.94	1.45
Area (µm)				
Width	264.44	392.38	672.52	1088.62
Height	208.86	297.80	469.42	824.78

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=2(nr=2, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**32**	**64**	**128**	**256**
bpw	**8**	**16**	**32**	**64**
Timing (ns)				
t_{wcyc}	1.02	1.13	1.36	2.00
t_{ckl}	0.66	0.65	0.63	0.69
t_{ckh}	0.22	0.25	0.33	0.63
t_{was}	0.43	0.40	0.36	0.33
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.71	0.69	0.67	0.70
t_{wh}	0.30	0.30	0.30	0.30
t_{ds}	0.50	0.48	0.43	0.40
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.29	1.44	1.57	1.78
t_{wacc}	1.39	1.57	1.69	2.05
t_{rcyc}	1.37	1.56	1.80	2.42
t_{acc}	1.37	1.56	1.80	2.42
t_{ras}	0.23	0.22	0.22	0.22
t_{rah}	0.10	0.10	0.11	0.11
t_{da}	0.60	0.63	0.67	0.69
t_{zd}	0.21	0.23	0.26	0.27
t_{dz}	0.20	0.22	0.26	0.26
t_{od}	0.37	0.41	0.49	0.69
Power (μW/MHz)				
Power_read	14.00	27.99	76.25	177.26
Power_write	23.93	46.58	99.98	257.51
Power_w_standby	1.59	2.39	3.90	6.95
Power_r_standby	0.22	0.38	0.63	1.20
Area (μm)				
Width	252.61	377.28	597.42	1028.76
Height	227.48	310.36	504.38	892.42

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=4(nr=2, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**64**	**128**	**256**	**512**
bpw	**4**	**8**	**16**	**32**
Timing (ns)				
t_{wcyc}	1.02	1.13	1.34	1.94
t_{ckl}	0.66	0.66	0.65	0.65
t_{ckh}	0.22	0.24	0.32	0.61
t_{was}	0.44	0.42	0.39	0.35
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.72	0.71	0.69	0.69
t_{wh}	0.30	0.30	0.30	0.30
t_{ds}	0.51	0.49	0.47	0.43
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.30	1.45	1.57	1.79
t_{wacc}	1.40	1.58	1.70	2.06
t_{rcyc}	1.39	1.58	1.81	2.44
t_{acc}	1.39	1.58	1.81	2.44
t_{ras}	0.23	0.22	0.22	0.22
t_{rah}	0.10	0.10	0.11	0.11
t_{da}	0.60	0.62	0.66	0.69
t_{zd}	0.19	0.21	0.24	0.25
t_{dz}	0.19	0.20	0.23	0.24
t_{od}	0.35	0.38	0.43	0.56
Power (μW/MHz)				
Power_read	12.90	25.18	69.71	160.76
Power_write	25.23	46.03	95.82	242.87
Power_w_standby	2.02	2.45	3.25	4.88
Power_r_standby	0.31	0.50	0.79	1.21
Area (μm)				
Width	252.61	377.28	597.42	1028.76
Height	227.48	310.36	504.38	892.42

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=8(nr=2, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**128**	**256**	**512**	**1024**
bpw	**2**	**4**	**8**	**16**
Timing (ns)				
t_{wcyc}	1.04	1.13	1.34	1.91
t_{ckl}	0.67	0.66	0.66	0.66
t_{ckh}	0.23	0.23	0.30	0.57
t_{was}	0.44	0.43	0.41	0.38
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.72	0.72	0.70	0.71
t_{wh}	0.30	0.30	0.30	0.30
t_{ds}	0.52	0.50	0.48	0.46
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.33	1.48	1.60	1.82
t_{wacc}	1.42	1.60	1.72	2.09
t_{rcyc}	1.42	1.61	1.84	2.48
t_{acc}	1.42	1.61	1.84	2.48
t_{ras}	0.23	0.22	0.22	0.22
t_{rah}	0.10	0.10	0.11	0.11
t_{da}	0.60	0.62	0.65	0.69
t_{zd}	0.19	0.20	0.22	0.24
t_{dz}	0.18	0.20	0.22	0.23
t_{od}	0.35	0.36	0.40	0.49
Power (µW/MHz)				
Power_read	12.64	23.95	66.78	152.79
Power_write	27.86	47.98	96.95	239.34
Power_w_standby	2.62	2.88	3.33	4.23
Power_r_standby	0.41	0.61	0.93	1.41
Area (µm)				
Width	252.61	377.28	597.42	1028.76
Height	227.48	310.36	504.38	892.42

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=2(nr=2, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**32**	**64**	**128**	**256**
bpw	**8**	**16**	**32**	**64**
Timing (ns)				
t_{wcyc}	1.11	1.27	1.61	2.59
t_{ckl}	0.36	0.37	0.52	1.09
t_{ckh}	0.20	0.24	0.34	0.73
t_{was}	0.55	0.52	0.48	0.43
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.84	0.83	0.82	0.85
t_{wh}	0.20	0.20	0.20	0.20
t_{ds}	0.63	0.60	0.55	0.51
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.20	0.24	0.34	0.73
t_{wda}	1.33	1.56	1.72	1.97
t_{wacc}	1.35	1.57	1.71	2.01
t_{rcyc}	1.37	1.56	1.80	2.42
t_{acc}	1.37	1.56	1.80	2.42
t_{ras}	0.23	0.22	0.22	0.22
t_{rah}	0.10	0.10	0.11	0.11
t_{da}	0.60	0.62	0.67	0.69
t_{zd}	0.21	0.23	0.26	0.27
t_{dz}	0.20	0.22	0.26	0.26
t_{od}	0.37	0.41	0.49	0.69
Power (µW/MHz)				
Power_read	14.00	27.99	76.25	177.26
Power_write	24.92	52.6472	120.13	366.81
Power_w_standby	1.23	2.02	3.58	6.60
Power_r_standby	0.22	0.38	0.63	1.20
Area (µm)				
Width	314.59	468.34	736.90	1262.10
Height	229.56	312.44	498.64	871.04

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=4(nr=2, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**64**	**128**	**256**	**512**
bpw	**4**	**8**	**16**	**32**
Timing (ns)				
t_{wcyc}	1.11	1.28	1.61	2.58
t_{ckl}	0.37	0.37	0.52	1.09
t_{ckh}	0.21	0.25	0.34	0.70
t_{was}	0.56	0.54	0.51	0.47
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.85	0.84	0.84	0.85
t_{wh}	0.20	0.20	0.20	0.20
t_{ds}	0.63	0.62	0.59	0.55
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.21	0.25	0.34	0.70
t_{wda}	1.35	1.58	1.74	1.99
t_{wacc}	1.37	1.58	1.73	2.03
t_{rcyc}	1.39	1.58	1.81	2.44
t_{acc}	1.39	1.58	1.81	2.44
t_{ras}	0.23	0.22	0.22	0.22
t_{rah}	0.10	0.10	0.11	0.11
t_{da}	0.60	0.62	0.66	0.69
t_{zd}	0.19	0.21	0.24	0.25
t_{dz}	0.19	0.20	0.23	0.24
t_{od}	0.35	0.38	0.43	0.56
Power (µW/MHz)				
Power_read	12.90	25.18	69.76	160.76
Power_write	25.97	52.60	117.15	369.39
Power_w_standby	1.30	1.73	2.56	4.18
Power_r_standby	0.31	0.50	0.79	1.21
Area (µm)				
Width	314.59	468.34	736.90	1262.10
Height	229.56	312.44	498.64	871.04

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

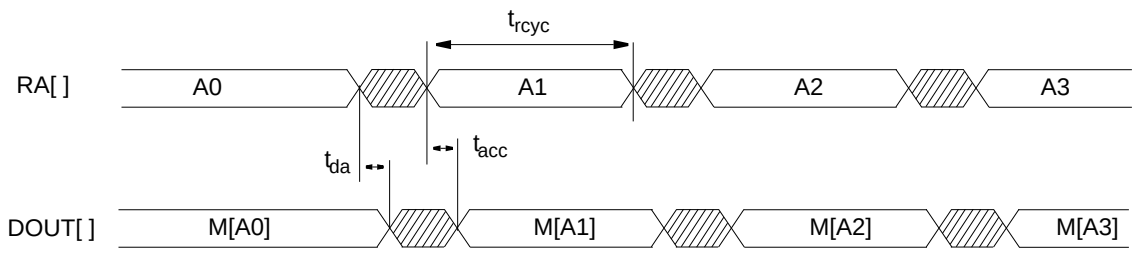
*** For Ymux=8(nr=2, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**128**	**256**	**512**	**1024**
bpw	**2**	**4**	**8**	**16**
Timing (ns)				
t_{wcyc}	1.14	1.27	1.62	2.59
t_{ckl}	0.37	0.36	0.52	1.10
t_{ckh}	0.23	0.25	0.34	0.68
t_{was}	0.56	0.55	0.53	0.50
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.85	0.84	0.84	0.85
t_{wh}	0.20	0.20	0.20	0.20
t_{ds}	0.64	0.63	0.61	0.58
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.23	0.25	0.34	0.68
t_{wda}	1.39	1.62	1.77	2.03
t_{wacc}	1.40	1.61	1.76	2.06
t_{rcyc}	1.42	1.61	1.84	2.48
t_{acc}	1.42	1.61	1.84	2.48
t_{ras}	0.23	0.22	0.22	0.22
t_{rah}	0.10	0.10	0.11	0.11
t_{da}	0.60	0.62	0.65	0.69
t_{zd}	0.19	0.20	0.22	0.24
t_{dz}	0.18	0.20	0.22	0.23
t_{od}	0.35	0.36	0.40	0.49
Power (µW/MHz)				
Power_read	12.64	23.95	66.78	152.79
Power_write	28.53	50.52	116.46	369.94
Power_w_standby	1.52	1.77	2.24	3.16
Power_r_standby	0.41	0.61	0.93	1.41
Area (µm)				
Width	314.59	468.34	736.90	1262.10
Height	229.56	312.44	498.64	871.04

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

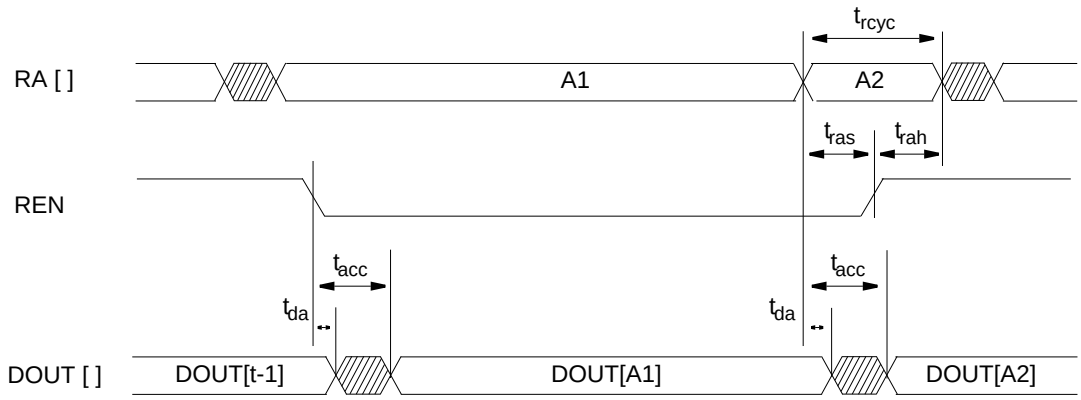
Timing Diagrams

Read Cycle



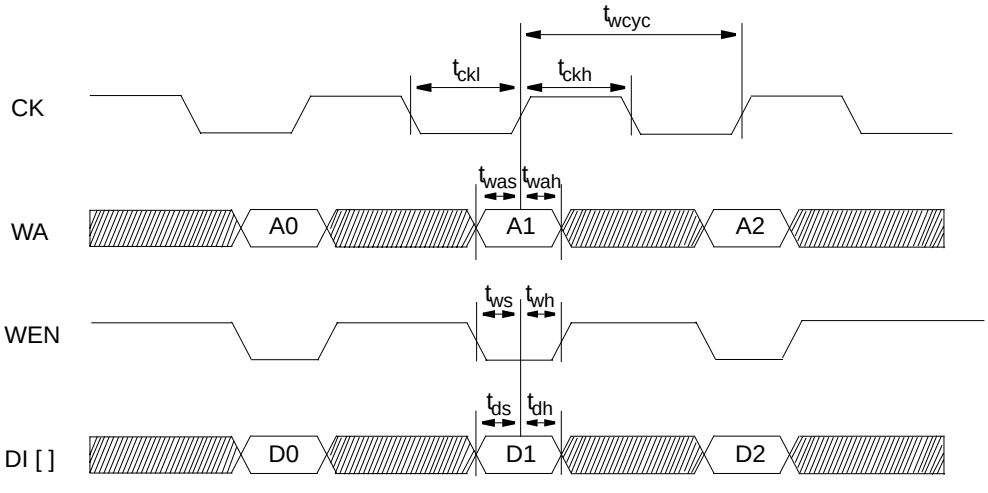
(OEN = low, REN= low, CK, WEN, DI[ ], WA[ ]= don't care)

Read Cycle with REN-Controlled



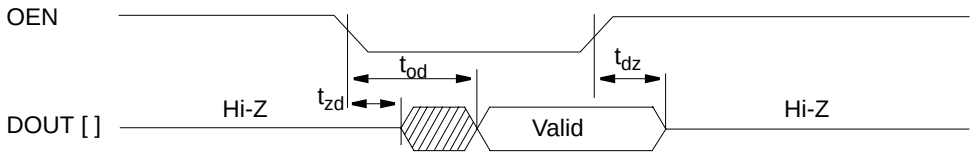
(OEN = low, CK, WEN, DI[ ], WA[ ] = don't care)

Write Cycle



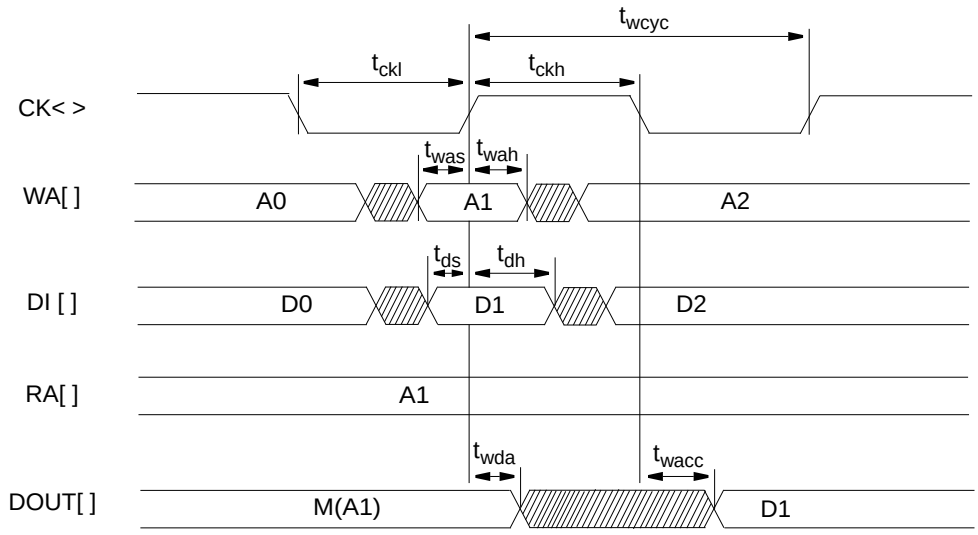
(REN, OEN, RA[ ] = don't care)

OEN Controlled Output Enable



(CK, REN, WEN, DI[ ], WA[ ], RA[ ] = don't care)

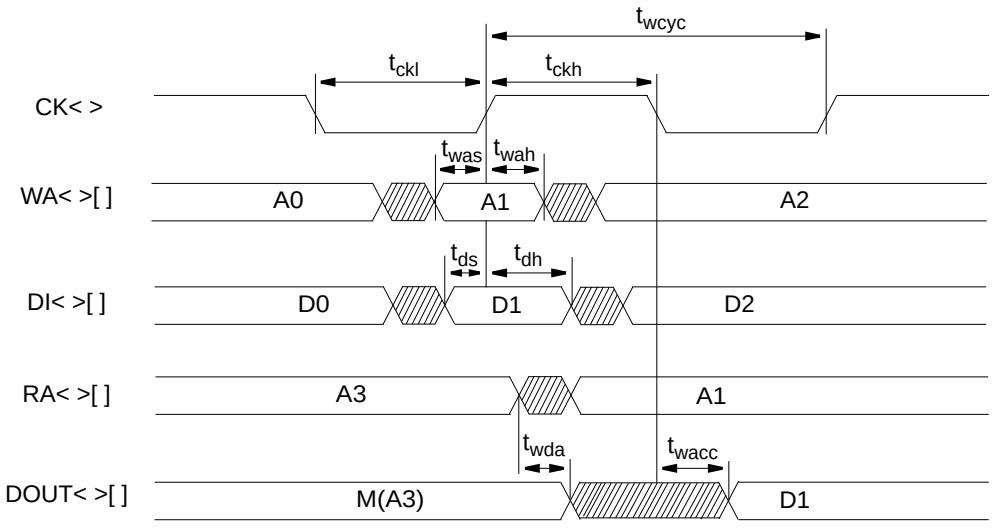
Read-Write Contention



(WA[ ] = RA[ ]; WEN, REN, OEN = low)

NOTE: If CK rise while WA[] is same as RA[], it is a read-write contention. While CK is high, DOUT[] is UNKNOWN and write data is valid. After twacc from the falling edge of CK, the read data (D1) is valid.

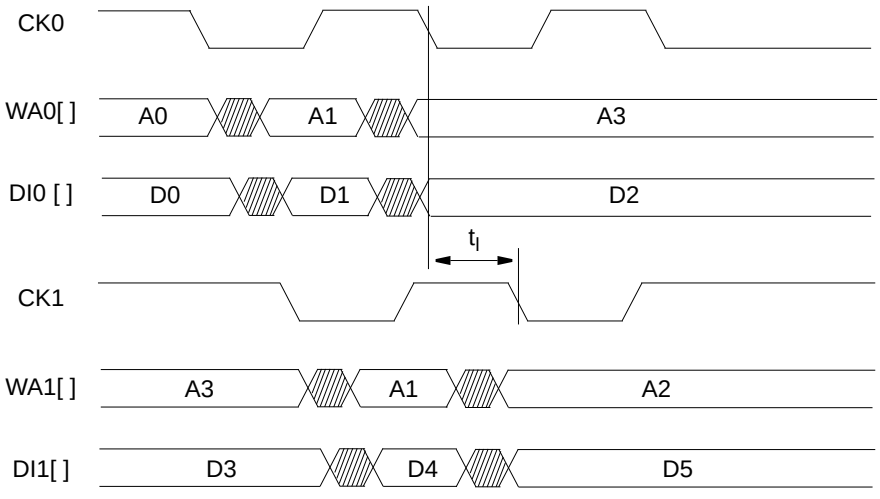
Write-Read Contention



(WA[ ] = RA[ ]; WEN, REN, OEN = low)

NOTE: While CK is high, if read access begins by RA<>[] which is same as WA<>[] latched at the rising edge of CK, it is Write-Read Contention. The read data is invalid whereas the write is still valid. After twacc from the falling edge of CK, DOUT[] is valid.

Write-Write Contention



(WA0[ ] = WA1[ ]; WEN0, WEN1 = low, OEN, REN, RA[ ] = don't care)

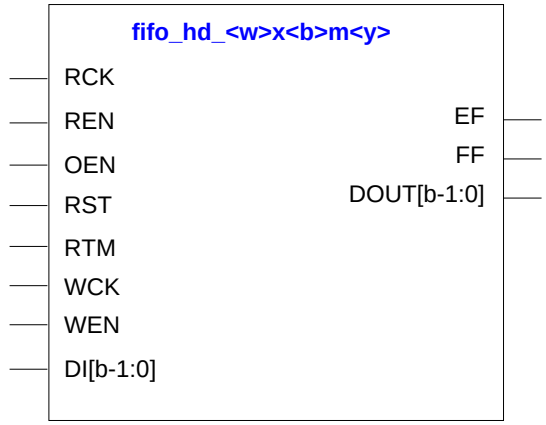
NOTES:

1. If addresses latched at the rising edge of CK are same and t1 is smaller than or equal to twwc, it is Write-Write Contention. The data stored at current address will be unpredictable.
2. "don't care" means the condition that these pins are in normal operation mode.

FIFO_HD

High-Density Synchronous First-In First-Out Memory

Logic Symbol



NOTES:
1. Words(w) is the number of words in FIFO_HD
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.

Features

- Suitable for high-density applications
- Over-read and over-write protection capability
- Retransmit capability
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched full and empty status flag output
- Automatic power-down
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 64 number of bits per word

Function Description

FIFO_HD is a synchronous first-in first-out buffer memory which is provided as a compiler. FIFO_HD is intended for use in high-density applications. After valid reset, on the rising of WCK, the write cycle is initiated when WEN is low, RST is high and FF is low. The data on DI[] is written into the memory location specified by the write pointer. During normal write operation, the rising edge of WCK will reset EF if it is set. At the last available memory location, write operation will set FF. DI[] and WEN must satisfy the setup and hold requirements with respect to the rising edge of WCK.

On the rising edge of RCK, the read cycle is initiated when REN is low, RST is high, RTM is high and EF is low. The data located in the memory specified by the read pointer comes in DOUT[] after some delay. During normal read operation, the rising edge of RCK will reset FF if it is set. At the last available memory location with available data, read operation will set EF. A valid DOUT[] will be possibly in some specified time after the rising edge of RCK, under that OEN is low. And the output data will remain unchanged until the next read, reset, or retransmit mode come in. REN must satisfy the setup and hold requirements with respect to the rising edge of RCK. When OEN is high, DOUT[] is placed in a high-impedance state.

In reset mode, a reset is globally initiated at the falling edge of RST. The reset operation will set EF and reset FF and make the data output zero.The reset operation will initiate the read pointer and the write pointer as 0. After reset operation, the status of EF will make RCK inoperable. The valid write input signal will become operable as RST is high. The read input signal will remain inoperable until EF is reset by the first valid write.

In retransmit mode, a retransmit is initiated at the falling edge of RTM only if the total number of writes after a reset operation is less than the word size of the memory in FIFO_HD and more than 0 (0 < total number of write < W-1). The retransmit operation will initiate the read pointer as 0 to allow the retransmission of data, make DOUT[] zero and make EF reset if it is set. The valid read input signal will become operable as RTM is high.

FIFO_HD Function Table

RST	WEN	WCK	REN	RCK	RTM	OEM	EF	FF	DI	DOUT	Comment
↓	X	X	X	X	X	X	↑	↓	X	L	Reset mode
H	X	X	X	X	↓	X	↓	X	X	L	Retransmit mode
H	X	X	L	↑	H	L	L	↓	X	DOUT(t)	Read mode
H	L	↑	X	X	X	X	↓	L	Valid	DOUT(t-1)	Write mode
H	X	X	L	↑	H	L	↑	L	X	DOUT(t)	Read and empty mode
H	L	↑	X	X	X	X	L	↑	Valid	DOUT(t-1)	Write and full mode
H	X	X	H	↑	H	L	X	X	X	DOUT(t-1)	(Note 1)
H	X	X	L	↑	H	L	H	X	X	DOUT(t-1)	(Note 2)
X	X	X	X	X	X	H	X	X	X	Hi-Z	(Note 3)
H	H	↑	X	X	X	X	X	X	Valid	DOUT(t-1)	(Note 4)
H	L	↑	X	X	X	X	X	H	Valid	DOUT(t-1)	(Note 5)

NOTES:

1. Read is blocked when REN is high and the read port is in disable mode.
2. Read is blocked when EF is high (overread protection).
3. Under that OEN is high, DOUT[] goes to tri-state output mode.
4. Write is blocked when WEN is high and the write port is in disable mode.
5. Write is blocked when FF is high (overwrite protection).

Parameter Description

FIFO_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 2	Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16
Words (w)	Min	16	32	64	128
	Max	1024	2048	4096	8192
	Step	w ⇐ 128:16	w ⇐ 256:32	w ⇐ 512:64	w ⇐ 1024:128
		w > 128:128	w > 256:256	w > 512:512	w > 1024:1024
Bpw (b)	Min	2	2	2	2
	Max	64	32	16	8
	Step	1	1	1	1

FIFO_HD

High-Density Synchronous First-In First-Out Memory

Pin Descriptions

Name	I/O	Description
RCK	Read Clock	Read Clock input. Upon the rising edge of RCK, it begins a read operation when REN is low, RST is high, RTM is high and EF is low.
REN	Read Enable	Read Enable input. When REN is low, the read access occurs properly. Conversely when REN is high, no read access can occur and the read port of the FIFO_HD goes to power down mode. REN is latched at the rising edge of RCK.
OEN	Data Output Enable	Output Enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
RST	Reset	Reset input. Upon the falling edge of RST, the reset mode is initiated. RST resets the read and write pointer to their initial position. RST sets EF and resets FF. RST makes DOUT[] zero.
RTM	Retransmit	Retransmit input. Upon the falling edge of RTM, the retransmit mode is initiated, provided that RST is high. RTM resets the read pointer to its initial position. RTM makes DOUT[] zero.
WCK	Write Clock	Write Clock input. Upon the rising edge of WCK, it begins a write operation when WE is low, RST is high and FF is low.
WEN	Write Enable	Write Enable input. When WEN is low, a write access occurs properly. Conversely when WEN is high, no write access can occur and the write port of the FIFO_HD goes to power down mode. WEN is latched at the rising edge of WCK.
DI	Data In	Data input bus. DI[] is latched on the rising edge of WCK. Data input is written into the addressed location in write mode.
EF	Empty Flag	Empty Flag. If the memory has no data to be read, EF goes high. Valid reset makes EF high and valid retransmit makes it low.
FF	Full Flag	Full Flag. If the memory has no vacancy to write data, FF goes high. Valid reset makes FF low.
DOUT	Data Output	Data output bus. Data output is valid after the rising edge of RCK while the FIFO_HD is in read mode when OEN is low. Conversely when OEN is high, DOUT[] goes to high-impedance state. By reset or retransmit operation. DOUT[] goes to 0.

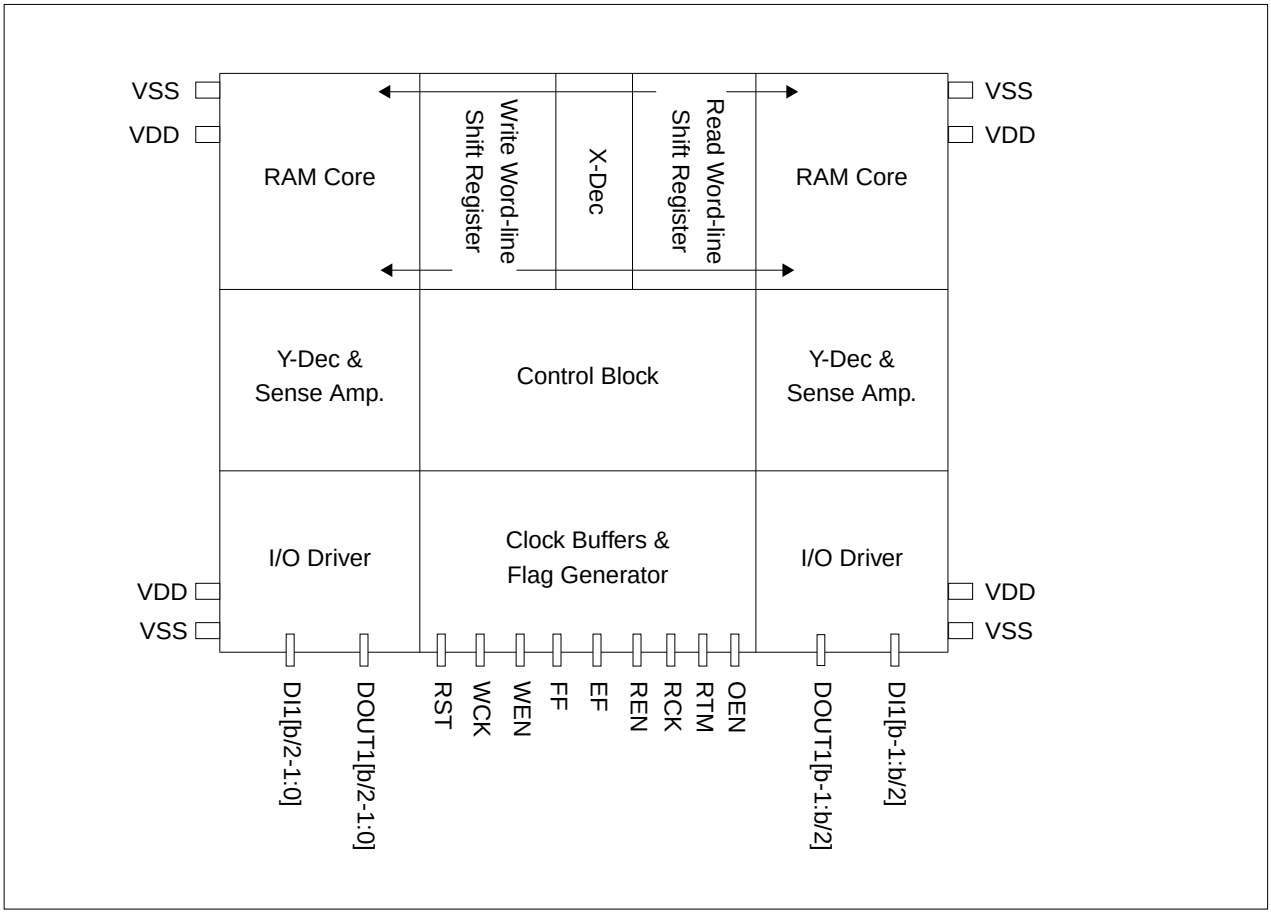
Pin Capacitance

(Unit = SL)

RST	RTM	WCK	RCK	OEN	WEN	REN	DI	DOUT
6.9826	3.0174	16.9246	9.4197	5.2998	3.4236	3.5010	2.538	7.6015

Block Diagrams

FIFO_HD supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in FIFO_HD is permitted for Metal-5 layer and Metal-6 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of FIFO_HD.
4. FIFO_HD must be reset before any operation performed. The reset operation initiates the read pointer and the write pointer as 0.
5. FIFO_HD should be reset again before resuming normal operation if abnormal operation is performed. Abnormal operations are invalid retransmit attemption, and read/write operation causing the timing requirement violations.
6. The retransmit operation initiates the read pointer as 0.
7. The retransmit is useful only when the total number of writes after a reset is less than the total word capacity of the FIFO_HD and more than 0.
8. Outputs are not changed until first valid read after a reset or retransmit.

Characteristics

Definition for AC Timing (ns)		
Symbol	**Description**	**Unit**
t_{rst}	Min RST pulse width low	ns
t_{rtm}	Min RTM pulse width low	ns
t_{rcyc}	Read clock cycle time	ns
t_{rckh}	Read clock pulse width high	ns
t_{rckl}	Read clock pulse width low	ns
t_{wcyc}	Write clock cycle time	ns
t_{wckh}	Write clock pulse width high	ns
t_{wckl}	Write clock pulse width low	ns
t_{rs}	REN setup to RCK rising	ns
t_{rh}	REN hold from RCK rising	ns
t_{ws}	WEN setup to WCK rising	ns
t_{wh}	WEN hold from WCK rising	ns
t_{wrcs}	WCK setup to RCK rising	ns
t_{rwcs}	RCK setup to WCK rising	ns
t_{ds}	DI setup to WCK rising	ns
t_{dh}	DI hold from WCK rising	ns
t_{rstw}	RST setup to WCK rising	ns
t_{rtmr}	RTM setup to RCK rising	ns
t_{rste}	Delay from RST falling to EF rising	ns
t_{rstf}	Delay from RST falling to FF falling	ns
t_{rstd}	Delay from RST falling to DOUT zero	ns
t_{rstda}	Output hold time from RST falling to DOUT	ns
t_{rtme}	Delay from RTM falling to EF falling	ns
t_{rtmd}	Delay from RTM falling to DOUT zero	ns
t_{rtmda}	Output hold time from RTM falling to DOUT	ns
t_{we}	Delay from WCK rising to EF falling	ns
t_{wf}	Delay from WCK rising to FF rising	ns
t_{rf}	Delay from RCK rising to FF falling	ns
t_{re}	Delay from RCK rising to EF rising	ns
t_{acc}	Data access time	ns
t_{da}	De-access time	ns
t_{dz}	DOUT drive to high-Z time	ns
t_{zd}	DOUT high-Z to drive time	ns
t_{od}	OEN to valid output time	ns
Definition for Power Consumption (µW/MHz)		
Power_read	The dynamic average power consumption while in a read cycle	µW/MHz
Power_write	The dynamic average power consumption while in a write cycle	µW/MHz
Power_w_standby	The write standby power consumption while WEN is high	µW/MHz
Power_r_standby	The read standby power consumption while REN is high	µW/MHz
Definition for Area (µm)		
Width	The physical width in X-direction	µm
Height	The physical height in Y-direction	µm

FIFO_HD

High-Density Synchronous First-In First-Out Memory

Reference Table

*** For Ymux=2** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters				
words	**64**	**128**	**384**	**1024**
bpw	**16**	**32**	**48**	**64**
Timing (ns)				
t_{rst}	3.13	3.13	3.14	3.63
t_{rtm}	3.03	3.03	3.04	3.53
t_{rcyc}	2.09	2.12	2.15	2.54
t_{rckl}	0.48	0.48	0.48	0.48
t_{rckh}	0.27	0.27	0.27	0.27
t_{wcyc}	1.85	1.90	1.94	2.34
t_{wckl}	0.59	0.61	0.64	0.67
t_{wckh}	0.48	0.51	0.54	0.57
t_{rs}	0.60	0.60	0.60	0.60
t_{rh}	0.01	0.01	0.01	0.01
t_{ws}	0.62	0.62	0.62	0.62
t_{wh}	0.01	0.01	0.01	0.01
t_{ds}	0.66	0.64	0.62	0.60
t_{dh}	0.01	0.01	0.01	0.01
t_{rstw}	0.36	0.36	0.36	0.36
t_{rtmr}	0.36	0.36	0.36	0.36
t_{wrcs}	0.94	0.94	0.94	0.94
t_{rwcs}	1.02	1.02	1.02	1.40
t_{rstd}	2.30	2.33	2.36	2.87
t_{rstda}	0.43	0.45	0.47	0.48
t_{rste}	3.08	3.08	3.09	3.58
t_{rstf}	3.08	3.08	3.09	3.58
t_{rtmd}	2.31	2.34	2.36	2.87
t_{rtmda}	0.44	0.46	0.48	0.49
t_{rtme}	2.85	2.85	2.86	3.35
t_{we}	0.63	0.63	0.63	0.63
t_{wf}	1.32	1.32	1.32	1.32
t_{re}	1.27	1.27	1.27	1.27
t_{rf}	0.68	0.68	0.68	0.68
t_{acc}	1.69	1.72	1.75	2.14
t_{da}	1.35	1.37	1.39	1.77
t_{dz}	0.22	0.23	0.25	0.26
t_{zd}	0.26	0.28	0.30	0.31
t_{od}	0.44	0.47	0.49	0.51
Power (µW/MHz)				
Power_read	61.43	99.25	139.12	190.99
Power_write	60.64	99.63	149.15	234.07
Power_w_standby	3.15	5.70	8.19	10.73
Power_r_standby	0.80	0.84	0.89	0.99
Area (µm)				
Width	459.54	632.34	805.14	977.94
Height	242.08	288.16	476.68	947.98

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters				
words	**128**	**256**	**768**	**2048**
bpw	**8**	**16**	**24**	**32**
Timing (ns)				
t_{rst}	3.13	3.13	3.14	3.63
t_{rtm}	3.03	3.03	3.04	3.53
t_{rcyc}	2.11	2.13	2.16	2.55
t_{rckl}	0.48	0.48	0.48	0.48
t_{rckh}	0.27	0.27	0.27	0.27
t_{wcyc}	1.85	1.90	1.94	2.34
t_{wckl}	0.58	0.60	0.62	0.64
t_{wckh}	0.48	0.50	0.52	0.54
t_{rs}	0.60	0.60	0.60	0.60
t_{rh}	0.01	0.01	0.01	0.01
t_{ws}	0.62	0.62	0.62	0.62
t_{wh}	0.01	0.01	0.01	0.01
t_{ds}	0.67	0.65	0.64	0.63
t_{dh}	0.01	0.01	0.01	0.01
t_{rstw}	0.36	0.36	0.36	0.36
t_{rtmr}	0.36	0.36	0.36	0.36
t_{wrcs}	0.94	0.94	0.94	0.94
t_{rwcs}	1.02	1.02	1.03	1.40
t_{rstd}	2.35	2.37	2.38	2.89
t_{rstda}	0.42	0.44	0.45	0.46
t_{rste}	3.08	3.08	3.09	3.58
t_{rstf}	3.08	3.08	3.09	3.58
t_{rtmd}	2.36	2.37	2.36	2.90
t_{rtmda}	0.44	0.45	0.46	0.47
t_{rtme}	2.85	2.85	2.86	3.35
t_{we}	0.63	0.63	0.63	0.63
t_{wf}	1.32	1.32	1.31	1.32
t_{re}	1.27	1.27	1.27	1.27
t_{rf}	0.68	0.68	0.68	0.68
t_{acc}	1.71	1.73	1.76	2.15
t_{da}	1.35	1.37	1.39	1.77
t_{dz}	0.21	0.23	0.23	0.24
t_{zd}	0.26	0.27	0.28	0.29
t_{od}	0.43	0.45	0.47	0.48
Power (µW/MHz)				
Power_read	56.52	90.41	126.98	174.06
Power_write	53.77	86.90	130.20	208.91
Power_w_standby	1.91	3.25	4.49	5.77
Power_r_standby	0.78	0.81	0.84	0.91
Area (µm)				
Width	459.54	632.34	805.14	977.94
Height	242.08	288.16	476.68	947.98

FIFO_HD

High-Density Synchronous First-In First-Out Memory

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	**256**	**512**	**1536**	**4096**
bpw	**4**	**8**	**12**	**16**
Timing (ns)				
t_{rst}	3.13	3.13	3.14	3.63
t_{rtm}	3.03	3.03	3.04	3.53
t_{rcyc}	2.13	2.16	2.19	2.58
t_{rckl}	0.48	0.48	0.48	0.48
t_{rckh}	0.27	0.27	0.27	0.27
t_{wcyc}	1.85	1.90	1.94	2.34
t_{wckl}	0.57	0.59	0.60	0.62
t_{wckh}	0.48	0.50	0.51	0.53
t_{rs}	0.60	0.60	0.60	0.60
t_{rh}	0.01	0.01	0.01	0.01
t_{ws}	0.62	0.62	0.62	0.62
t_{wh}	0.01	0.01	0.01	0.01
t_{ds}	0.68	0.66	0.65	0.64
t_{dh}	0.01	0.01	0.01	0.01
t_{rstw}	0.36	0.36	0.36	0.36
t_{rtmr}	0.36	0.36	0.36	0.36
t_{wrcs}	0.94	0.94	0.94	0.94
t_{rwcs}	1.02	1.02	1.02	1.40
t_{rstd}	2.44	2.45	2.47	2.97
t_{rstda}	0.42	0.43	0.44	0.45
t_{rste}	3.08	3.08	3.09	3.58
t_{rstf}	3.08	3.08	3.09	3.58
t_{rtmd}	2.45	2.46	2.48	2.98
t_{rtmda}	0.43	0.45	0.46	0.47
t_{rtme}	2.85	2.85	2.86	3.35
t_{we}	0.63	0.63	0.63	0.63
t_{wf}	1.32	1.32	1.32	1.32
t_{re}	1.27	1.27	1.27	1.27
t_{rf}	0.68	0.68	0.68	0.68
t_{acc}	1.73	1.76	1.79	2.18
t_{da}	1.35	1.37	1.39	1.77
t_{dz}	0.21	0.22	0.23	0.24
t_{zd}	0.26	0.27	0.28	0.29
t_{od}	0.43	0.45	0.46	0.47
Power (µW/MHz)				
Power_read	53.89	86.02	119.86	165.72
Power_write	50.16	80.44	120.69	196.33
Power_w_standby	1.26	2.00	2.64	3.29
Power_r_standby	0.77	0.79	0.82	0.86
Area (µm)				
Width	459.54	632.34	805.14	977.94
Height	242.08	288.16	476.68	947.98

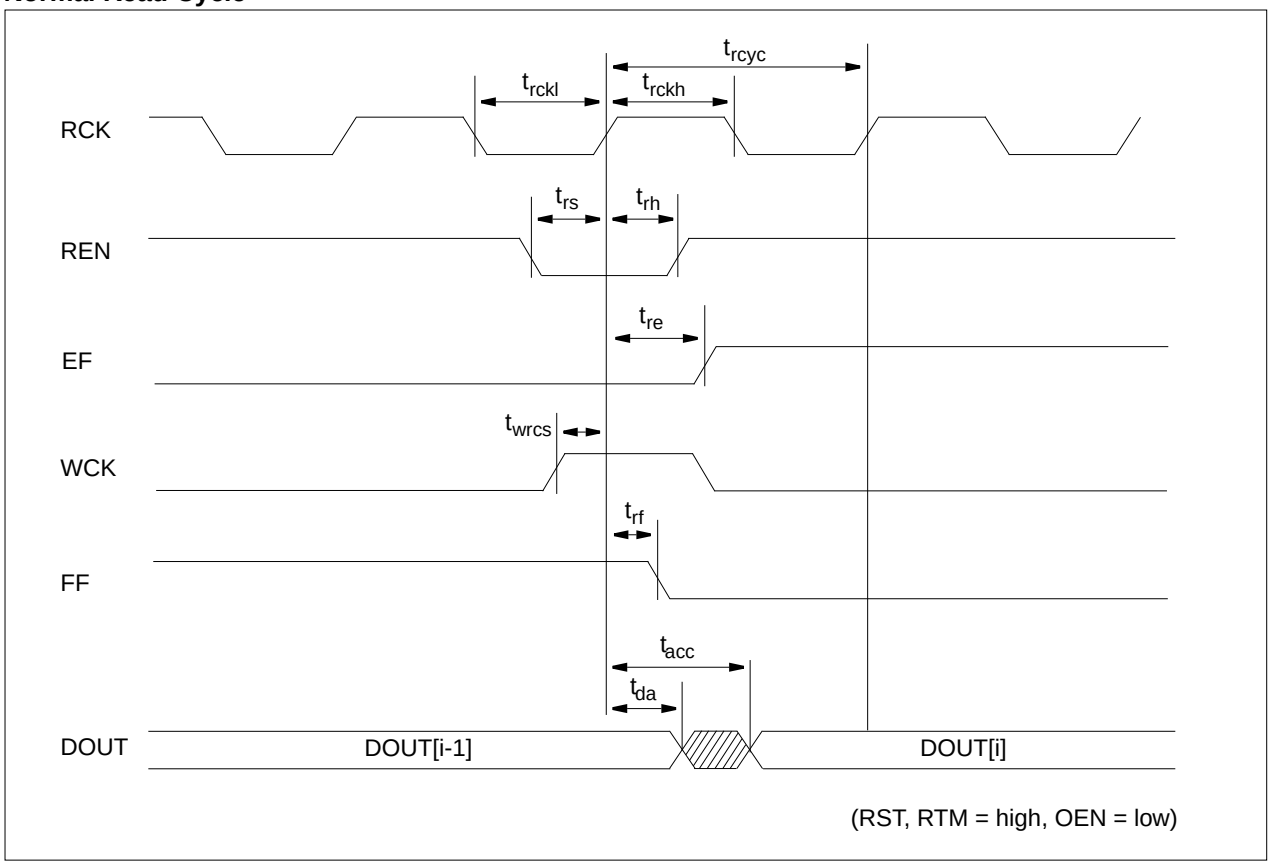
Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	**512**	**1024**	**3072**	**8192**
bpw	**2**	**4**	**6**	**8**
Timing (ns)				
t_{rst}	3.13	3.13	3.14	3.63
t_{rtm}	3.03	3.03	3.04	3.53
t_{rcyc}	2.18	2.20	2.23	2.62
t_{rckl}	0.48	0.48	0.48	0.48
t_{rckh}	0.27	0.27	0.27	0.27
t_{wcyc}	1.86	1.90	1.94	2.34
t_{wckl}	0.57	0.58	0.60	0.61
t_{wckh}	0.50	0.51	0.53	0.54
t_{rs}	0.60	0.60	0.60	0.60
t_{rh}	0.01	0.01	0.01	0.01
t_{ws}	0.62	0.62	0.62	0.62
t_{wh}	0.01	0.01	0.01	0.01
t_{ds}	0.68	0.66	0.65	0.65
t_{dh}	0.01	0.01	0.01	0.01
t_{rstw}	0.36	0.36	0.36	0.36
t_{rtmr}	0.36	0.36	0.36	0.36
t_{wrcs}	0.94	0.94	0.94	0.94
t_{rwcs}	1.02	1.02	1.02	1.40
t_{rstd}	2.62	2.63	2.64	3.15
t_{rstda}	0.42	0.43	0.44	0.45
t_{rste}	3.08	3.08	3.09	3.58
t_{rstf}	3.08	3.08	3.09	3.58
t_{rtmd}	2.63	2.64	2.65	3.16
t_{rtmda}	0.43	0.44	0.45	0.46
t_{rtme}	2.85	2.85	2.86	3.35
t_{we}	0.63	0.63	0.63	0.63
t_{wf}	1.32	1.32	1.32	1.32
t_{re}	1.27	1.27	1.27	1.27
t_{rf}	0.68	0.68	0.68	0.68
t_{acc}	1.78	1.80	1.83	2.22
t_{da}	1.36	1.37	1.39	1.77
t_{dz}	0.21	0.22	0.23	0.23
t_{zd}	0.26	0.27	0.27	0.28
t_{od}	0.43	0.44	0.45	0.46
Power (µW/MHz)				
Power_read	52.35	83.71	116.62	161.43
Power_write	47.58	77.30	116.00	190.23
Power_w_standby	0.77	1.38	1.71	2.07
Power_r_standby	0.77	0.77	0.80	0.85
Area (µm)				
Width	459.54	632.34	805.14	977.94
Height	242.08	288.16	476.68	947.98

Timing Diagrams

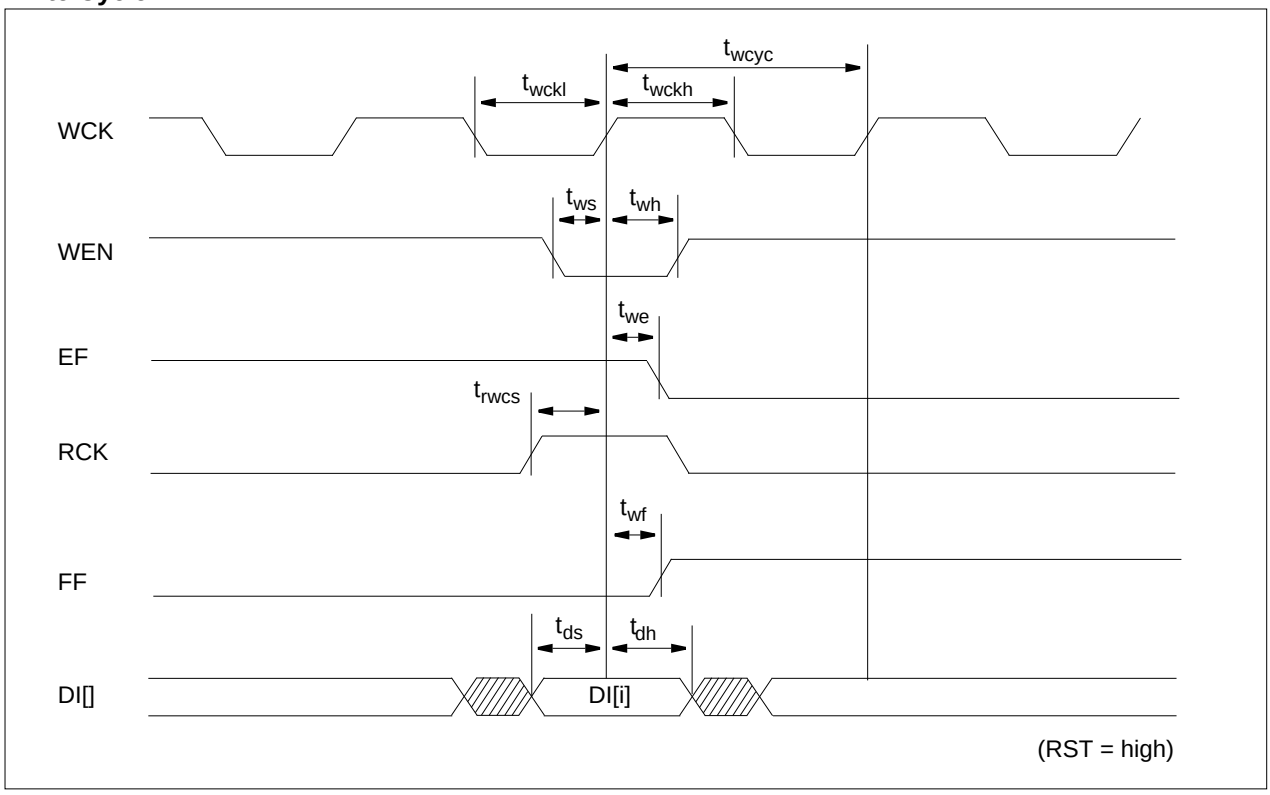
Normal Read Cycle



NOTES:

1. Read cycle is blocked during empty state (over-read protected)
2. t_{wrcs} is the timing related between first write on empty state and first subsequent read. If it is not satisfied, DOUT[i] will be unpredictable.
3. The is the timing related the read and empty mode.

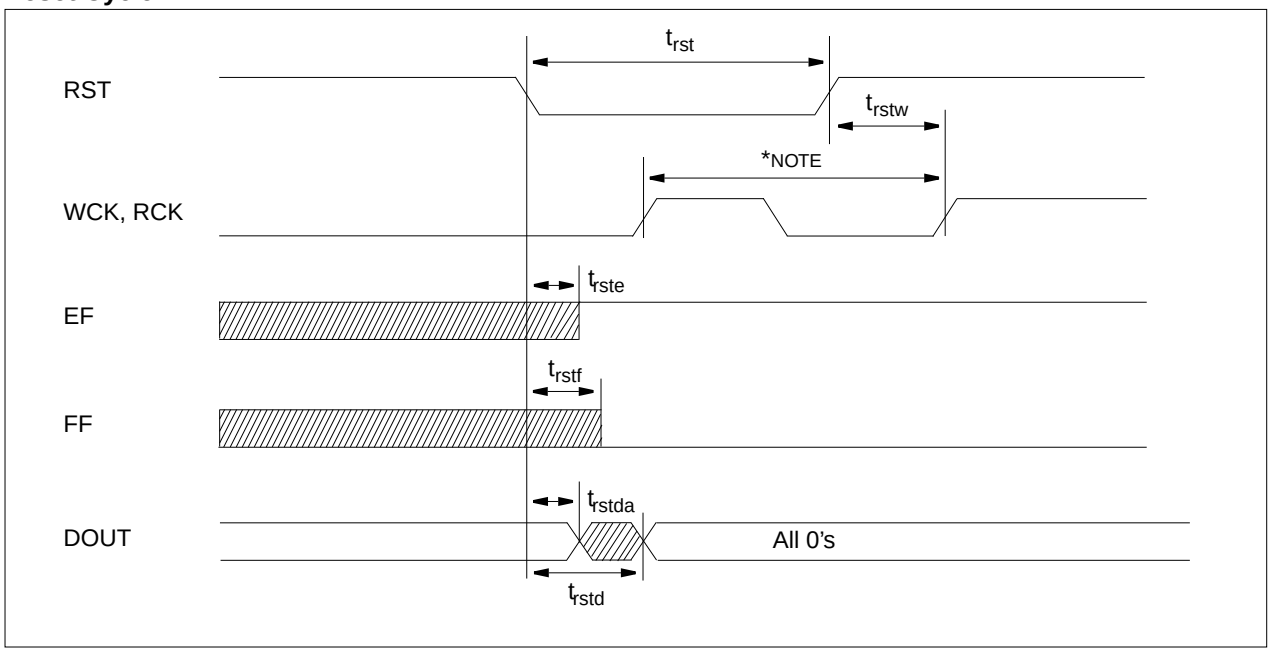
Write Cycle



NOTES:

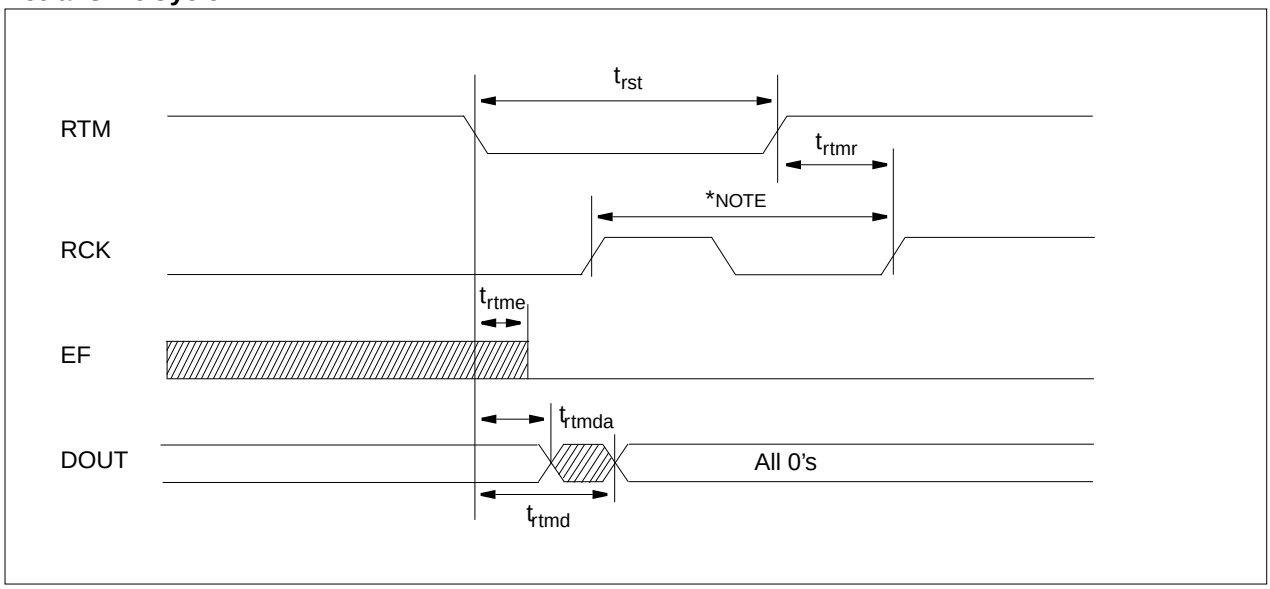
1. Write cycle is blocked during full state (over-write protected)
2. t_{rwcs} is the timing related between first read on full state and first subsequent write. If it is not satisfied, DOUT[i] (not shown) will be unpredictable.
3. t_{wf} is the timing related the write and full mode.

Reset Cycle



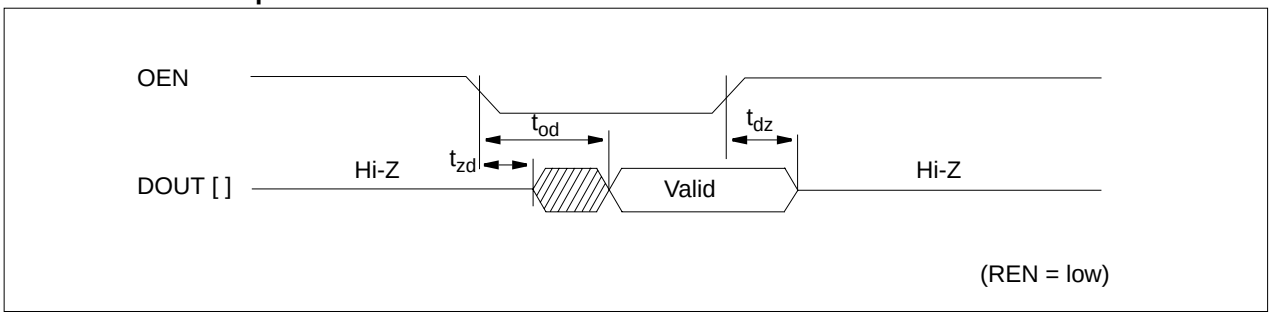
NOTE: Read cycle and write cycle are blocked when RST is low.

Retransmit Cycle

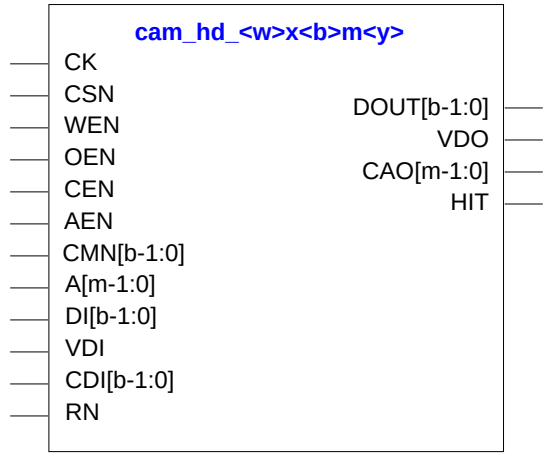


NOTE: Read cycle is blocked when RTM is low.

OEN Controlled Output Enable



Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Single cycle compare operation
- Low noise output optimization
- Global hit/miss
- Built-in priority address encoder
- Asynchronous reset control for all the valid-bits
- Up to 32K bits capacity
- Up to 512 number of words
- Up to 64 number of bit per word

Function Description

CAM_HD is a single-port synchronous binary CAM which is provided as a compiler. CAM_HD is intended for use in high-density applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low and CEN and RN are high. The data on DI[] is written to the addressed CAM location and VDI overwrites the valid bit associated with CAM entry with the state selected by A[], and DOUT[], VDO, CAO[] and HIT remains stable during a normal write access cycle. On the rising edge of CK, the read cycle begins when WEN is high and CSN is low and CEN and RN are high. The data at DOUT[] become valid after a delay and VDO, during a normal read access cycle, reads back the valid bit associated with the A[] selected by CAM entry. On the rising edge of CK, the compare cycle starts when CSN and CEN are low and RN are high, All valid data entries in the CAM are simultaneously searched for the match pattern (CDI[]) defined by mask pattern(CMN[]). CDI[] bits are considered as matched bits at all times, if the corresponding bits of the applied CMN[] are in low states. Each CAM entry can be excluded from the compare function by setting the associated valid bit to a low state by the use of VDI. If one or more entries match with the masked CMN[] pattern, HIT will be asserted and CAO[] will contain the lowest one of all matched addresses by the built-in priority address encoder. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[], VDO, CAO[] and HIT remains stable. When OEN is high, DOUT[] and VDO are placed in a high-impedance state. When AEN is high, CAO[] is placed in a high-impedance state. On the falling edge of RN, all the valid-bits are invalidated and settled to low states, therefore all the entries are excluded from CAM match function so no match can occur. A low state of RN inhibits all access, same as when CSN is in a high state.

CAM_HD

High-Density Single-Port Synchronous Binary CAM

CAM_HD Function Table

CK	CSN	RN	WEN	AEN	OEN	A	DI/ VDI	CDI	CMN	CEN	DOUT/ VDO	HIT	CAO	Comment
X	X	L	X	L	L	X	X	X	X	X	X	X	X	Reset
X	H	H	X	L	L	X	X	X	X	X	UNCH	UNCH	UNCH	Idle
X	X	X	X	H	H	X	X	X	X	X	Z	UNCH	Z	Tri-state
↑	L	H	L	L	L	Valid	Valid	X	X	H	UNCH	UNCH	UNCH	Write
↑	L	H	H	L	L	Valid	X	X	X	H	Data-out	UNCH	UNCH	Read
↑	L	H	X	L	L	X	X	Valid	Valid	L	UNCH	1	Lowest of all matched addresses	Matched compare cycle
↑	L	H	X	L	L	X	X	Valid	Valid	L	UNCH	0	0	Missed compare cycle

NOTES:

1. DOUT and VDO are high impedance when OEN is high.
2. CAO is high impedance when AEN is high.
3. HIT is 1 if matched or 0 if not.
4. Match pattern is defined by CDI, bit-wise enabled by CMN.

Parameter Description

CAM_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w) and Number of bit per word(b) and Column mux(y).

Parameters	Min	Max	Step	Note
Address Inputs(m)	3	9	1	Words(w) is limited to one of (8, 16, 32, 64, 128, 256, 512).
Words (w)	8	512	Note	
Bpw (b)	2	64	1	
Mux(y)	1	1	-	
Capacity	16	32K	-	

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[], DI[], CDI[], CMN[], VDI and CEN are latched into the RAM on the rising edge of CK. If CSN and WEN are low and CEN and RN are high on the rising edge of CK, the RAM is in write mode. If CSN is low and WEN is high and CEN and RN are high on the rising edge of CK, the RAM is in read mode. If CSN and CEN are low and RN is high on the rising edge of CK, the RAM is in compare mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low and RN is high, the RAM is enabled for reading, writing or comparing, depending on the state of WEN and CEN. When CSN is high and RN is high, the RAM goes to the standby mode and is disabled for reading or writing or comparing. DOUT[], VDO, HIT and CAO[] remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK depending on the state of CEN. When CSN and WEN is low and CEN and RN are high, data are written to the addressed location and DOUT[], VDO, HIT and CAO[] remains stable. When CSN is low and WEN is high and CEN and RN are high, data from the addressed word are present at DOUT[] and VDO, whereas HIT and CAO[] remains stable.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT[] and VDO are disabled and go to high-impedance state.
CEN	Compare Enable	Compare enable input. The compare enable is latched into the RAM on the rising edge of CK. When CSN and CEN is low and RN is high, the CAM match function is activated. When CSN is low and CEN and RN are high, only read-write accesses are permitted.
AEN	Address Output Enable	Address output enable input. The address output enable is asynchronously operated regardless of any input. When AEN is high, CAO[] is disabled and goes to high-impedance state.
CMN [ ]	Compare Mask Input	Compare mask input bus. CMN[] defines the pattern which enables the CDI[] pattern to be used for the CAM match function. If the CMN[] bit is low, the corresponding CDI[] bit will be interpreted as a wild card.
A [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
VDI	Valid Bit Input	Valid Bit Input. VDI overwrites the valid bit associated with the CAM entry with the state selected by A[], during a normal write access cycle. Valid Bit Input are latched on the rising edge of CK.
CDI [ ]	Compare Data Input	Compare Data input bus. Compare-data are latched on the rising edge of CK and define the data pattern to be matched with the CAM entries, in conjunction to CMN[].
RN	Reset Enable	Reset Enable. RN, if low, invalidates all the CAM entries by setting all the valid-bits, one per entry, to low states, therefore all the entries are excluded from CAM match function so no match can occur. A low state of RN inhibits all access, same as when CSN is in a high state.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode and compare mode.
VDO	Valid Bit Output	Valid bit output. VDO, during a normal read access cycle, reads back the valid bit associated with the A[] selected by CAM entry.
CAO [ ]	Address Output	Address output bus. CAO[] presents the address of the matched entry, in a single match case. In a multiple-match case, CAO[] is the lowest one of all matched addresses by the built-in priority address encoder.
HIT	Match Output	Match Output. HIT indicates one or more CAM entries matched the masked CDI[], if high.

CAM_HD

High-Density Single-Port Synchronous Binary CAM

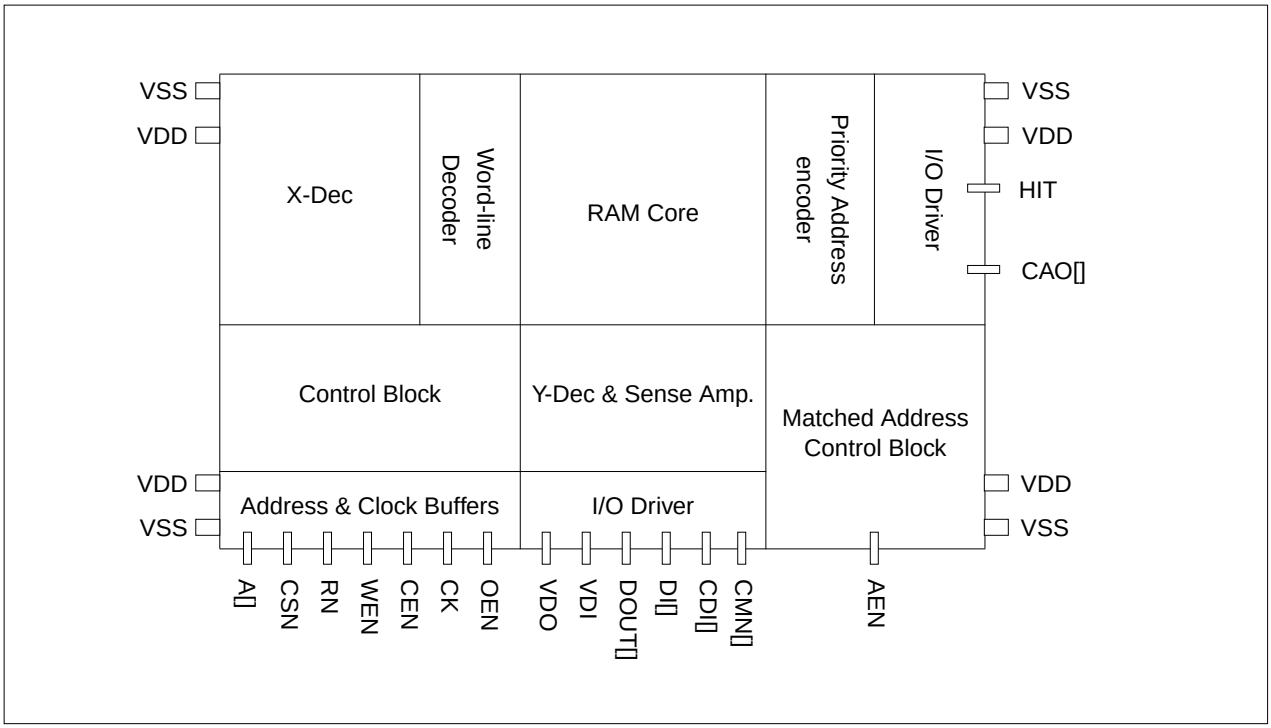
Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	CEN	AEN	CMN	A
4.2847	0.7056	1.4209	0.7056	1.4209	1.5259	1.4209	1.4209
DI	**VDI**	**CDI**	**RN**	**DOUT**	**CDO**	**CAO**	
1.4209	1.4209	1.4209	0.7056	16.7244	16.7244	16.7244	

Block Diagrams

CAM_HD supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports except HIT and CAO are located on the bottom of the memory. HIT and CAO are located on the right-edge of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in CAM_HD is permitted only for Metal-5 layer or upper layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of CAM_HD.

4. Power reduction during standby mode. The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{da}	De-access time
t_{ckl}	Clock pulse width low	t_{vdacc}	Validity data access time
t_{ckh}	Clock pulse width high	t_{vdda}	Validity data de-access time
t_{as}	Address setup time	t_{caacc}	Matched address access time
t_{ah}	Address hold time	t_{cada}	Matched address de-access time
t_{cs}	CSN setup time	t_{htacc}	Global Hit/Miss access time
t_{ch}	CSN hold time	t_{htda}	Global Hit/Miss de-access time
t_{ds}	Data-In setup time	t_{dz}	DOUT drive to high-Z time
t_{dh}	Data-In hold time	t_{zd}	DOUT high-Z to drive time
t_{ws}	WEN setup time	t_{od}	OEN to valid output time
t_{wh}	WEN hold time	t_{vddz}	VDO drive to high-Z time
t_{ces}	CEN setup time	t_{vdzd}	VDO high-Z to drive time
t_{ceh}	CEN hold time	t_{vdod}	OEN to valid output time for VDO
t_{cms}	CMN setup time	t_{cadz}	CAO drive to high-Z time
t_{cmh}	CMN hold time	t_{cazd}	CAO high-Z to drive time
t_{vds}	VDI setup time	t_{caod}	AEN to valid output time for CAO
t_{vdh}	VDI hold time	t_{rn}	Min RN pulse width low
t_{cds}	CDI setup time	t_{rns}	RN setup time
t_{cdh}	CDI hold time	t_{rnh}	RN hold time
t_{acc}	Data access time		

Definition for Power Consumption (μW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_compare	The dynamic average power consumption while in a compare cycle
Power_reset	The dynamic average power consumption while in a reset mode
Power_standby	The standby power consumption while CSN and RN are high, OEN and AEN are low and other signals are in normal operations

Definition for Area (μm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

Reference Table

*** For Ymux=1** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**8**	**8**	**8**	**8**	**8**	**8**
Timing (ns)						
t_{cyc}	2.68	2.71	2.77	3.56	4.44	5.60
t_{ckl}	0.70	0.72	0.74	0.75	0.77	0.78
t_{ckh}	0.75	0.75	0.75	0.75	0.75	0.75
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ah}	0.25	0.28	0.30	0.32	0.35	0.37
t_{cs}	0.70	0.72	0.74	0.75	0.77	0.78
t_{ch}	0.50	0.50	0.50	0.50	0.50	0.50
t_{ces}	0.38	0.40	0.42	0.43	0.45	0.45
t_{ceh}	0.50	0.50	0.50	0.50	0.50	0.50
t_{cms}	0.24	0.24	0.24	0.24	0.24	0.24
t_{cmh}	0.30	0.30	0.30	0.30	0.30	0.30
t_{ds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{dh}	0.33	0.33	0.33	0.33	0.33	0.33
t_{vds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{vdh}	0.33	0.33	0.33	0.33	0.33	0.33
t_{cds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{cdh}	0.30	0.30	0.30	0.30	0.30	0.30
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.25	0.28	0.30	0.32	0.35	0.37
t_{acc}	1.41	1.45	1.52	1.64	1.88	2.40
t_{da}	1.25	1.28	1.35	1.48	1.71	2.24
t_{dz}	0.34	0.34	0.34	0.34	0.34	0.34
t_{zd}	0.42	0.42	0.42	0.42	0.42	0.42
t_{od}	0.46	0.46	0.46	0.46	0.46	0.46
t_{vdacc}	1.41	1.45	1.52	1.64	1.88	2.40
t_{vdda}	1.25	1.28	1.35	1.48	1.71	2.24
t_{vddz}	0.34	0.34	0.34	0.34	0.34	0.34
t_{vdzd}	0.42	0.42	0.42	0.42	0.42	0.42
t_{vdod}	0.46	0.46	0.46	0.46	0.46	0.46
t_{caacc}	2.04	2.13	2.37	2.85	3.52	4.35
t_{cada}	1.26	1.31	1.39	1.77	2.20	2.76
t_{cadz}	0.30	0.32	0.34	0.39	0.48	0.71
t_{cazd}	0.41	0.43	0.45	0.50	0.59	0.83
t_{caod}	0.46	0.47	0.50	0.54	0.64	0.87
t_{htacc}	1.81	1.96	2.15	2.64	2.18	3.84
t_{htda}	1.26	1.31	1.39	1.77	2.20	2.76
t_{rn}	2.08	2.11	2.17	2.96	3.84	5.00
t_{rns}	0.70	0.72	0.74	0.75	0.77	0.78
t_{rnh}	2.08	2.11	2.17	2.96	3.84	5.00
Power (µW/MHz)						
Power_read	21.65	24.07	27.48	34.03	47.10	75.50
Power_write	20.59	23.08	30.05	41.05	66.73	111.22
Power_compare	81.76	92.65	111.20	145.38	196.97	306.16
Power_standby	0.55	0.64	0.65	0.74	0.91	1.20
Power_reset	1.37	2.23	3.74	7.21	15.85	39.82
Area (µm)						
Width	210.48	232.12	253.76	275.40	297.06	318.70
Height	382.08	455.04	600.96	892.80	1476.48	2643.84

CAM_HD

High-Density Single-Port Synchronous Binary CAM

Reference Table

*** For Ymux=1** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**16**	**16**	**16**	**16**	**16**	**16**
Timing (ns)						
t_{cyc}	2.84	2.87	2.94	3.71	4.59	5.66
t_{ckl}	0.70	0.72	0.74	0.75	0.77	0.78
t_{ckh}	0.75	0.75	0.75	0.75	0.75	0.75
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ah}	0.25	0.28	0.30	0.32	0.35	0.37
t_{cs}	0.70	0.72	0.74	0.75	0.77	0.78
t_{ch}	0.50	0.50	0.50	0.50	0.50	0.50
t_{ces}	0.38	0.40	0.42	0.43	0.45	0.46
t_{ceh}	0.50	0.50	0.50	0.50	0.50	0.50
t_{cms}	0.24	0.24	0.24	0.24	0.24	0.24
t_{cmh}	0.33	0.33	0.33	0.33	0.33	0.33
t_{ds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{dh}	0.37	0.37	0.36	0.36	0.36	0.36
t_{vds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{vdh}	0.37	0.37	0.36	0.36	0.36	0.36
t_{cds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{cdh}	0.33	0.33	0.33	0.33	0.33	0.33
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.25	0.28	0.30	0.32	0.35	0.37
t_{acc}	1.47	1.51	1.58	1.70	1.94	2.47
t_{da}	1.31	1.34	1.41	1.54	1.78	2.30
t_{dz}	0.37	0.37	0.37	0.37	0.37	0.37
t_{zd}	0.45	0.45	0.45	0.45	0.45	0.45
t_{od}	0.50	0.50	0.50	0.50	0.50	0.50
t_{vdacc}	1.47	1.51	1.58	1.70	1.94	2.47
t_{vdda}	1.31	1.34	1.41	1.54	1.78	2.30
t_{vddz}	0.37	0.37	0.37	0.37	0.37	0.37
t_{vdzd}	0.45	0.45	0.45	0.45	0.45	0.45
t_{vdod}	0.50	0.50	0.50	0.50	0.50	0.50
t_{caacc}	2.14	2.23	2.48	2.95	3.60	4.43
t_{cada}	1.37	1.41	1.50	1.86	2.29	2.84
t_{cadz}	0.30	0.32	0.34	0.39	0.48	0.71
t_{cazd}	0.41	0.43	0.45	0.50	0.59	0.83
t_{caod}	0.46	0.47	0.50	0.54	0.64	0.87
t_{htacc}	1.92	2.07	2.26	2.73	3.26	3.92
t_{htda}	1.37	1.41	1.50	1.86	2.29	2.84
t_{rn}	2.24	2.27	2.34	3.11	3.99	5.06
t_{rns}	0.70	0.72	0.74	0.75	0.77	0.78
t_{rnh}	2.24	2.27	2.34	3.11	3.99	5.06
Power (µW/MHz)						
Power_read	30.19	33.11	37.06	43.98	58.04	88.70
Power_write	28.21	32.54	41.53	56.73	89.40	152.97
Power_compare	126.05	141.28	166.26	214.90	282.62	436.80
Power_standby	0.67	0.79	0.83	0.98	1.19	1.69
Power_reset	1.38	2.24	3.76	7.25	15.92	39.95
Area (µm)						
Width	255.44	277.08	298.72	320.36	342.02	363.66
Height	382.08	455.04	600.96	892.80	1476.48	2643.84

Reference Table

*** For Ymux=1** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**32**	**32**	**32**	**32**	**32**	**32**
Timing (ns)						
t_{cyc}	3.13	3.16	3.23	4.01	4.86	5.88
t_{ckl}	0.70	0.72	0.74	0.75	0.77	0.79
t_{ckh}	0.75	0.75	0.75	0.75	0.75	0.75
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ah}	0.25	0.28	0.30	0.32	0.35	0.37
t_{cs}	0.70	0.72	0.74	0.75	0.77	0.79
t_{ch}	0.50	0.50	0.50	0.50	0.50	0.50
t_{ces}	0.38	0.40	0.42	0.43	0.45	0.47
t_{ceh}	0.50	0.50	0.50	0.50	0.50	0.50
t_{cms}	0.24	0.24	0.24	0.24	0.24	0.24
t_{cmh}	0.39	0.39	0.39	0.39	0.39	0.39
t_{ds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{dh}	0.43	0.43	0.43	0.43	0.43	0.43
t_{vds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{vdh}	0.43	0.43	0.43	0.43	0.43	0.43
t_{cds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{cdh}	0.39	0.39	0.39	0.39	0.39	0.39
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.25	0.28	0.30	0.32	0.35	0.37
t_{acc}	1.57	1.61	1.68	1.82	2.06	2.59
t_{da}	1.41	1.45	1.52	1.65	1.89	2.42
t_{dz}	0.43	0.43	0.43	0.43	0.43	0.43
t_{zd}	0.51	0.51	0.51	0.51	0.51	0.51
t_{od}	0.56	0.56	0.56	0.56	0.56	0.56
t_{vdacc}	1.57	1.61	1.68	1.82	2.06	2.59
t_{vdda}	1.41	1.45	1.52	1.65	1.89	2.42
t_{vddz}	0.43	0.43	0.43	0.43	0.43	0.43
t_{vdzd}	0.51	0.51	0.51	0.51	0.51	0.51
t_{vdod}	0.56	0.56	0.56	0.56	0.56	0.56
t_{caacc}	2.33	2.42	2.67	3.14	3.77	4.59
t_{cada}	1.55	1.60	1.69	2.05	2.46	3.01
t_{cadz}	0.30	0.32	0.34	0.39	0.48	0.71
t_{cazd}	0.41	0.43	0.45	0.50	0.59	0.83
t_{caod}	0.46	0.47	0.50	0.54	0.64	0.87
t_{htacc}	2.10	2.26	2.45	2.92	3.43	4.08
t_{htda}	1.55	1.60	1.69	2.05	2.46	3.01
t_{rn}	2.53	2.56	2.63	3.41	4.26	5.28
t_{rns}	0.70	0.72	0.74	0.75	0.77	0.79
t_{rnh}	2.53	2.56	2.63	3.41	4.26	5.28
Power (µW/MHz)						
Power_read	48.19	52.48	63.38	65.01	81.08	116.12
Power_write	44.04	50.60	57.26	88.61	141.73	237.62
Power_compare	176.03	238.12	277.68	315.01	457.76	706.64
Power_standby	0.96	1.09	1.15	1.38	1.78	2.52
Power_reset	1.40	2.27	3.80	7.32	16.06	40.20
Area (µm)						
Width	345.36	367.00	388.64	410.28	431.94	453.58
Height	382.08	455.04	600.96	892.80	1476.48	2643.84

CAM_HD

High-Density Single-Port Synchronous Binary CAM

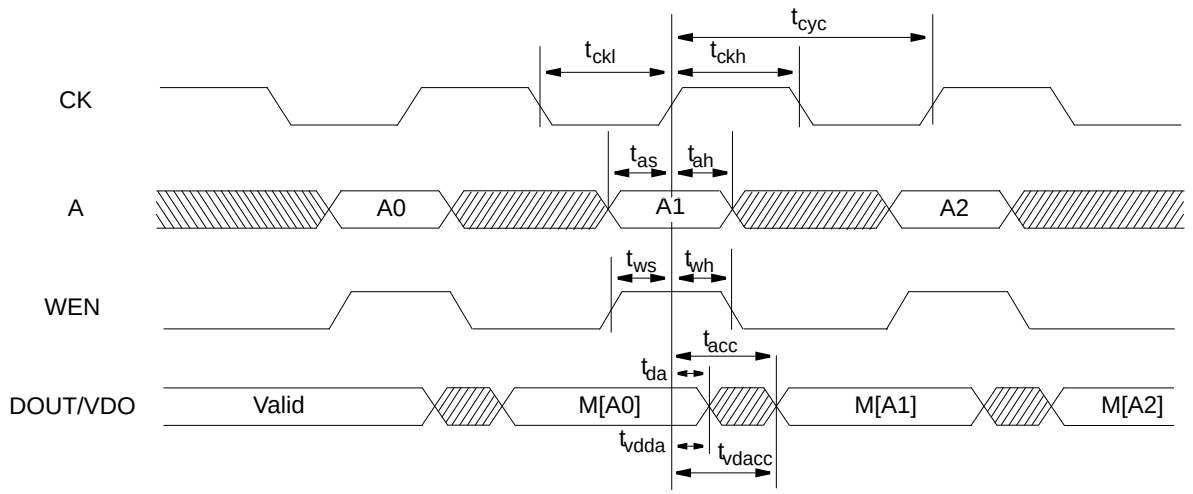
Reference Table

*** For Ymux=1** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**64**	**64**	**64**	**64**	**64**	**64**
Timing (ns)						
t_{cyc}	3.68	3.72	3.79	4.58	5.43	6.42
t_{ckl}	0.70	0.72	0.74	0.75	0.77	0.79
t_{ckh}	0.75	0.75	0.75	0.75	0.75	0.75
t_{as}	0.25	0.25	0.25	0.25	0.25	0.25
t_{ah}	0.25	0.28	0.30	0.32	0.35	0.37
t_{cs}	0.70	0.72	0.74	0.75	0.77	0.79
t_{ch}	0.50	0.50	0.50	0.50	0.50	0.50
t_{ces}	0.38	0.40	0.42	0.43	0.45	0.47
t_{ceh}	0.50	0.50	0.50	0.50	0.50	0.50
t_{cms}	0.24	0.24	0.24	0.24	0.24	0.24
t_{cmh}	0.51	0.51	0.51	0.51	0.51	0.51
t_{ds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{dh}	0.55	0.55	0.55	0.55	0.55	0.55
t_{vds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{vdh}	0.55	0.55	0.55	0.55	0.55	0.55
t_{cds}	0.24	0.24	0.24	0.24	0.24	0.24
t_{cdh}	0.51	0.51	0.51	0.51	0.51	0.51
t_{ws}	0.19	0.19	0.19	0.19	0.19	0.19
t_{wh}	0.25	0.28	0.30	0.32	0.35	0.37
t_{acc}	1.77	1.81	1.89	2.03	2.28	2.81
t_{da}	1.60	1.64	1.72	1.86	2.12	2.65
t_{dz}	0.55	0.55	0.55	0.55	0.55	0.55
t_{zd}	0.62	0.62	0.62	0.62	0.62	0.62
t_{od}	0.67	0.67	0.67	0.67	0.67	0.67
t_{vdacc}	1.77	1.61	1.89	2.03	2.28	2.81
t_{vdda}	1.60	1.64	1.72	1.86	2.12	2.65
t_{vddz}	0.55	0.55	0.55	0.55	0.55	0.55
t_{vdzd}	0.62	0.62	0.62	0.62	0.62	0.62
t_{vdod}	0.67	0.67	0.67	0.67	0.67	0.67
t_{caacc}	2.67	2.76	3.02	3.49	4.13	4.92
t_{cada}	1.89	1.94	2.03	2.41	2.81	3.34
t_{cadz}	0.30	0.32	0.34	0.39	0.48	0.71
t_{cazd}	0.41	0.43	0.45	0.50	0.59	0.83
t_{caod}	0.46	0.47	0.50	0.54	0.64	0.87
t_{htacc}	2.44	2.60	2.80	3.28	3.78	4.49
t_{htda}	1.89	1.94	2.03	2.41	2.81	3.34
t_{rn}	3.08	3.12	3.19	3.98	4.83	5.82
t_{rns}	0.70	0.72	0.74	0.75	0.77	0.79
t_{rnh}	3.08	3.12	3.19	3.98	4.83	5.82
Power (µW/MHz)						
Power_read	86.85	93.50	100.12	110.23	130.68	174.62
Power_write	89.99	90.01	111.90	157.16	244.13	411.65
Power_compare	323.65	360.80	428.70	638.57	816.35	1241.60
Power_standby	1.59	1.58	1.79	2.21	2.97	4.34
Power_reset	1.50	2.32	3.88	7.46	16.33	40.71
Area (µm)						
Width	525.20	546.84	568.48	590.12	611.78	633.42
Height	382.08	455.04	600.96	892.80	1476.48	2643.84

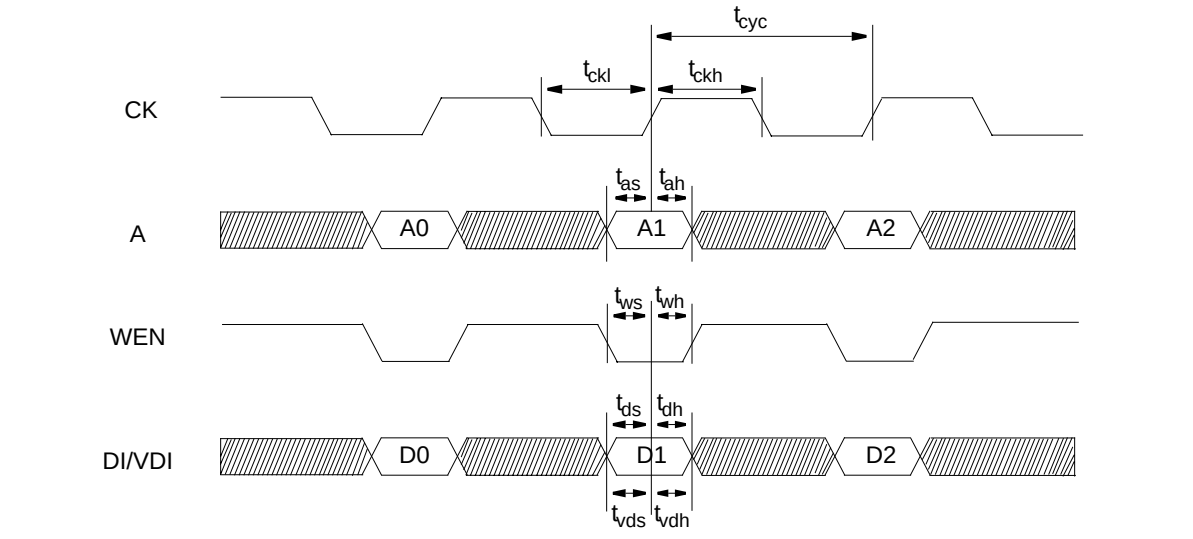
Timing Diagrams

Read Cycle



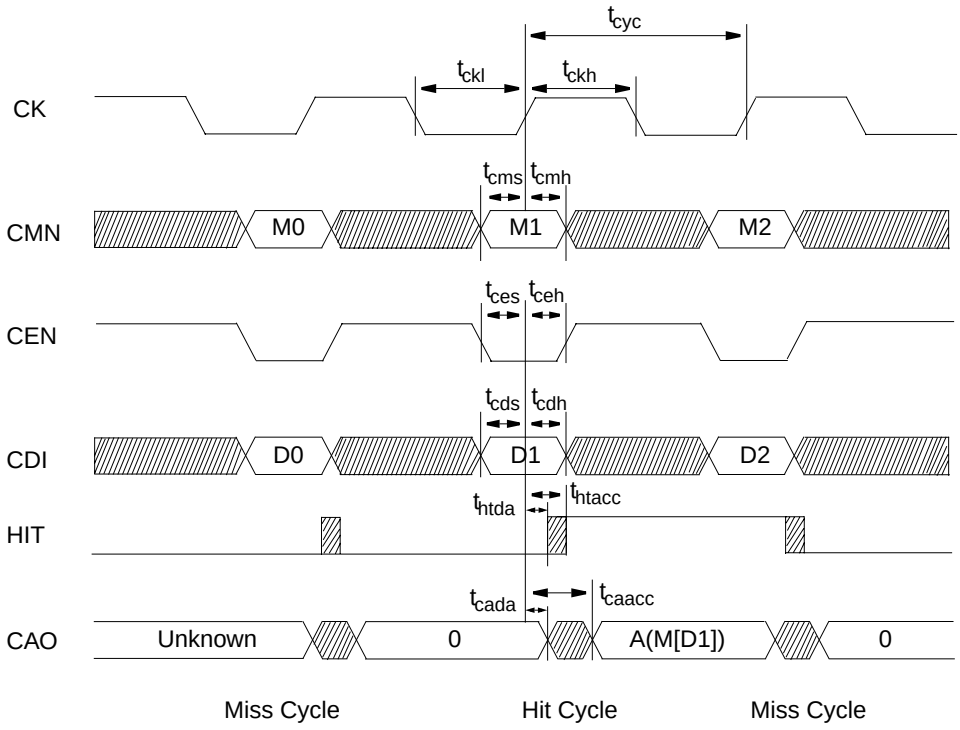
(RN=high, CSN=low, OEN=low, CEN=high, AEN, DI, VDI, CDI, CMN= don't care)

Write Cycle



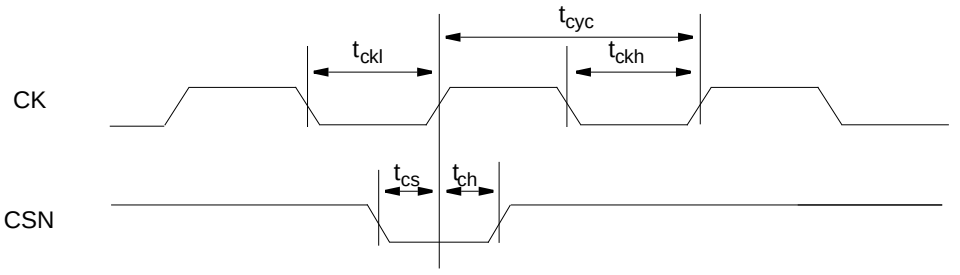
(RN = high, CSN = low, CEN = high, OEN, AEN, CDI, CMN = don't care)

Compare Cycle



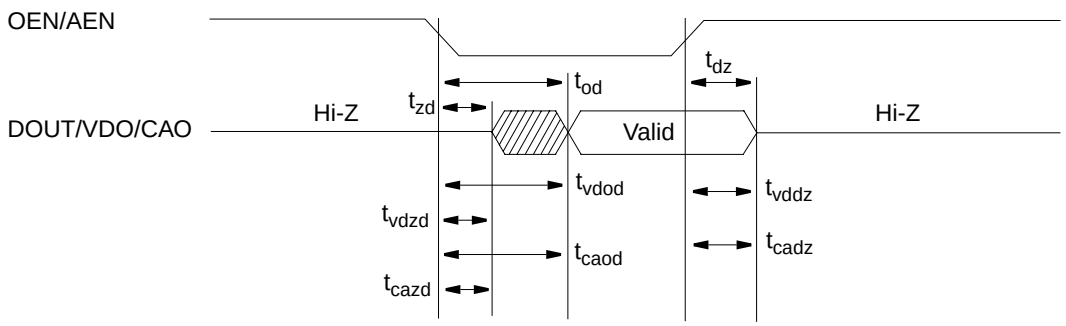
(RN = high, CSN = low, A, WEN, OEN, AEN = don't care)

CSN Controlled



(RN, WEN, OEN CEN, AEN, A, DI, VDI, CDI, CMN = valid)

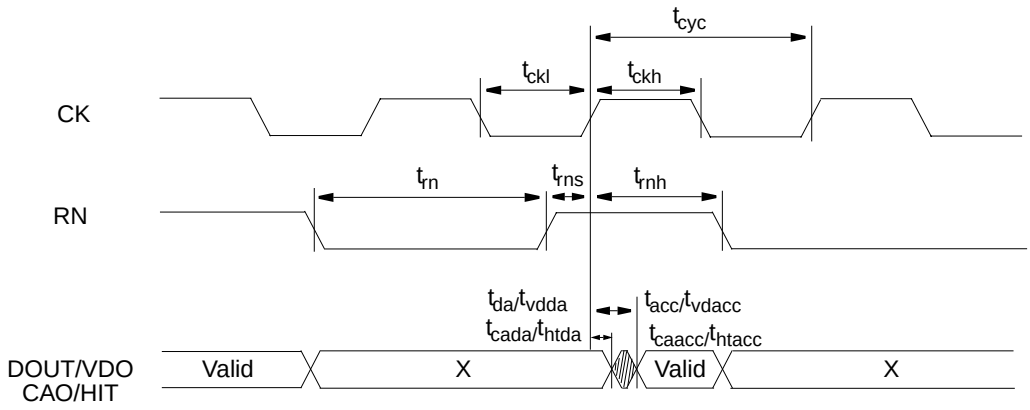
OEN/AEN Controlled Output Enable



(RN, CK, CSN, WEN, CEN, AEN, CMN, A, DI, VDI, CDI = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

RN Controlled Reset Mode



(OEN, CSN, WEN, CEN, AEN, CMN, A, DI, VDI, CDI = valid)