LH52A512

CMOS 512K (64K × 8) Static Ram

FEATURES

- 64K × 8 bit organization
- Access time: 70/100 ns (MAX.)
- Current consumption:
  - Operating: 385 mW (MAX.)
    - 110 mW (t_{RC}, t_{WC} = 1 µs)
  - Standby: 275 µW (MAX.)
  - Data retention:
    - 3 µW (V_{CC} = 3 V, T_A = 25°C)
    - 9 µW (V_{CC} = 3 V, T_A = 40°C)
- Single 5 V power supply: 5 V ±10%
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Operating temperature: 0°C to +70°C
- Packages:
  - 32-pin, 525-mil SOP
  - 32-pin, 8 × 20 mm² TSOP (Type I)

DESCRIPTION

The LH52A512 is a static RAM organized as 64K × 8 bits. An efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

PIN CONNECTIONS

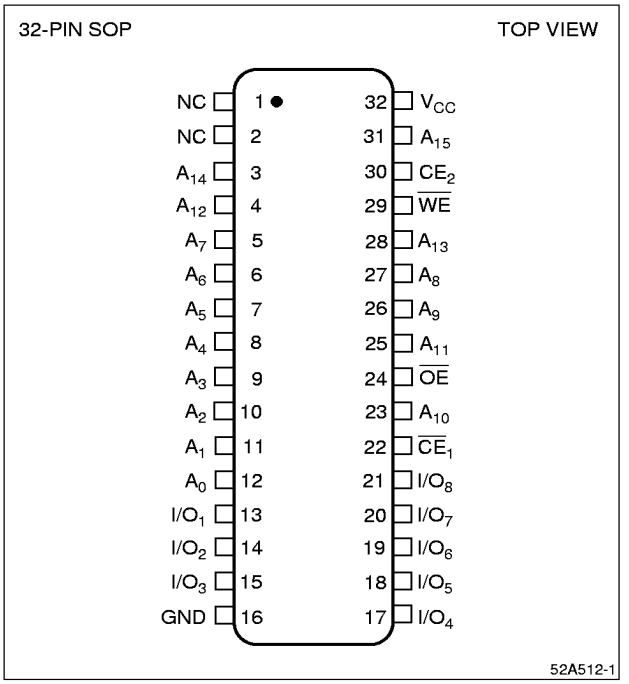


Figure 1. Pin Connections for SOP Package

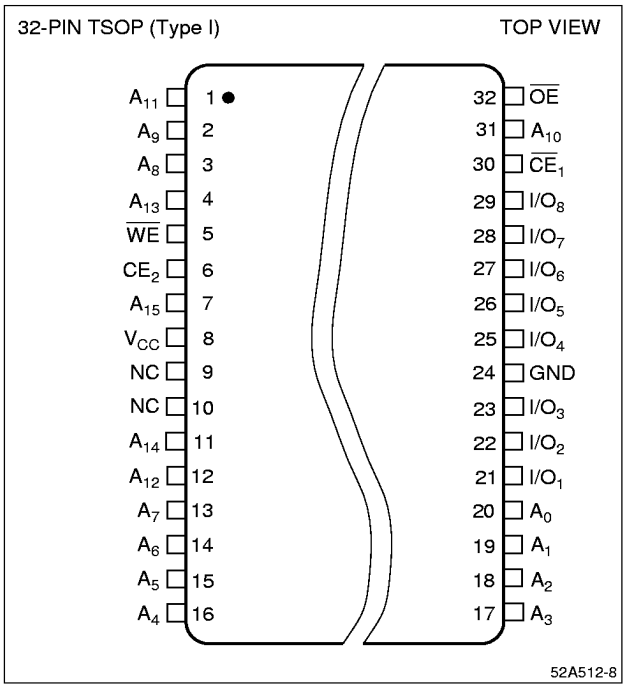


Figure 2. Pin Connections for TSOP Package

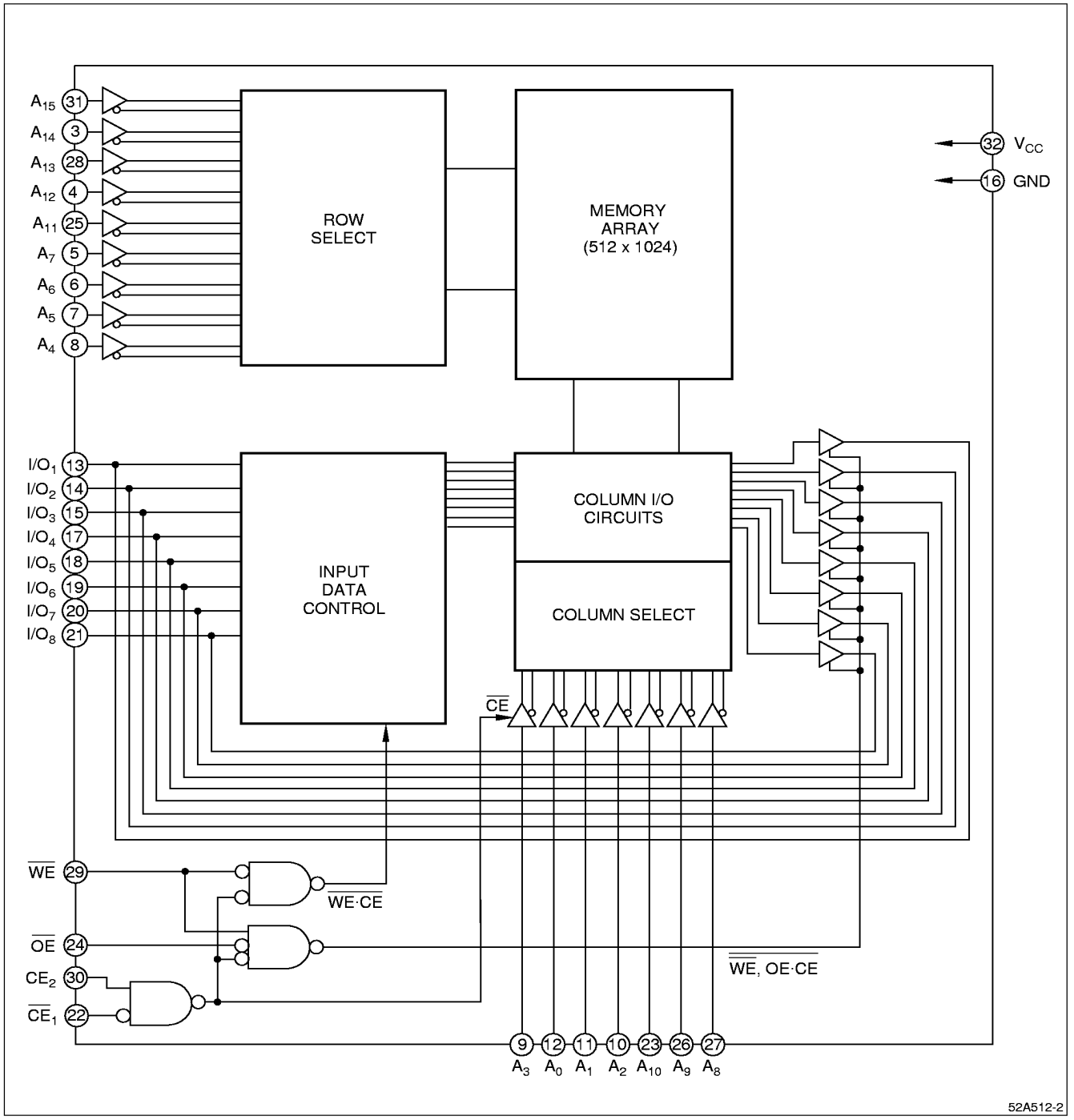


Figure 3. LH52A512 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{15}	Address inputs
$\overline{CE_1}$	Chip Enable input 1
CE_2	Chip Enable input 2
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	No connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	–0.5 to +7.0	V	1
Input voltage	V_{IN}	–0.5 to V_{CC} +0.3	V	1, 2
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–65 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Undershoot of –3.0 V is allowed for pulse width below 50 ns.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Logic '1' input voltage	V_{IH}	2.2		V_{CC} + 0.3	V	
Logic '0' input voltage	V_{IL}	–0.3		0.8	V	1

NOTE:
1. Undershoot of –3.0 V is allowed for pulse width below 50 ns.

DC CHARACTERISTICS [1] (T_A = 0°C to +70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0	1.0	µA
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 V to V_{CC}	–1.0	1.0	µA
Operating supply current	I_{CC1}	Minimum cycle, V_{IN} = V_{IL} or V_{IH} $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}, $I_{I/O}$ = 0 mA		70	mA
Standby current	I_{SB}	$CE_2 \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CC} - 0.2$ V		50	µA
	I_{SB1}	$\overline{CE_1}$, CE_2 = V_{IH} or CE_2 = V_{IL}		3	mA
Output voltage	V_{OL}	I_{OL} = 2.1 mA		0.4	V
	V_{OH}	I_{OH} = –1.0 mA	2.4		

READ CYCLE (T_A = 0°C to +70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	–70 ns		–100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		100		ns	
Address access time	t_{AA}		70		100	ns	
$\overline{CE_1}$ Low to valid data	t_{ACE1}		70		100	ns	
CE_2 High to valid data	t_{ACE2}		70		100	ns	
$\overline{OE}$ Low to valid data	t_{OE}		40		50	ns	
Output hold from address change	t_{OH}	10		10		ns	
$\overline{CE_1}$ Low to output active	t_{CLZ1}	10		10		ns	1
CE_2 High to output active	t_{CLZ2}	10		10		ns	1
$\overline{OE}$ Low to output active	t_{OLZ}	5		5		ns	1
$\overline{CE_1}$ High to output in High-Z	t_{CHZ1}		30		35	ns	1
CE_2 Low to output in High-Z	t_{CHZ2}		30		35	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}		30		35	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

WRITE CYCLE (T_A = 0°C to +70°C, V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	–70 ns		–100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		100		ns	
$\overline{CE}_1$ Low to end of write	t_{CW1}	60		80		ns	
CE_2 High to end of write	t_{CW2}	60		80		ns	
Address valid to end of write	t_{AW}	60		80		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	55		75		ns	
Write recovery time	t_{WR}	0		0		ns	
Input data setup time	t_{DW}	30		40		ns	
Input data hold time	t_{DH}	0		0		ns	
$\overline{WE}$ High to output active	t_{WLZ}	5		5		ns	1
$\overline{WE}$ Low to output in High-Z	t_{HWZ}		30		35	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}		30		35	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

TEST CONDITIONS

PARAMETER	MODE	NOTE
Input pulse levels	0.6 V to 2.4 V	
Input rise/fall times	5 ns	
Input/output timing levels	1.5 V	
Output load, timing test	1TTL + C_L (100 pF)	1

NOTE:
1. Includes scope and jig capacitance.

PIN CAPACITANCE (T_A = 25°C, f = 1 MHz)

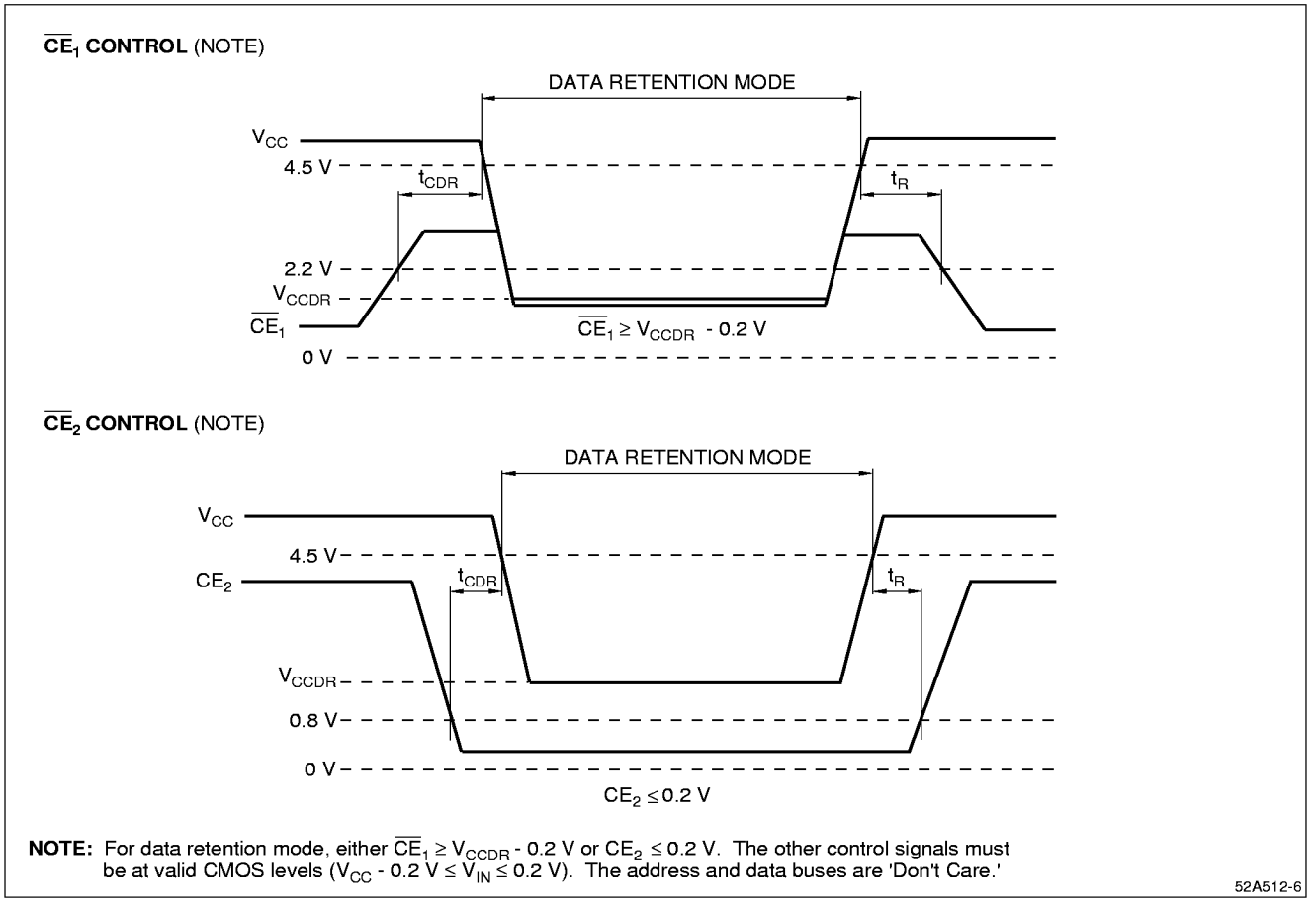
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	V_{IN} = 0 V		10		pF	1
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V		10		pF	1

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR} - 0.2$ V		2.0	5.5	V	1
Data retention supply current	I_{CCDR}	V_{CCDR} = 3.0 V, $CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CCDR} - 0.2$ V	t_A = 25°C		1	µA	
			t_A = 40°C		3		
					25		1
Chip enable setup time	t_{CDR}			0		ns	
Chip enable hold time	t_R			t_{RC}		ns	2

NOTES:
1. $CE_2 \ge V_{CCDR} - 0.2$ V or $CE_2 \le 0.2$ V.
2. t_{RC} = Read cycle time.



NOTE: For data retention mode, either $\overline{CE_1} \ge V_{CCDR}$ - 0.2 V or $CE_2 \le 0.2$ V. The other control signals must be at valid CMOS levels (V_{CC} - 0.2 V ≤ V_{IN} ≤ 0.2 V). The address and data buses are 'Don't Care.'

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Figure 4. Low Voltage Data Retention

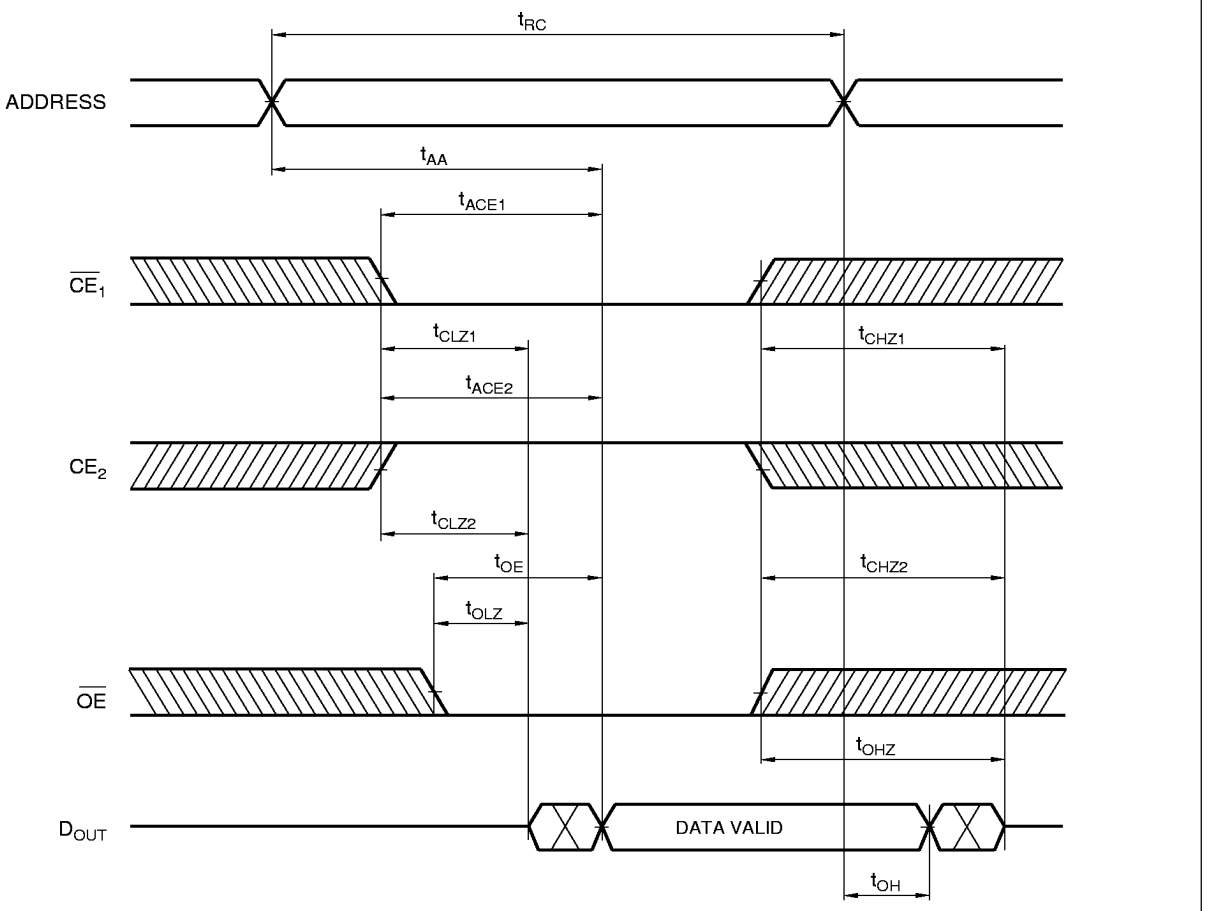
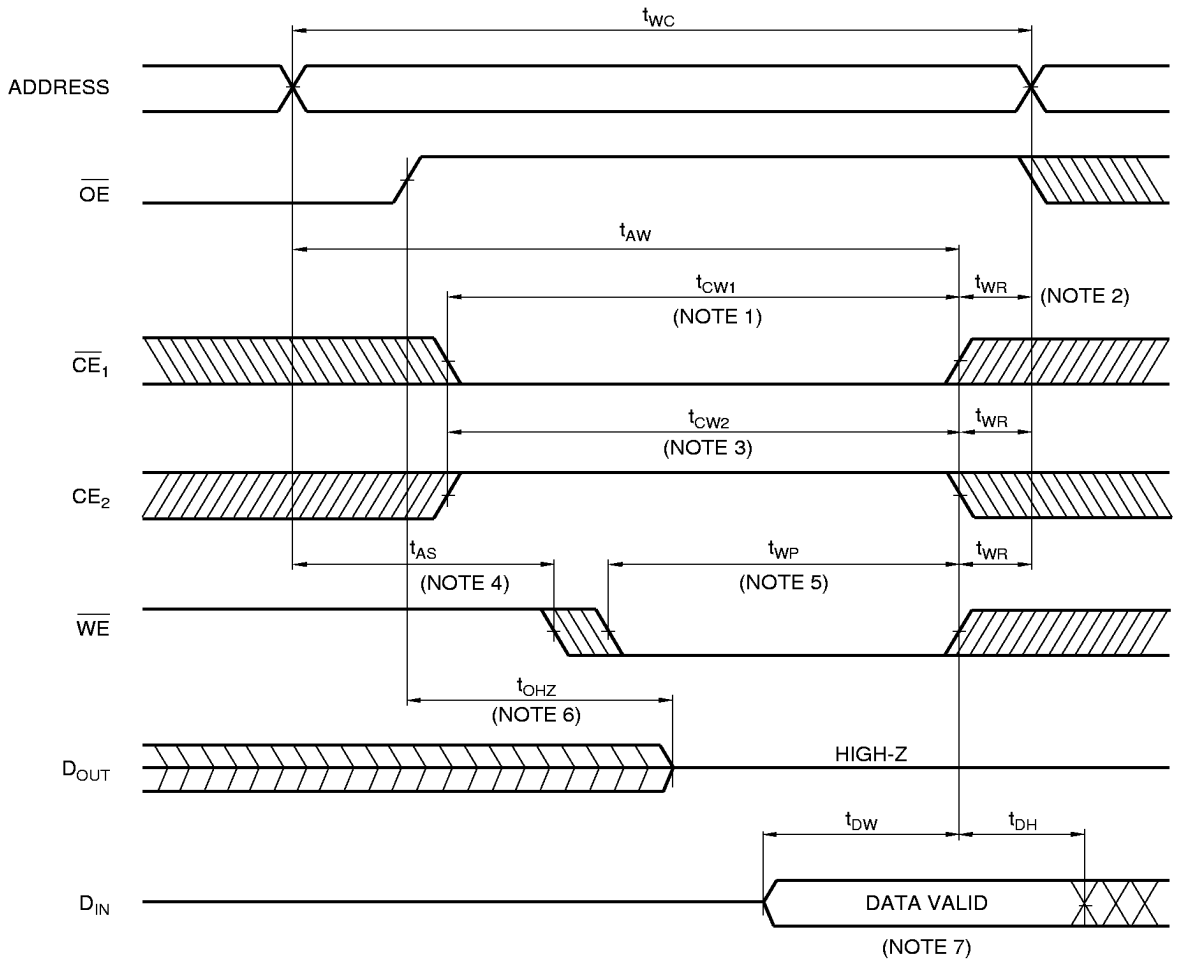


Figure 5. Read Cycle



NOTES:

1. t_{CW1} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition, to the time when the writing is finished.
2. t_{WR} is defined as the time from writing finish to address change.
3. t_{CW2} is defined as the time from the last occuring transition, either CE_2 HIGH transition, to the time when the writing is finished.
4. t_{AS} is defined as the time from address change to writing start.
5. The writing occurs during an overlapping period of $\overline{CE_1}$ = 'LOW,' CE_2 = 'HIGH,' and $\overline{WE}$ = 'LOW' (t_{WP}).
6. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
7. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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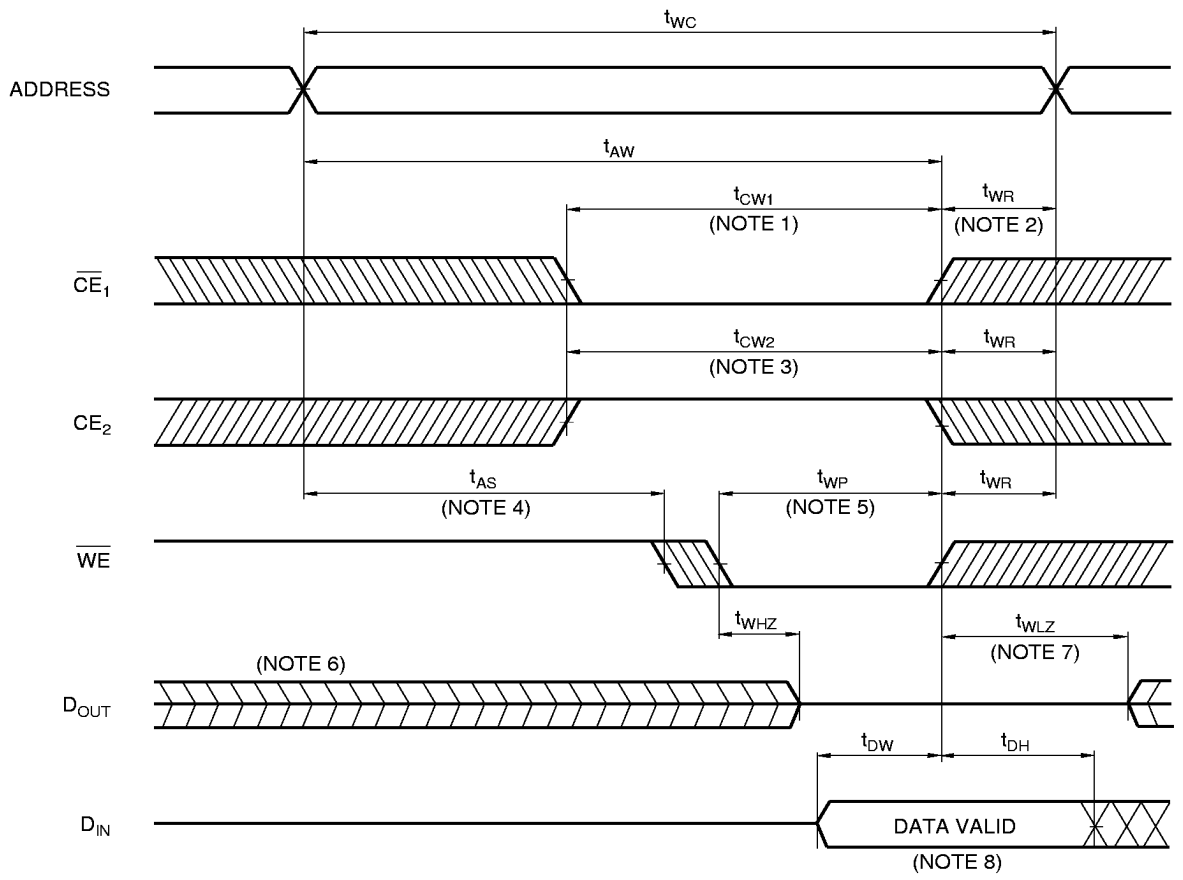
Figure 6. Write Cycle – $\overline{OE}$ Controlled



NOTES:

1. t_{CW1} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition, to the time when the writing is finished.
2. t_{WR} is defined as the time from writing finish to address change.
3. t_{CW2} is defined as the time from the last occuring transition, either CE_2 HIGH transition, to the time when the writing is finished.
4. t_{AS} is defined as the time from address change to writing start.
5. The writing occurs during an overlapping period of $\overline{CE_1}$ = 'LOW,' CE_2 = 'HIGH,' and $\overline{WE}$ = 'LOW' (t_{WP}).
6. If $\overline{CE_1}$ LOW transition, or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
7. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the outputs will remain high-impedance.
8. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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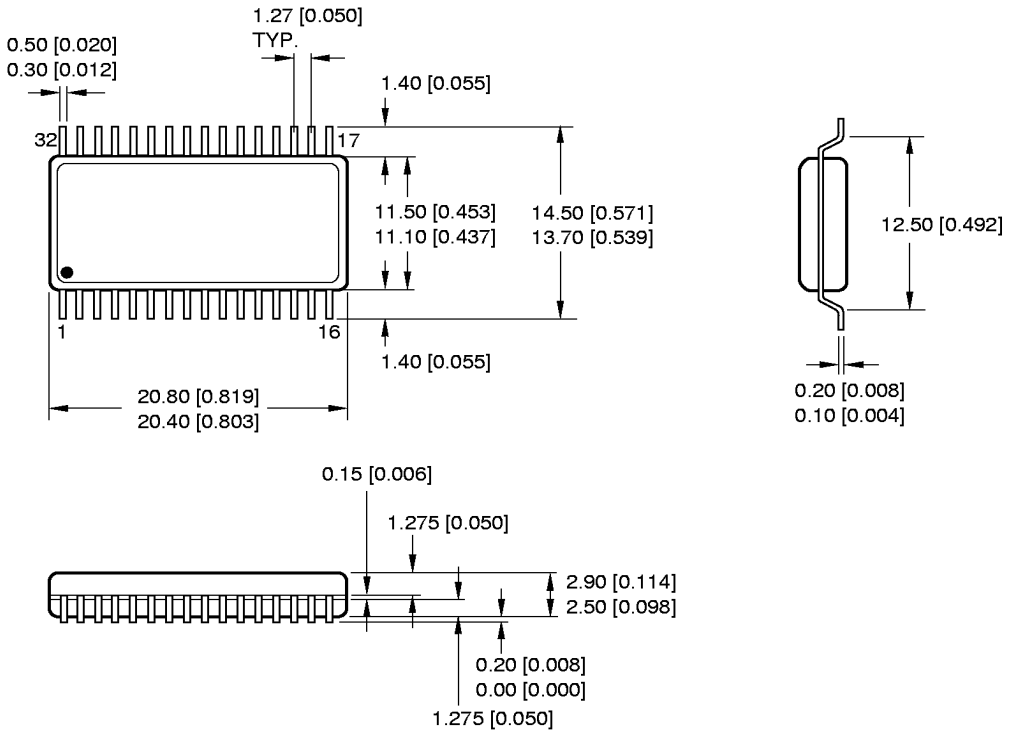
Figure 7. Write Cycle – $\overline{OE}$ Low Fixed

PACKAGE DIAGRAMS

32SOP (SOP032-P-0525)

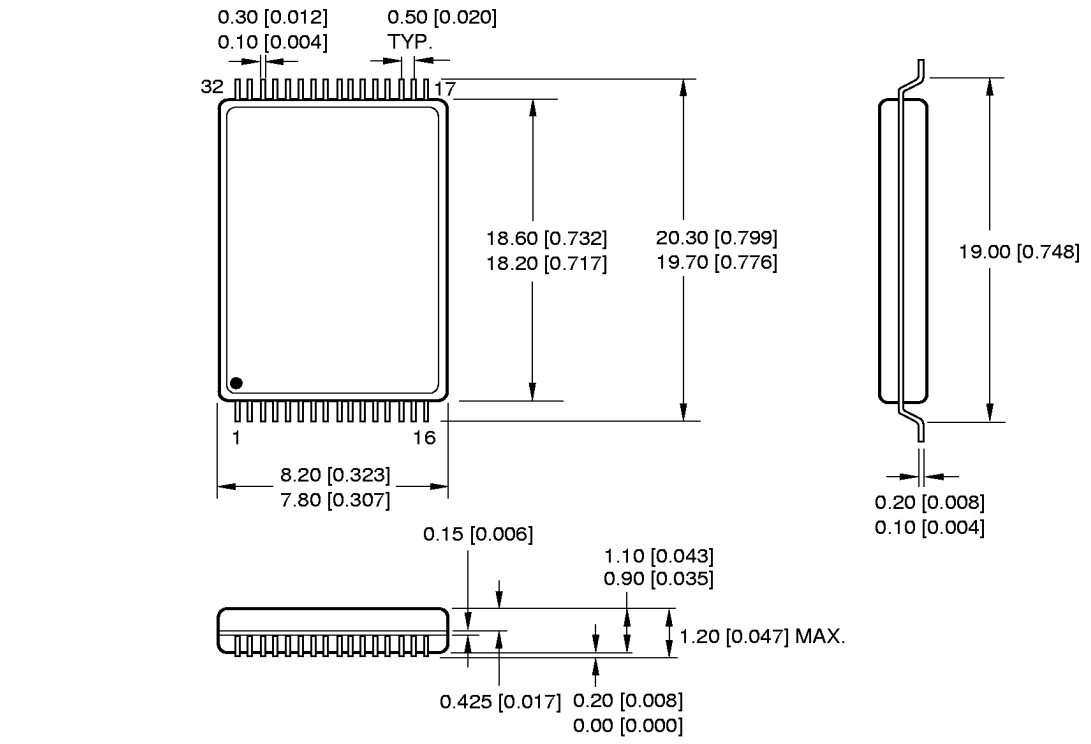


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32SOP

32-pin, 525-mil SOP

32TSOP (Type I) (TSOP032-P-0820)



32-pin, 8 × 20 mm^2 TSOP (Type I)

ORDERING INFORMATION