V•I CHIP
FACTORIZED POWER

BCM™
DC to DC
Bus Converter Module

FEATURES

- 384 Vdc – 48 Vdc 325 W Bus Converter Module
- High efficiency (>95%) reduces system power consumption
- High power density (>1000 W/in³) reduces power system footprint by >40%
- "Full Chip" V•I Chip package enables surface mount, low impedance interconnect to system board
- Contains built-in protection features: undervoltage, overvoltage lockout, overcurrent protection, short circuit protection, overtemperature protection.
- Provides enable/disable control, internal temperature monitoring
- ZVS/ZCS Resonant Sine Amplitude Converter topology
- Can be paralleled to create multi-kW arrays

TYPICAL APPLICATIONS

- High End Computing Systems
- Automated Test Equipment
- Telecom Base Stations
- High Density Power Supplies
- Communications Systems

DESCRIPTION

The V•I Chip Bus Converter Module is a high efficiency (>95%) Sine Amplitude Converter (SAC)™ operating from a 360 to 400 Vdc primary bus to deliver an isolated 45 – 50 V nominal, un-regulated secondary. The SAC offers a low AC impedance beyond the bandwidth of most downstream regulators, meaning that input capacitance normally located at the input of a regulator can be located at the input to the SAC. Since the K factor of the VIB0002TFJ is 1/8, that capacitance value can be reduced by a factor of 64x, resulting in savings of board area, materials and total system cost.

The VIB0002TFJ is provided in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The V•I Chip package provides flexible thermal management through its low junction-to-case and junction-to-board thermal resistance. With high conversion efficiency the VIB0002TFJ increases overall system efficiency and lowers operating costs compared to conventional approaches.
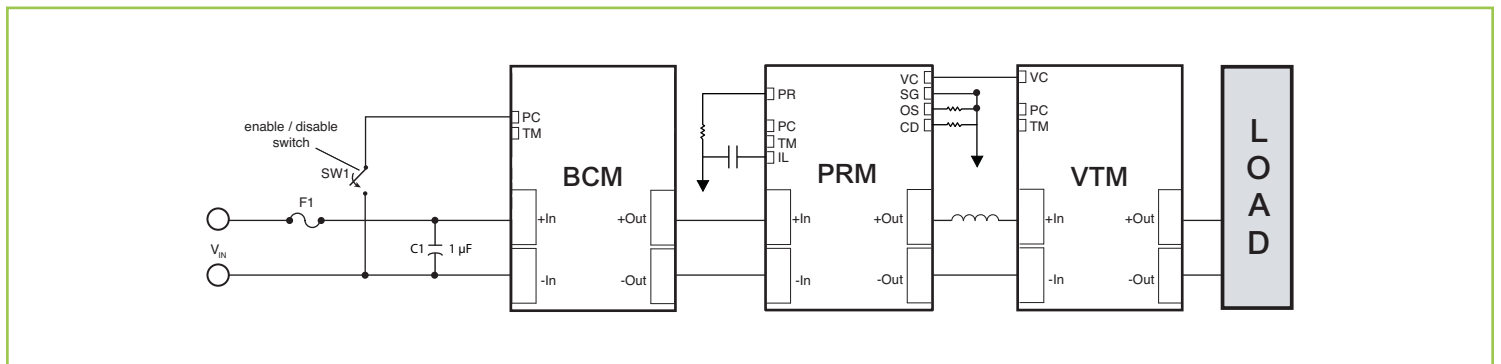
V_{IN} = 360 – 400 V	P_{OUT} = 325 W (NOM)
V_{OUT} = 45 – 50 V (NO LOAD)	K = 1/8

TYPICAL APPLICATION

ABSOLUTE MAXIMUM RATINGS

+IN to –IN . . . . -1.0 Vdc – +440 Vdc

PC to –IN . . . . -0.3 Vdc – +20 Vdc

TM to –IN . . . . -0.3 Vdc – +7 Vdc

+IN/-IN to +OUT/-OUT . . . . 4242 V (Hi Pot)

+IN/-IN to +OUT/-OUT . . . . 500 V (working)

+OUT to –OUT . . . . -1.0 Vdc - +60 Vdc

Temperature during reflow . . . . 225°C (MSL5)

PACKAGE ORDERING INFORMATION

Bottom View

Signal Name	Designation
+In	A1-E1, A2-E2
–In	L1-T1, L2-T2
TM	H1, H2
RSV	J1, J2
PC	K1, K2
+Out	A3-D3, A4-D4, J3-M3, J4-M4
–Out	E3-H3, E4-H4, N3-T3, N4-T4

PART NUMBER	DESCRIPTION
VIB0002TFJ	-40°C – 125°C T_J, J lead
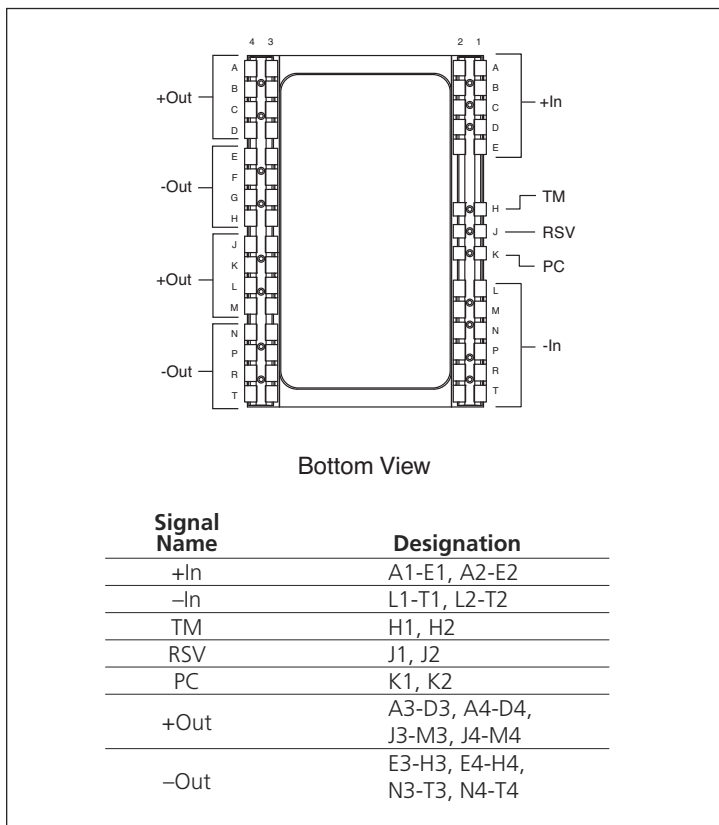
CONTROL PIN SPECIFICATIONS

See section 5.0 for further application details and guidelines.

PC (V•I Chip BCM Primary Control)

The PC pin can enable and disable the BCM. When held below V_{PC_DIS} the BCM shall be disabled. When allowed to float with an impedance to –IN of greater than 50 kΩ the module will start. When connected to another BCM PC pin, the BCMs will start simultaneously when enabled. The PC pin is capable of being driven high by an either external logic signal or internal pull up to 5 V (operating).

TM (V•I Chip BCM Temperature Monitor)

The TM pin monitors the internal temperature of the BCM within an accuracy of +5/-5°C. It has a room temperature setpoint of ~3.0 V and an approximate gain of 10 mV/°C. It can source up to 100 µA and may also be used as a "Power Good" flag to verify that the BCM is operating.

VIB0002TFJ

1.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T$_J$ < 125°C (T-Grade)**; All other specifications are at **T$_J$ = 25°C** unless otherwise noted

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Voltage range	V$_{IN}$		**360**	**384**	**400**	Vdc
dV/dt	dV$_{IN}$/dt				**1**	V/µs
Quiescent power	P$_Q$	PC connected to -IN		395	**410**	mW
No load power dissipation	P$_{NL}$	V$_{IN}$ = 384 V		6.5	10	W
		V$_{IN}$ = 360 to 400 V			**13.5**	
Inrush Current Peak	I$_{INR\_P}$	V$_{IN}$ = 400 V C$_{OUT}$ = 100 µF, P$_{OUT}$ = 325 W		2	**4**	A
DC Input Current	I$_{IN\_DC}$	P$_{OUT}$ = 325 W			**1**	A
K Factor $\left(\dfrac{V_{OUT}}{V_{IN}}\right)$	K			1/8		
Output Power (Average)	P$_{OUT}$	V$_{IN}$ = 384 V$_{DC}$; See Figure 14			**325**	W
		V$_{IN}$ = 360 – 400 V$_{DC}$; See Figure 14			**300**	
Output Power (Peak)	P$_{OUT\_P}$	V$_{IN}$ = 384 V$_{DC}$ Average P$_{OUT}$ <= 325 W, Tpeak < 5 ms			**495**	W
Output Voltage	V$_{OUT}$	Section 3.0 No load	**45**		**50**	V
Output Current (Average)	I$_{OUT}$	Pout <= 325 W			7.05	A
Efficiency (Ambient)	η	V$_{IN}$ = 384 V, P$_{OUT}$ = 325 W	94.2	95.5		%
		V$_{IN}$ = 360 V to 400 V, P$_{OUT}$ = 325 W	94.2			
Efficiency (Hot)	η	V$_{IN}$ = 384 V, T$_J$ = 100° C, P$_{OUT}$ = 325 W	94	95		%
Minimum Efficiency (Over Load Range)	η	60 W < P$_{OUT}$ < 325 W Max	**90**			%
Output Resistance (Ambient)	R$_{OUT}$	T$_J$ = 25° C	100	170	200	mΩ
Output Resistance (Hot)	R$_{OUT}$	T$_J$ = 125° C	150	235	270	mΩ
Output Resistance (Cold)	R$_{OUT}$	T$_J$ = -40° C	60	130	180	mΩ
Load Capacitance	C$_{OUT}$				**100**	uF
Switching Frequency	F$_{SW}$		**1.66**	1.75	**1.83**	MHz
Ripple Frequency	F$_{SW\_RP}$		**3.33**	3.5	**3.66**	MHz
Output Voltage Ripple	V$_{OUT\_PP}$	C$_{OUT}$ = 0 µF, P$_{OUT}$ = 325 W, V$_{IN}$ = 384 V, Section 8.0		160	**400**	mV
V$_{IN}$ to V$_{OUT}$ (Application of V$_{IN}$)	T$_{ON1}$	V$_{IN}$ = 384 V, C$_{PC}$ = 0; See Figure 16	460	540	620	ms
PC						
PC Voltage (Operating)	V$_{PC}$		**4.7**	5	**5.3**	V
PC Voltage (Enable)	V$_{PC\_EN}$		**2**	2.5	**3**	V
PC Voltage (Disable)	V$_{PC\_DIS}$				**1.95**	V
PC Source Current (Startup)	I$_{PC\_EN}$		**50**	100	**300**	uA
PC Source Current (Operating)	I$_{PC\_OP}$		**2**	3.5	**5**	mA
PC Internal Resistance	R$_{PC\_SNK}$	Internal pull down resistor	**50**	150	**400**	kΩ
PC Capacitance (Internal)	C$_{PC\_INT}$	Section 5.0			1000	pF
PC Capacitance (External)	C$_{PC\_EXT}$	External capacitance delays PC enable time			1000	pF
External PC Resistance	R$_{PC}$	Connected to –V$_{IN}$	**50**			kΩ
PC External Toggle Rate	F$_{PC\_TOG}$				**1**	Hz
PC to V$_{OUT}$ with PC Released	Ton2	V$_{IN}$ = 384 V, Pre-applied C$_{PC}$ = 0, C$_{OUT}$ = 0; See Figure 16	50	100	150	µs
PC to V$_{OUT}$, Disable PC	T$_{PC\_DIS}$	V$_{IN}$ = 384 V, Pre-applied C$_{PC}$ = 0, C$_{OUT}$ = 0; See Figure 16		4	**10**	µs

1.0 ELECTRICAL CHARACTERISTICS (CONT.)

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T$_J$ < 125°C (T-Grade)**; All other specifications are at **T$_J$ = 25°C** unless otherwise noted

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
TM						
TM accuracy	A$_{CTM}$		**-5**		**+5**	°C
TM Gain	A$_{TM}$			10		mV/°C
TM Source Current	I$_{TM}$		**100**			uA
TM Internal Resistance	R$_{TM\_SNK}$		**25**	40	**50**	kΩ
External TM Capacitance	C$_{TM}$				**50**	pF
TM Voltage Ripple	V$_{TM\_PP}$	C$_{TM}$ = 0µF, V$_{IN}$ = 400 V, P$_{OUT}$ = 325 W	**200**	400	**500**	mV
PROTECTION						
Negative going OVLO	V$_{IN\_OVLO-}$		**400**	420	**430**	V
Positive going OVLO	V$_{IN\_OVLO+}$		**420**	430	**440**	V
Negative going UVLO	V$_{IN\_UVLO-}$		**270**	285	**304**	V
Positive going UVLO	V$_{IN\_UVLO+}$		**290**	310	**330**	V
Output Overcurrent Trip	I$_{OCP}$	V$_{IN}$ = 384 V, 25°C	**9**	11	**14**	A
Short Circuit Protection Trip Current	I$_{SCP}$		**14**			A
Short Circuit Protection Response Time	T$_{SCP}$				**1.2**	us
Thermal Shutdown Junction setpoint	T$_{J\_OTP}$		**125**	130	**135**	°C
GENERAL SPECIFICATION						
Isolation Voltage (Hi-Pot)	V$_{HIPOT}$		**4242**			V
Working Voltage (IN – OUT)	V$_{WORKING}$				**500**	V
Isolation Capacitance	C$_{IN\_OUT}$	Unpowered unit	**500**	660	**800**	pF
Isolation Resistance	R$_{IN\_OUT}$		**10**			MΩ
MTBF		MIL HDBK 217F, 25° C, GB		4.2		Mhrs
Agency Approvals/Standards		cTUVus				
		CE Mark				
		ROHS 6 of 6				

1.1 APPLICATION CHARACTERISTICS

All specifications are at $T_J = 25°C$ unless otherwise noted. See associated figures for general trend data.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	TYP	UNIT
No Load Power	P_{NL}	V_{IN} = 384 V, PC enabled; See Figure 1	6.5	W
Inrush Current Peak	I_{NR_P}	C_{OUT} = 100 µF, P_{OUT} = 325 W	2	A
Efficiency (Ambient)	η	V_{IN} = 384 V, P_{OUT} = 325 W	95.5	%
Efficiency (Hot – 100°C)	η	V_{IN} = 384 V, P_{OUT} = 325 W	95	%
Output Resistance (-40°C)	R_{OUT}	V_{IN} = 384 V	130	mΩ
Output Resistance (25°C)	R_{OUT}	V_{IN} = 384 V	170	mΩ
Output Resistance (100°C)	R_{OUT}	V_{IN} = 384 V	235	mΩ
Output Voltage Ripple	V_{OUT_PP}	C_{OUT} = 0 uF, P_{OUT} = 325 W @ V_{IN} = 384, V_{IN} = 384 V	160	mV
V_{OUT} Transient (Positive)	V_{OUT_TRAN+}	I_{OUT_STEP} = 0 TO 7.07 A, I_{SLEW} >10 A/us; See Figure 11	1.5	mV
V_{OUT} Transient (Negative)	V_{OUT_TRAN-}	I_{OUT_STEP} = 7.07 A to 0 A, I_{SLEW} > 10 A/us; See Figure 12	1.5	mV
Undervoltage Lockout Response Time Constant	T_{UVLO}		150	µs
Output Overcurrent Response Time Constant	T_{OCP}	9 < I_{OCP} < 14 A	5	ms
Overvoltage Lockout Response Time Constant	T_{OVLO}		120	µs
TM Voltage (Ambient)	V_{TM_AMB}	$T_J \cong 27°C$	3	V

No Load Power Dissipation vs Line
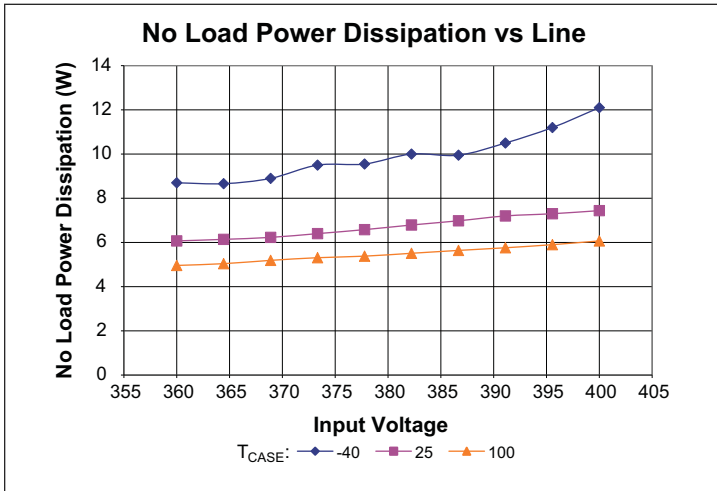
Figure 1 – *No load power dissipation vs. V_{IN}; T_{CASE}*

Full Load Efficiency vs Temperature
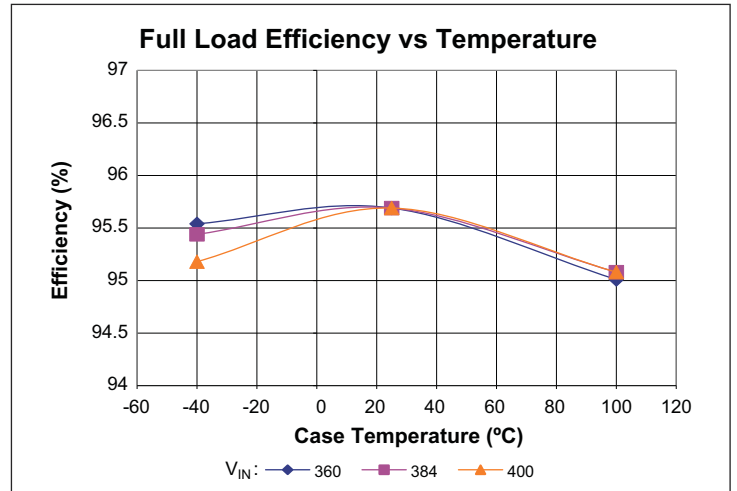
Figure 2 – *Full load efficiency vs. temperature; V_{IN}*

Efficiency & Power Dissipation -40°C Case
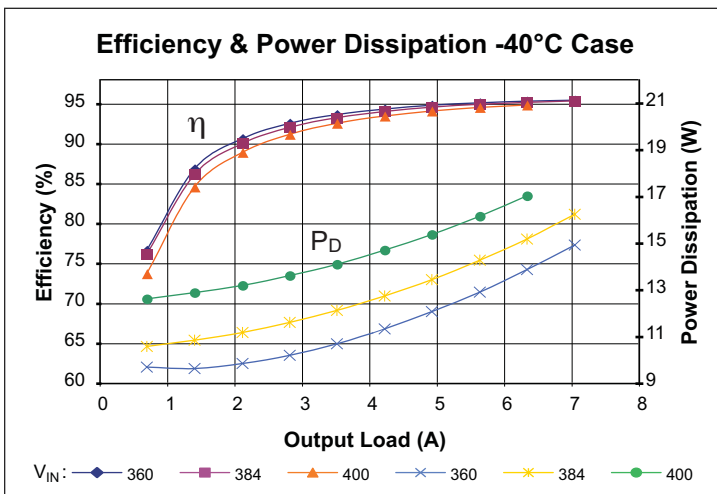
Figure 3 – *Efficiency and power dissipation at -40°C (case); V_{IN}*

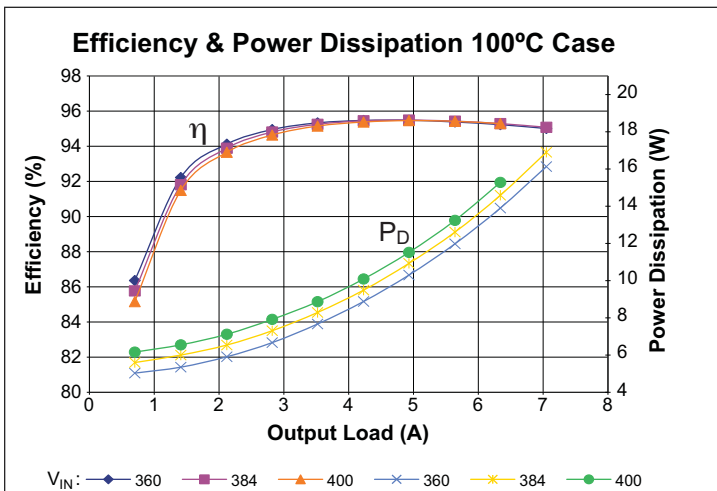## Efficiency & Power Dissipation 25°C Case
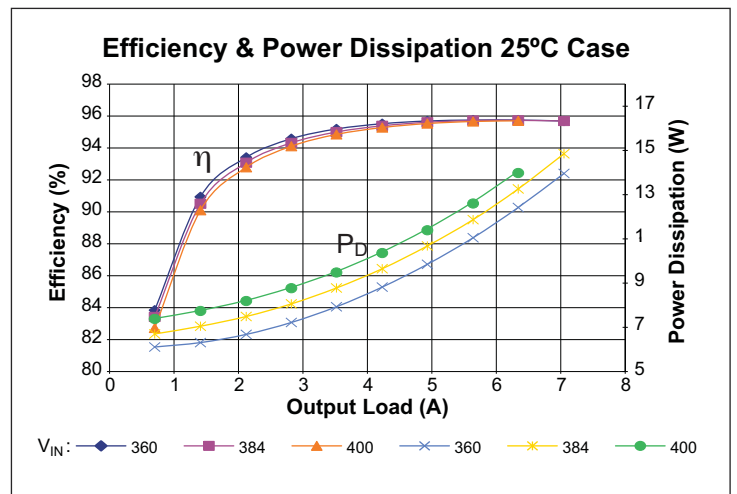
Figure 4 – *Efficiency and power dissipation at 25°C (case); V_{IN}*

Efficiency & Power Dissipation 100°C Case

Figure 5 – *Efficiency and power dissipation at 100°C (case); V_{IN}*

Rout vs Case Temperature
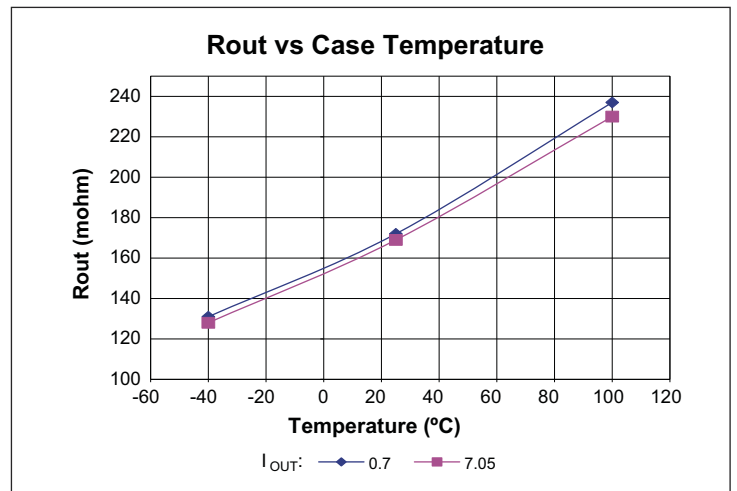
Figure 6 – *R_{OUT} vs. temperature vs. I_{OUT}*
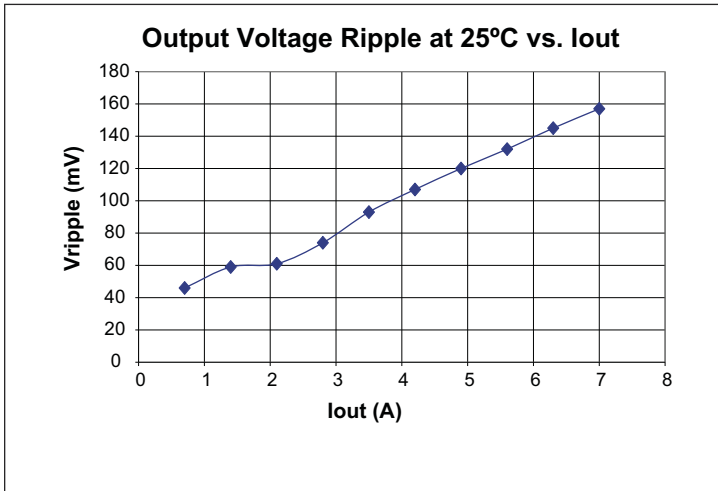
Figure 7 – *Vripple vs. I$_{OUT}$; 384 Vin, no external capacitance*

CH1 V$_{OUT}$: 20 V/div
CH2 V$_{PC}$: 2 V/div
Timebase: 200 μs/div
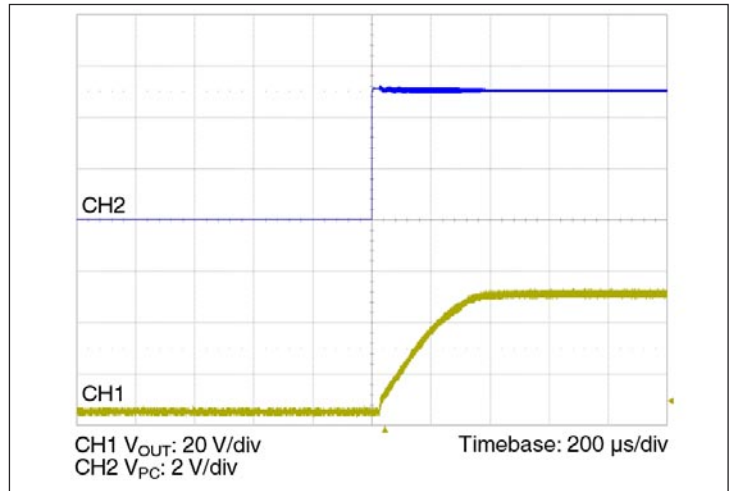
Figure 8 – *PC to V$_{OUT}$ startup waveform*

CH1 V$_{OUT}$: 20 V/div
Timebase: 100 ms/div
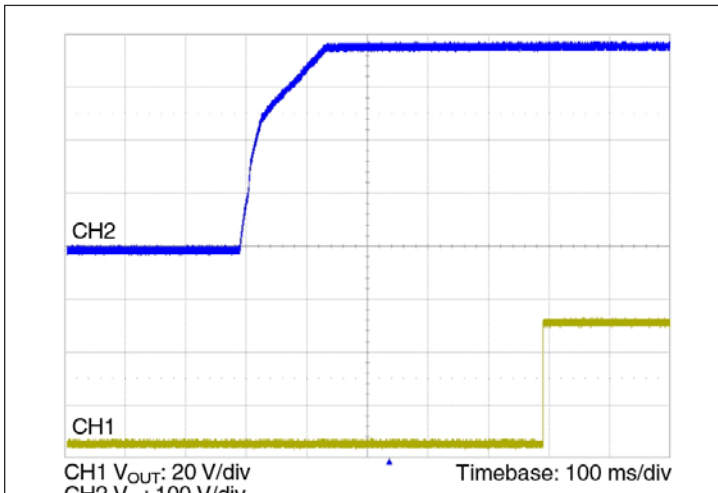
Figure 9 – *V$_{IN}$ to V$_{OUT}$ startup waveform*

CH1 V$_{OUT}$: 100 mV
CH2 I$_{IN}$: 500 mA
Timebase: 500 ns/div
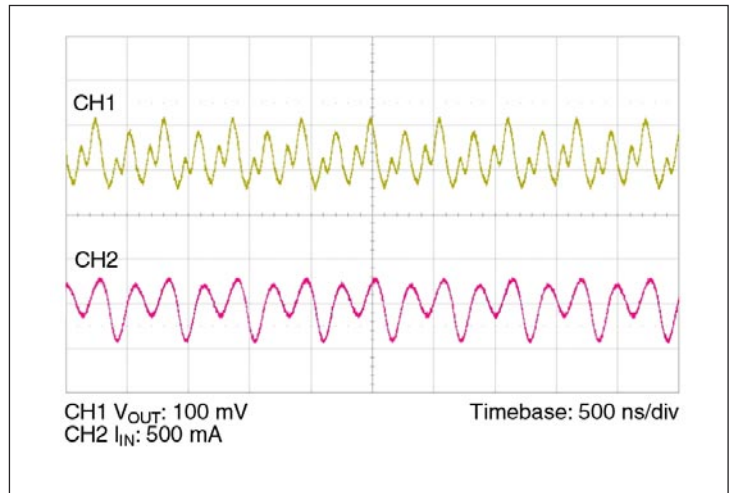
Figure 10 – *Output voltage and input current ripple, 384 Vin, 325 W no C$_{OUT}$*

CH1 V$_{OUT}$: 5 V/div
CH2 I$_{OUT}$: 5 A/div
CH3 V$_{IN}$: 20 V/div
CH4 I$_{IN}$: 1 A/div
Timebase: 2 μs/div
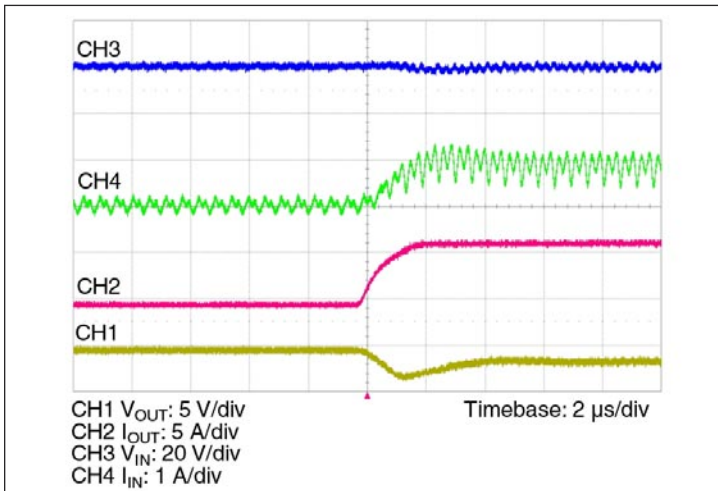
Figure 11 – *Positive load transient (0 – 7.07 A)*

CH1 V$_{OUT}$: 5 V/div
CH2 I$_{OUT}$: 5 A/div
CH3 V$_{IN}$: 20 V/div
CH4 I$_{IN}$: 1 A/div
Timebase: 2 μs/div
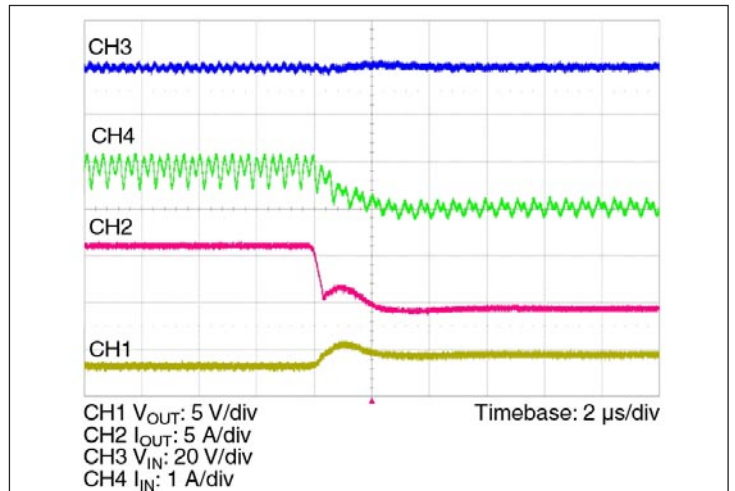
Figure 12 – *Negative load transient (7.07 A – 0 A)*

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CH1 V_OUT: 2 V/div
CH2 V_PC: 1 V/div
Timebase: 500 μs/div
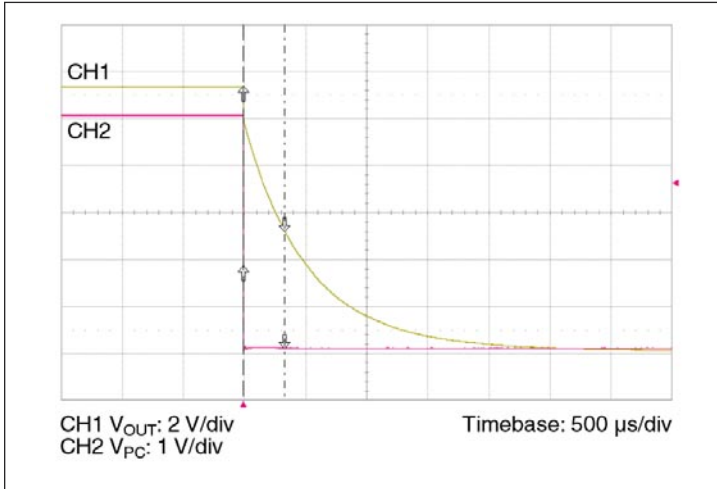
Figure 13 – PC disable waveform, 384 V_{IN}, 100 μF C_{OUT} full load
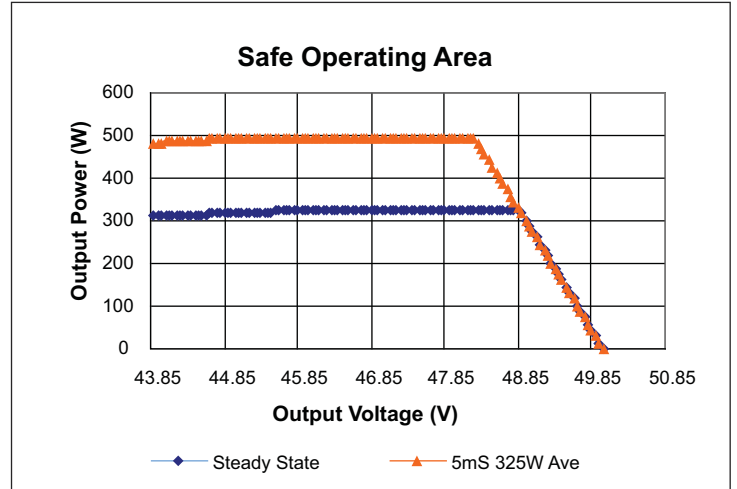
Figure 14 – Safe Operating Area vs. V_{OUT}

2.0 PACKAGE/MECHANICAL SPECIFICATIONS

All specifications are at **T_J = 25°C** unless otherwise noted. See associated figures for general trend data.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Length	L		32.4 / 1.27	32.5 / 1.28	32.6 / 1.29	mm/in
Width	W		21.7 / 0.85	22.0 / 0.87	22.3 / 0.89	mm/in
Height	H		6.48 / 0.255	6.73 / 0.265	6.98 / 0.275	mm/in
Volume	Vol	No Heatsink		4.81 / 0.295		cm³/in³
Footprint	F	No Heatsink		7.3 / 1.1		cm²/in²
Power Density	P_D	No Heatsink		1100		W/in³
				68		W/cm³
Weight	W			0.5/14		oz/g
Lead Finish		Nickel (0.51-2.03 μm)				μm
		Palladium (0.02-0.15 μm)				
		Gold (0.003-0.05 μm)				
Operating Temperature	T_J		-40		125	°C
Storage Temperature	T_{ST}		-40		125	°C
Thermal Capacity				9		Ws/°C
Peak Compressive Force Applied to Case (Z-axis)		No J-lead support		5	6	lbs
Moisture Sensitivity Level		MSL Level 5	5			
ESD Rating	ESD_{HBM}	Human Body Model[a]	1500			V_{DC}
	ESD_{MM}	Machine Model[b]	400			
Peak Temperature During Reflow					225	°C
Peak Time Above 183°C					150	s
Peak Heating Rate During Reflow				1.5	3	°C/s
Peak Cooling Rate Post Reflow				1.5	6	°C/s
Thermal Impedance	$\varnothing_{JC}$	Min Board Heatsinking		1.1	1.5	°CW

[a] JEDEC JESD 22-A114C.01
[b] JEDED JESD 22-A115-A

2.1 MECHANICAL DRAWING

TOP VIEW (COMPONENT SIDE)

BOTTOM VIEW

NOTES:
1. DIMENSIONS ARE $\frac{mm}{inch}$.
2. UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
   .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
3. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

2.2 RECOMMENDED LAND PATTERN

RECOMMENDED LAND PATTERN
(COMPONENT SIDE SHOWN)

NOTES:
1. DIMENSIONS ARE $\frac{mm}{inch}$.
2. UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
   .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
3. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

3.0 POWER, VOLTAGE, EFFICIENCY RELATIONSHIPS

Because of the high frequency, fully resonant SAC topology, power dissipation and overall conversion efficiency of BCM converters can be estimated as shown below.

Key relationships to be considered are the following:

1. Transfer Function

   a. No load condition

   $$V_{OUT} = V_{IN} \bullet K \qquad \textbf{Eq. 1}$$

   Where K (transformer turns ratio) is constant for each part number

   b. Loaded condition

   $$V_{OUT} = V_{in} \bullet K - I_{OUT} \bullet R_{OUT} \qquad \textbf{Eq. 2}$$

2. Dissipated Power
   The two main terms of power losses in the BCM module are:

   - No load power dissipation (P_{NL}) defined as the power used to power up the module with an enabled power train at no load.
   - Resistive loss (R_{OUT}) refers to the power loss across the BCM modeled as pure resistive impedance.

   $$P_{DISSIPATED} \approx P_{NL} + P_{R_{OUT}} \qquad \textbf{Eq. 3}$$

Therefore, with reference to the diagram shown in Figure 15

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \qquad \textbf{Eq. 4}$$

Notice that R_{OUT} is temperature and input voltage dependent and P_{NL} is temperature dependent (See Figure 15).
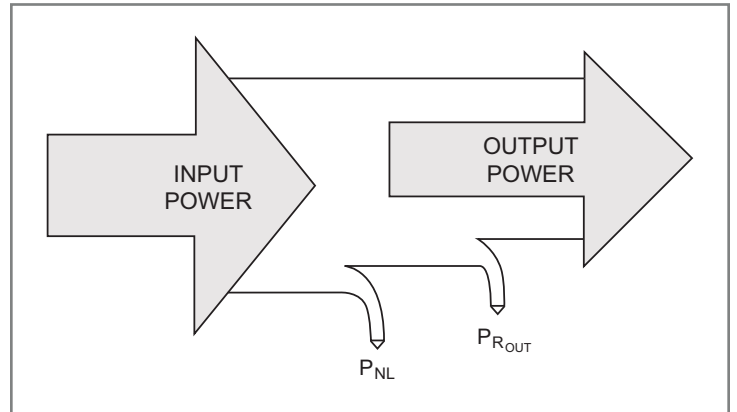
Figure 15 – *Power transfer diagram*

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} = \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}} = 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}} \right) \qquad \textbf{Eq. 5}$$

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4.0 OPERATING
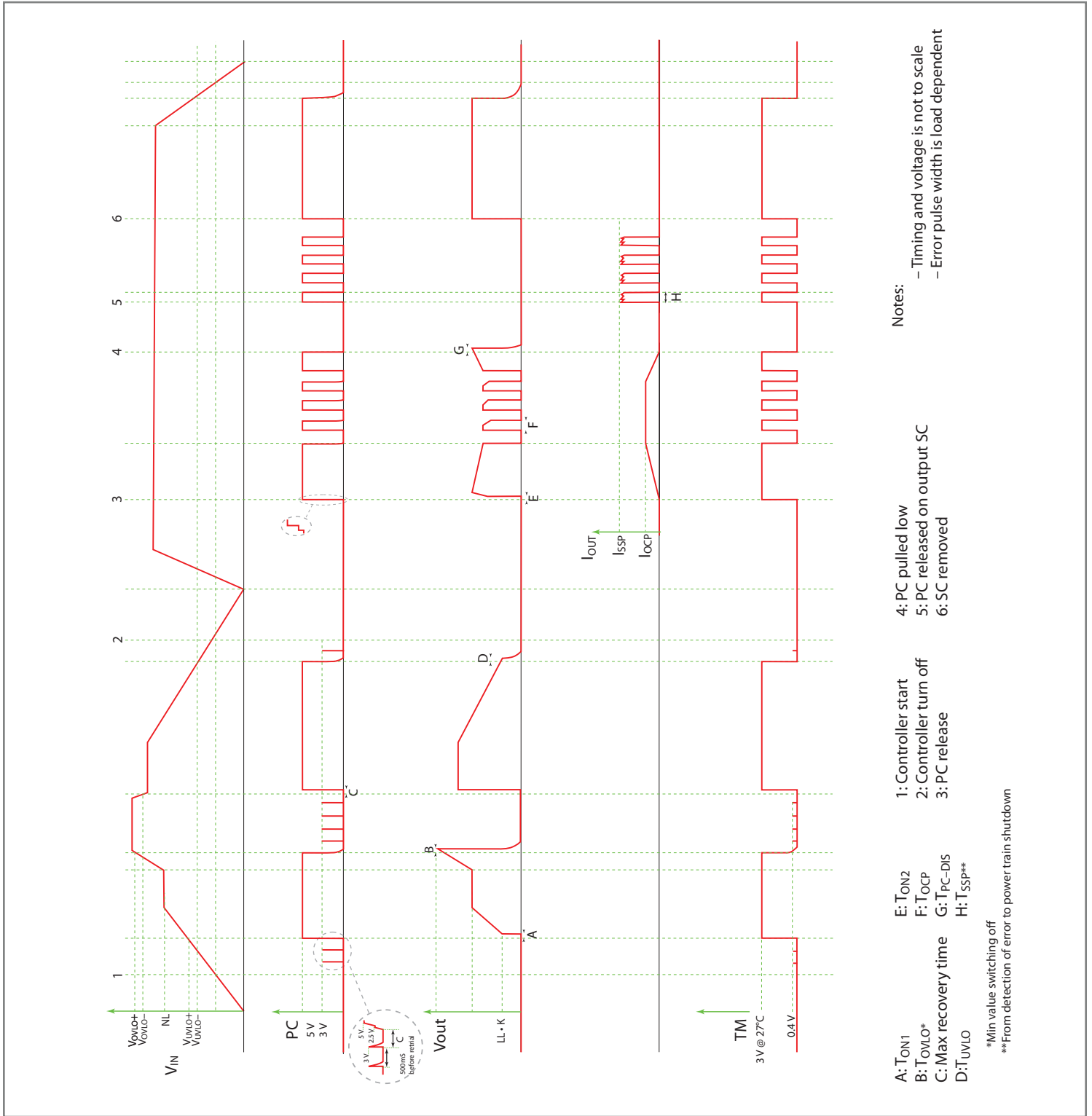
Figure 16 – Timing diagram

5.0 USING THE CONTROL SIGNALS TM AND PC

The PC control pin can be used to accomplish the following functions:

- **Delayed start:** At start-up, PC pin will source a constant 100 uA current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5 V threshold for module start.

- **Synchronized start up:** In a parallel module array, PC pins shall be connected in order to ensure synchronous start of all the units. While every controller has a calibrated 2.5 V reference on PC comparator, many factors might cause different timing in turning on the 100 uA current source on each module, i.e.:

  – Different V_{IN} slew rate

  – Statistical component value distribution

  By connecting all PC pins, the charging transient will be shared and all the modules will be enabled synchronously.

- **Auxiliary voltage source:** Once enabled in regular operational conditions (no fault), each BCM PC provides a regulated 5 V, 2 mA voltage source.

- **Output Disable:** PC pin can be actively pulled down in order to disable module operations. Pull down impedance shall be lower than 400 Ω and toggle rate lower than 1 Hz.

- **Fault detection flag:** The PC 5 V voltage source is internally turned off as soon as a fault is detected. After a minimum disable time, the module tries to re-start, and PC voltage is re-enabled. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of PC signal.

  It is important to notice that PC doesn't have current sink capability (only 150 kΩ typical pull down is present), therefore, in an array, PC line will not be capable of disabling all the modules if a fault occurs on one of them.

The temperature monitor (TM) pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- **Monitor the control IC temperature:** The temperature in Kelvin is equal to the voltage on the TM pin scaled by x100. (i.e. 3.0 V = 300 K = 27°C). It is important to remember that V•I chips are multi-chip modules, whose temperature distribution greatly vary for each part number as well with input/output conditions, thermal management and environmental conditions. Therefore, TM cannot be used to thermally protect the system.

- **Fault detection flag:** The TM voltage source is internally turned off as soon as a fault is detected. After a minimum disable time, the module tries to re-start, and TM voltage is re-enabled.

6.0 FUSE SELECTION

V•I Chips are not internally fused in order to provide flexibility in configuring power systems. Input line fusing of V•I Chips is recommended at system level, in order to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum BCM current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommended fuse: ≤2.5 A Bussmann PC-Tron or SOC type 36CFA.

7.0 CURRENT SHARING

The SAC topology bases its performance on efficient transfer of energy through a transformer, without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array (with same K factor), the BCM module will inherently share the load current with parallel units, according to the equivalent impedance divider that the system implements from the power source to the point of load.

It is important to notice that, when successfully started, BCMs are capable of bidirectional operations (reverse power transfer is enabled if the BCM input falls within its operating range and the BCM is otherwise enabled). In parallel arrays, because of the resistive behavior, circulating currents are never experienced (energy conservation law).

General recommendations to achieve matched array impedances are (see also AN016 for further details):

- to dedicate common copper planes within the PCB to deliver and return the current to the modules
- to make the PCB layout as symmetric as possible
- to apply same input/output filters (if present) to each unit
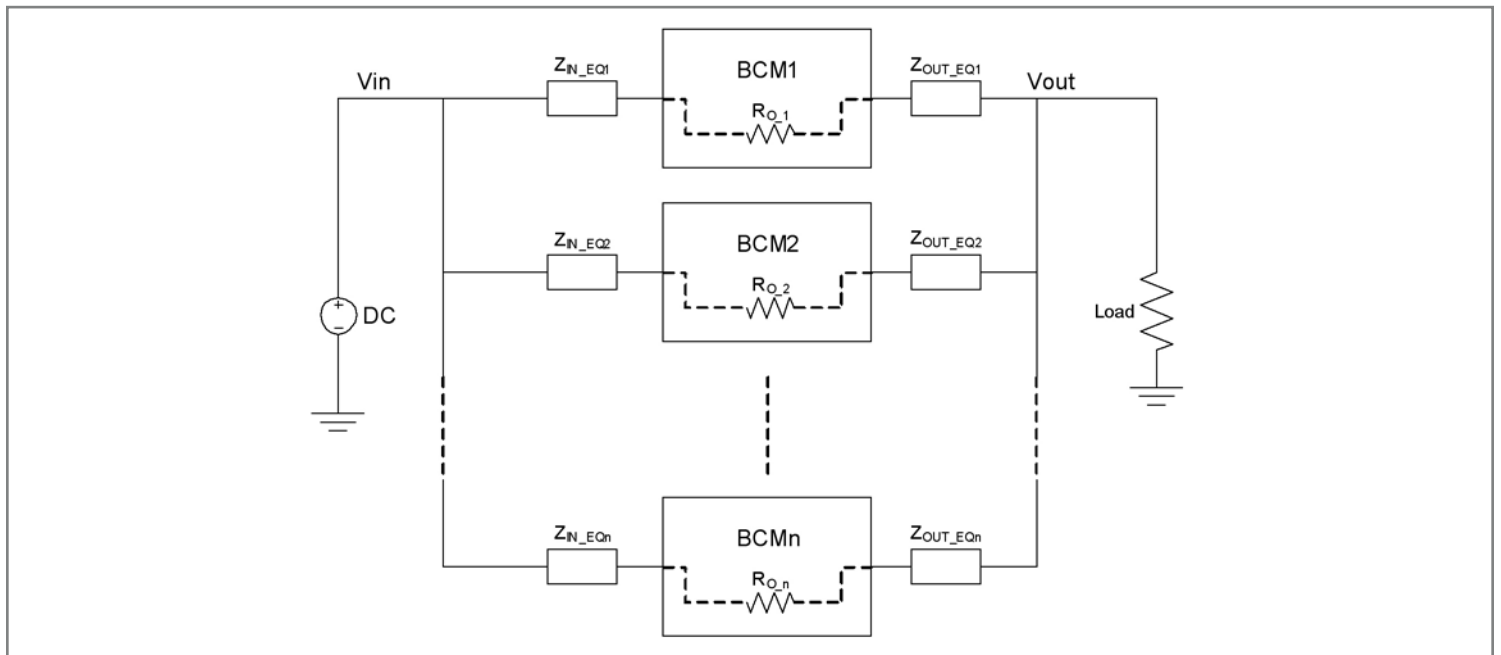
Figure 17 – BCM Array

8.0 INPUT AND OUTPUT FILTER DESIGN

A major advantage of SAC systems versus conventional PWM converters is that the transformers do not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current, and efficiently transfers charge through the isolation transformer. A small amount of capacitance, embedded in the input and output stages of the module, is sufficient for full functionality and is key to achieve power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. Guarantee low source impedance:

   To take full advantage of the BCM dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be as high as 1 µF in series with 0.3 Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

2. Further reduce input and/or output voltage ripple without sacrificing dynamic response:

   Given the wide bandwidth of the BCM, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the BCM multiplied by its K factor. This is illustrated in Figures 11 and 12.

3. Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:

   The V•I Chip input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it. A criterion for protection is the maximum amount of energy that the input or output switches can tolerate if avalanched.

Total load capacitance at the output of the BCM shall not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the BCM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the BCM. At frequencies <500 kHz the BCM appears as an impedance of R_{OUT} between the source and load. Within this frequency range capacitance at the input appears as effective capacitance on the output per the relationship defined in Eq. 5.

$$C_{OUT} = \frac{C_{IN}}{K^2} \qquad \textbf{Eq. 6}$$

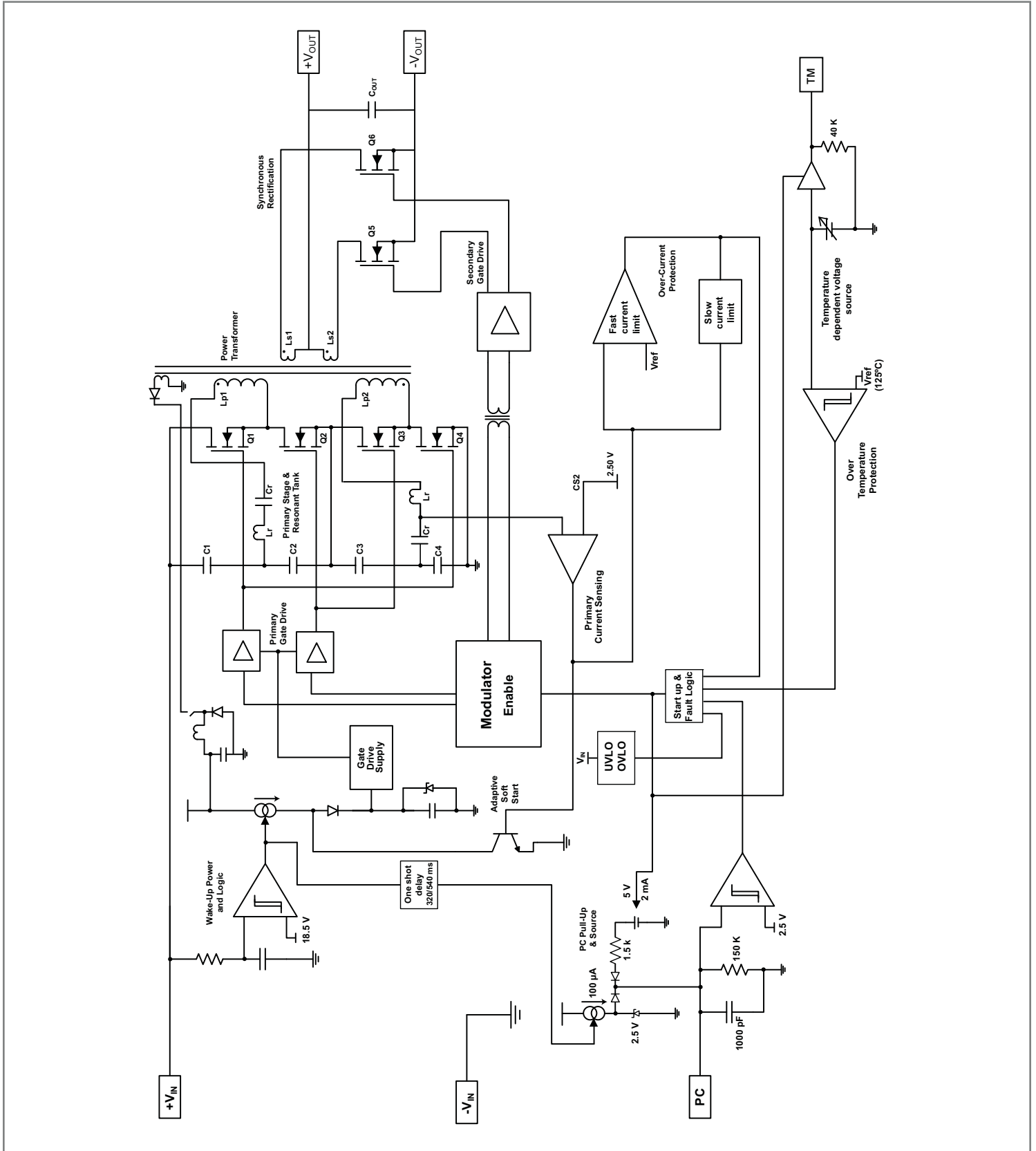This enables a reduction in the size and number of capacitors used in a typical system.

Figure 18 – BCM block diagram

Warranty

Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

Specifications are subject to change without notice.

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