REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change V_{IH1}, V_{IH2}, and t_{PHL13}.	1985 Jan 2	
B	Change end-point electrical test requirements in table II. Extensive changes to table I. Editorial changes throughout.	1986 Apr 14	
C	Change to military drawing format. Changes to table I. Change to timing diagram. Change to vendor similar part numbers. Editorial changes throughout.	1987 Apr 6	
D	Correct parameter name for t_{PHL13}. Correct vendor CAGE number and address. Add switching test circuits and input/output switching test waveforms. Editorial changes throughout. Change drawing CAGE code.	1989 Jan 21	

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	D	D																						
SHEET	22	23																						

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY:

DRAWING APPROVAL DATE: 24 AUGUST 1984

REVISION LEVEL: D

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, N-CHANNEL, DUAL SERIAL INPUT/OUTPUT CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	83015

SHEET 1 OF 23

DESC FORM 193-1
SEP 87

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1140

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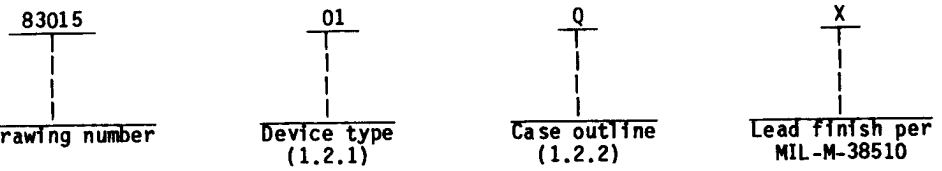
1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Clock frequency	Circuit function
01	Z8442A/Z0844204	4.0 MHz	Dual serial input/ output controller
02	Z8442/Z0844202	2.5 MHz	

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

V_{CC} supply voltage range (V_{CC} - GND)	-0.3 V dc to +7 V dc
Voltage on any pin (referenced to ground)	-0.3 V dc to +7 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation at -55°C	1.0 W
Maximum power dissipation at +125°C	0.5 W
Lead temperature (soldering, 5 seconds)	+270°C
Maximum junction temperature (T_J)	+170°C
Thermal resistance, junction to case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH}):	
Logic inputs	2.2 V dc
Clock input	V_{CC} -0.6 V dc
Maximum low-level input voltage (V_{IL}):	
Logic inputs	0.8 V dc
Clock input	0.45 V dc
Frequency of operation:	
Device type 01 circuit	0.5 to 4.0 MHz
Device type 02 circuit	0.5 to 2.5 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Clock rise time	30 ns maximum
Clock fall time	30 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Conditions (T_C = -55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Group A subgroups	Reference number	Limits		Unit
					Min	Max	
Clock input low voltage	V_{IL1}		1, 2, 3		1/ -0.3	0.45	V
Clock input high voltage	V_{IH1}		1, 2, 3		V_{CC}- 0.6 V	1/ V_{CC}+ 0.3 V	V
Input low voltage	V_{IL2}		1, 2, 3		1/ -0.3	0.8	V
Input high voltage	V_{IH2}		1, 2, 3		2.2	1/ V_{CC}	V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA	1, 2, 3			1/ 0.4	V
Output high voltage	V_{OH}	I_{OH} = -250 µA	1, 2, 3		1/ 2.4		V
Power supply current	I_{CC}	Outputs open	1, 2, 3			182	mA
Output leakage current low, open drain outputs	I_{LOL}	V_{OUT} = 0.4 V	1, 2, 3		-10	+10	µA
Output leakage current high, open drain outputs	I_{LOH}	V_{OUT} = 2.4 V	1, 2, 3		-10	+10	µA
$\overline{SYNCA}$ pin leakage current low	I_{IL1}	V_{IN} = 0.4 V	1, 2, 3		-40	+10	µA
$\overline{SYNCA}$ pin leakage current high	I_{IH1}	V_{IN} = 2.4 V	1, 2, 3		-40	+10	µA
Input low current (input and bi-directional)	I_{IL2}	V_{IN} = 0.4 V	1, 2, 3		-10	+10	µA
Input high current (input and bi-directional)	I_{IH2}	V_{IN} = 2.4 V	1, 2, 3		-10	+10	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions (T_C = -55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)		Group A subgroups	Reference number 2/	Limits Min	Limits Max	Unit
Clock capacitance	C_{CLK}	T_C = +25°C; f = 1 MHz see 4.3.1c Unmeasured pins returned to ground		4			40	pF
Input capacitance	C_I						5	
Output capacitance	C_O						15	
Functional tests		See 4.3.1d		7, 8				
Maximum frequency	f_{MAX}	C_L = 100 pF ±10%	Device 01	9, 10, 11		1/ 4.0		MHz
			Device 02			1/ 2.5		MHz
Clock cycle time 3/ 4/	t_{CYC1}	C_L = 100 pF ±10% 5/	Device 01	9, 10, 11	1	250	1/ 4000	ns
			Device 02			400	1/ 4000	
$\overline{TxC}$ cycle time 1/	t_{CYC2}			9, 10, 11	24	400	∞	ns
$\overline{RxC}$ cycle time 1/	t_{CYC3}			9, 10, 11	30	400	∞	ns
Clock fall time 1/	t_{fC}			9, 10, 11	3		30	ns
Clock rise time 1/	t_{rC}			9, 10, 11	4		30	ns
Clock width high 1/ 6/	t_{PWH1}		Device 01	9, 10, 11	2	105	2000	ns
			Device 02			170	2000	
Clock width low 1/ 7/	t_{PWL1}		Device 01	9, 10, 11	5	105	2000	ns
			Device 02			170	2000	
Pulse width high 1/ ($\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$)	t_{PWH2}			9, 10, 11	22	200		ns
Pulse width low 1/ ($\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$)	t_{PWL2}			9, 10, 11	23	200		ns
$\overline{TxC}$ width high 1/	t_{PWH3}			9, 10, 11	26	180	∞	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions (T_C = -55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)		Group A subgroups	Reference number 2/	Limits Min	Limits Max	Unit
$\overline{TxC}$ width low 1/	t_{PWL3}	C_L = 100 pF ±10%		9, 10, 11	25	180	∞	ns
$\overline{RxC}$ width high 1/	t_{PWH4}			9, 10, 11	32	180	∞	ns
$\overline{RxC}$ width low 1/	t_{PWL4}			9, 10, 11	31	180	∞	ns
$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to clock setup	t_{SHL1} t_{SLH1}	5/	Device 01	9, 10, 11	6	145		ns
			Device 02			160		
$\overline{IORQ}$, $\overline{RD}$ to clock ↑ setup	t_{SHL2} t_{SLH2}		Device 01	9, 10, 11	7	115		ns
			Device 02			240		
Data in to clock ↑ setup (Write or $\overline{MI}$ cycle)	t_{SHL3} t_{SLH3}			9, 10, 11	9	50		ns
RxD to $\overline{RxC}$ ↑ setup (x1 mode) 1/	t_{SHL4} t_{SLH4}			9, 10, 11	33	0		ns
$\overline{MI}$ to clock ↑ setup	t_{SHL5} t_{SLH5}		Device 01	9, 10, 11	12	90		ns
			Device 02			210		
IEI to $\overline{IORQ}$ ↓ setup (INTA cycle) 1/	t_{SHL6} t_{SLH6}		Device 01	9, 10, 11	13	140		ns
			Device 02			200		
$\overline{SYNC}$ to $\overline{RxC}$ ↑ setup (External SYNC 1/ modes)	t_{SHL7} t_{SLH7}		Device 01	9, 10, 11	38	-100		ns
			Device 02			-100		
$\overline{RxC}$ ↑ to RxD hold (x1 mode)	t_{HHL1} t_{HLH1}			9, 10, 11	34	140		ns
Any unspecified 1/ hold when setup specified	t_{HHL2} t_{HLH2}			9, 10, 11	21	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions (T_C = -55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)		Group A subgroups	Reference number 2/	Limits Min	Limits Max	Unit
Clock ↑ to data out delay	t_{PHL1} t_{PLH1}	C_L = 100 pF ±10%	Device 01	9, 10, 11	8		220	ns
			Device 02				240	
$\overline{RD}$ ↑ to data out float delay 1/	t_{PHZ1} t_{PLZ1}		Device 01	9, 10, 11	10		110	ns
			Device 02				230	
$\overline{IORQ}$ 1/ ↓ to data out delay (INTA cycle)	t_{PHL2} t_{PLH2}		Device 01	9, 10, 11	11		160	ns
			Device 02				340	
$\overline{TxC}$ ↓ to TxD delay (x1 mode)	t_{PHL3} t_{PLH3}		Device 01	9, 10, 11	27		300	ns
			Device 02				400	
$\overline{MI}$ 1/ ↓ to IEO ↓ delay (Interrupt before $\overline{MI}$)	t_{PHL4}		Device 01	9, 10, 11	14		190	ns
			Device 02				300	
IEI ↑ to IEO ↑ (After ED decode) 1/	t_{PLH4}	5/	Device 01	9, 10, 11	15		100	ns
			Device 02				150	
IEI ↓ to IEO ↓ delay	t_{PHL5}		Device 01	9, 10, 11	16		100	ns
			Device 02				150	
Clock ↑ to $\overline{INT}$ ↓ delay	t_{PHL6}			9, 10, 11	17		200	ns
$\overline{IORQ}$ 1/ ↓ to $\overline{CE}$ ↓ to $\overline{W/RDY}$ delay (Wait mode)	t_{PHL7}		Device 01	9, 10, 11	18		210	ns
			Device 02				300	
Clock ↑ to $\overline{W/RDY}$ ↓ delay (Ready mode)	t_{PHL8}		Device 01	9, 10, 11	19		120	ns
			Device 02				1/ 120	
Clock ↓ to $\overline{W/RDY}$ 1/ float delay (Wait mode)	t_{PLZ2}		Device 01	9, 10, 11	20		130	ns
			Device 02				150	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions (T_C = -55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Group A subgroups	Reference number 2/	Limits Min	Limits Max	Unit
$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ 1/ delay (Ready mode)	t_{PHL9}	C_L = 100 pF ±10% 5/	9, 10, 11	28	5	9	8/
$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ 1/ delay	t_{PHL10}		9, 10, 11	29	5	9	8/
$\overline{RxC}$ ↓ to $\overline{W/RDY}$ ↓ 1/ delay (Ready mode)	t_{PHL11}		9, 10, 11	35	10	13	8/
$\overline{RxC}$ ↓ to $\overline{INT}$ ↓ delay 1/	t_{PHL12}		9, 10, 11	36	10	13	8/
$\overline{RxC}$ to $\overline{SYNC}$ setup (Output mode)	t_{PHL13}		9, 10, 11	37	4	7	8/

1/ If not tested, shall be guaranteed to the specified limits.

2/ The reference number refers to the position where the parameters being tested appears on figure 2.

3/ In all modes, the system clock rate must be at least five times the maximum data rate.

4/ RESET must be active a minimum of one complete clock cycle.

5/ Figure 2 represents the electrical performance characteristics associated with the ac limits shown in table I.

6/ $t_{PWH1} = t_{CYC} - t_{PWL1} - t_{rC} - t_{fC}$.

7/ $t_{PWL1} = t_{CYC} - t_{PWH1} - t_{rC} - t_{fC}$.

8/ Clock periods (system clock).

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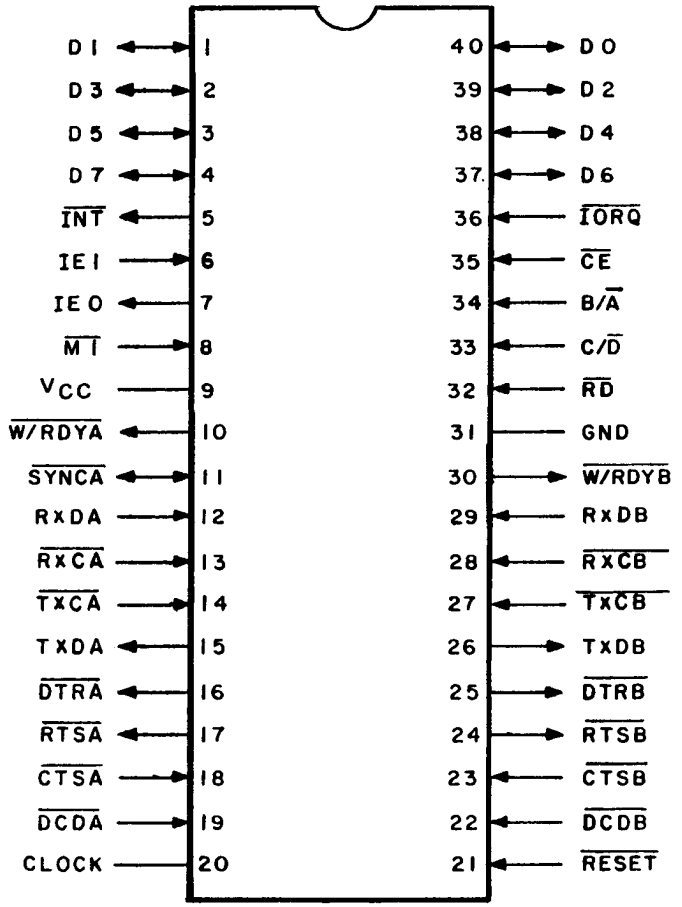
Device types 01 and 02

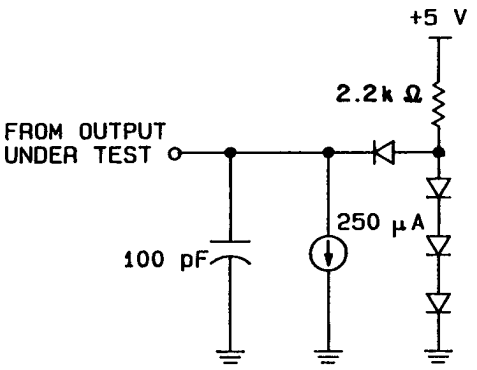


CASE Q

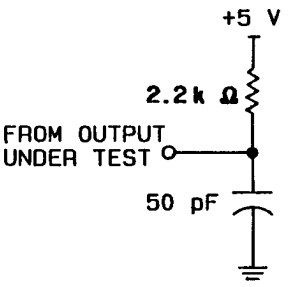
FIGURE 1. Terminal connections (top view).

Switching test circuits

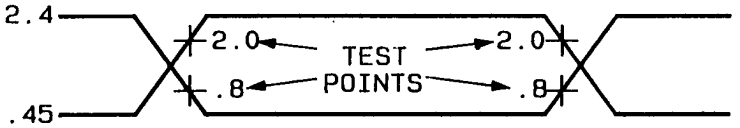
Standard test load



Open drain test load

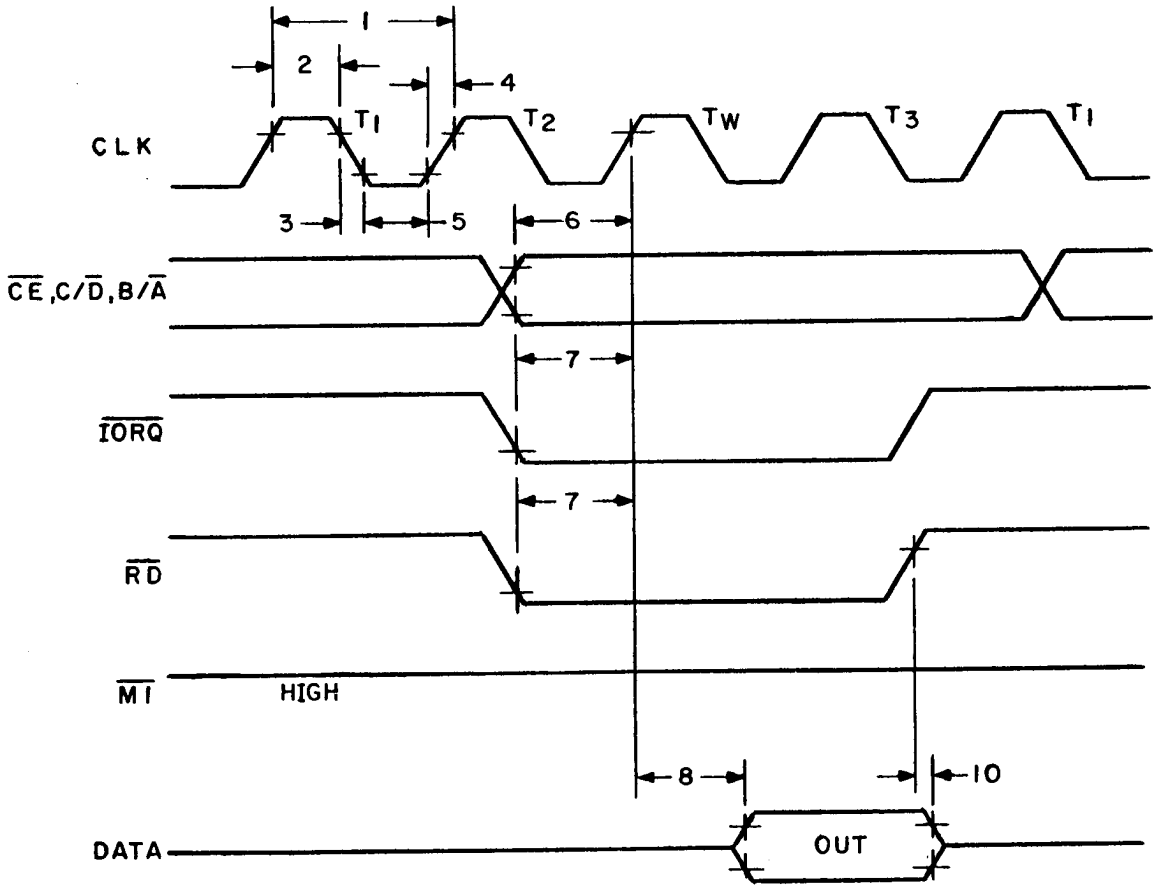


Switching test input/output waveform



AC testing: Inputs are driven at 2.4 V for logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for logic "0".

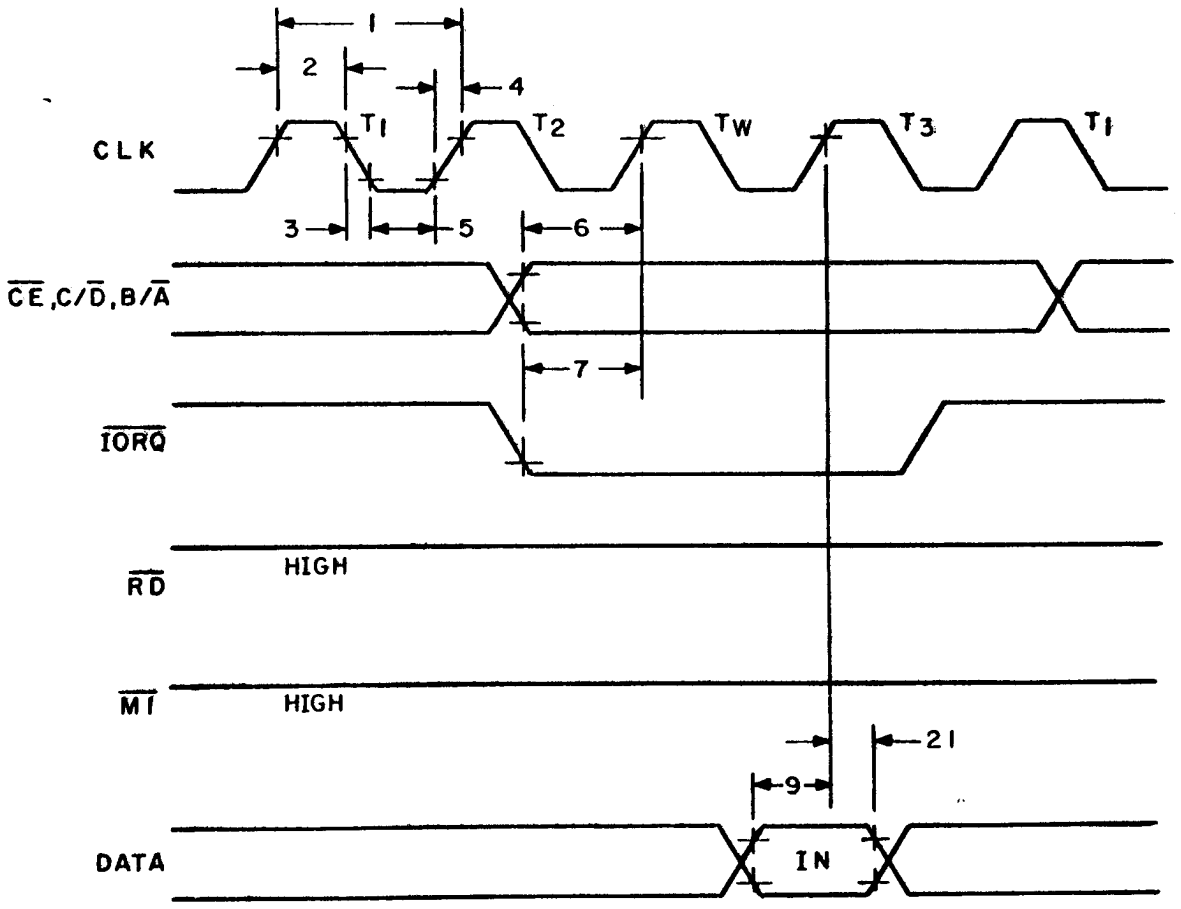
FIGURE 2. Switching test circuits and timing diagrams.



Read cycle

NOTE: Optional condition occurs only when any combination of these inputs must change state to reprogram during read/write operation.

FIGURE 2. Switching test circuits and timing diagrams - Continued.



Write cycle

FIGURE 2. Switching test circuits and timing diagrams - Continued.

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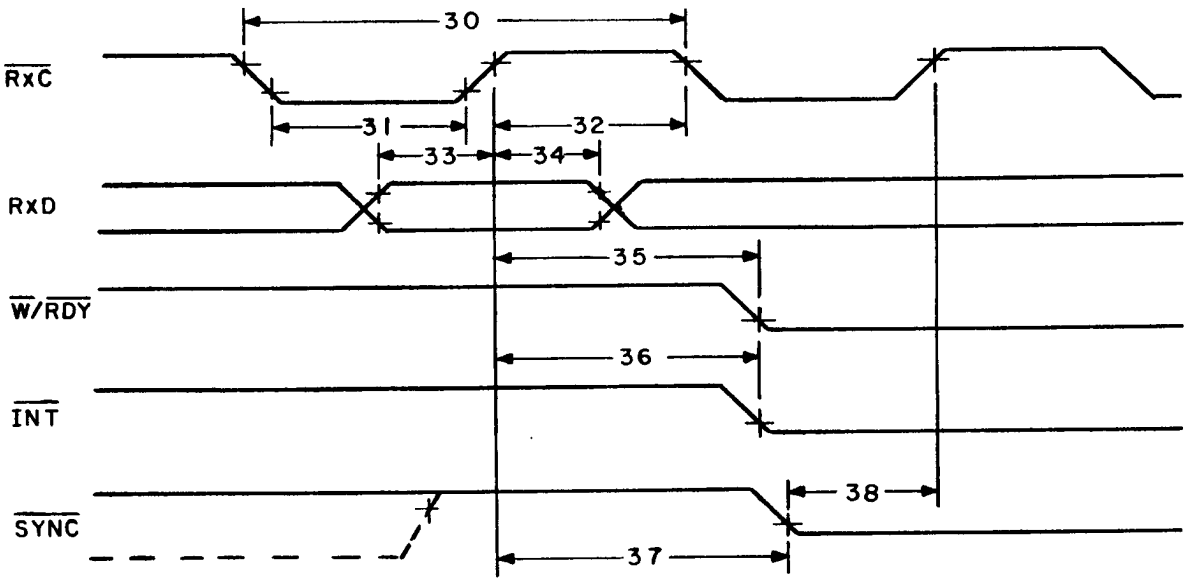
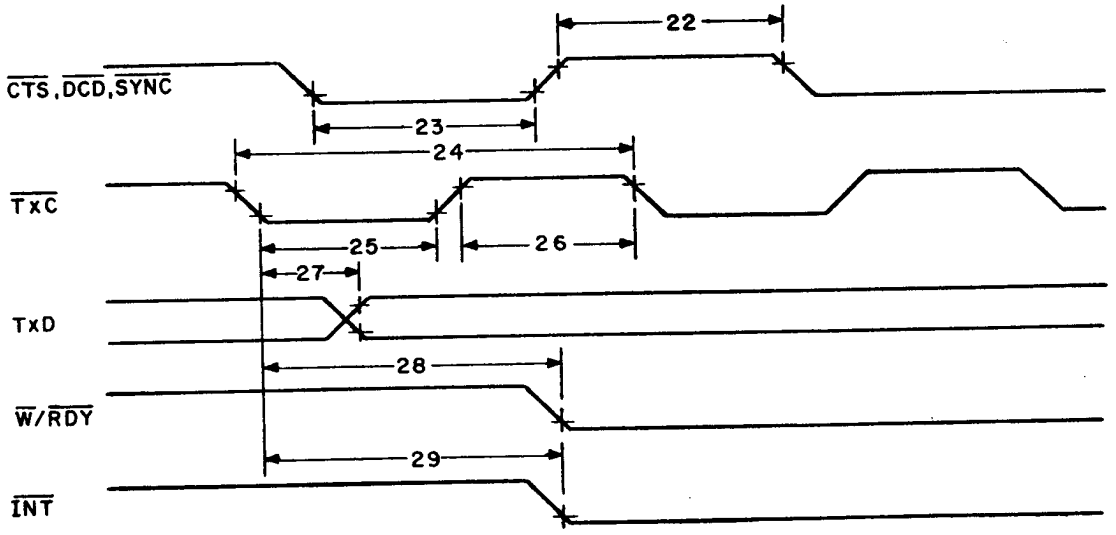


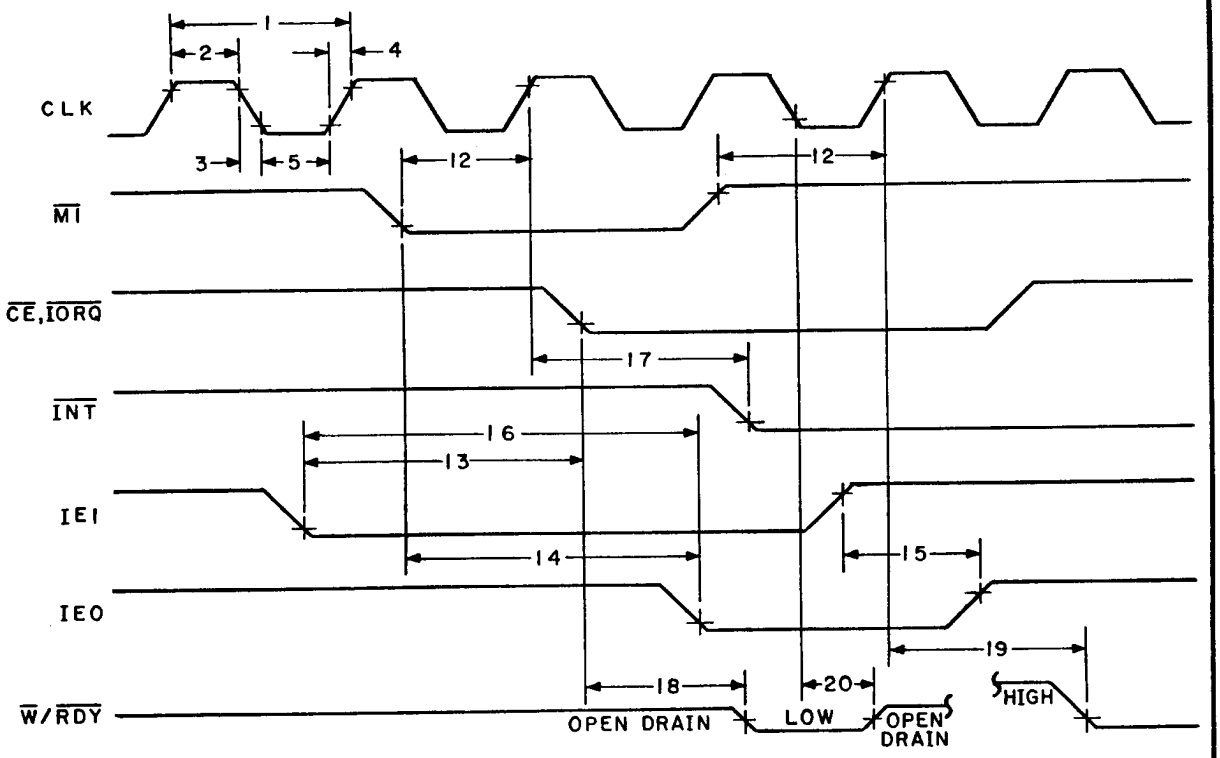
Receiver serial data

FIGURE 2. Switching test circuits and timing diagrams - Continued.



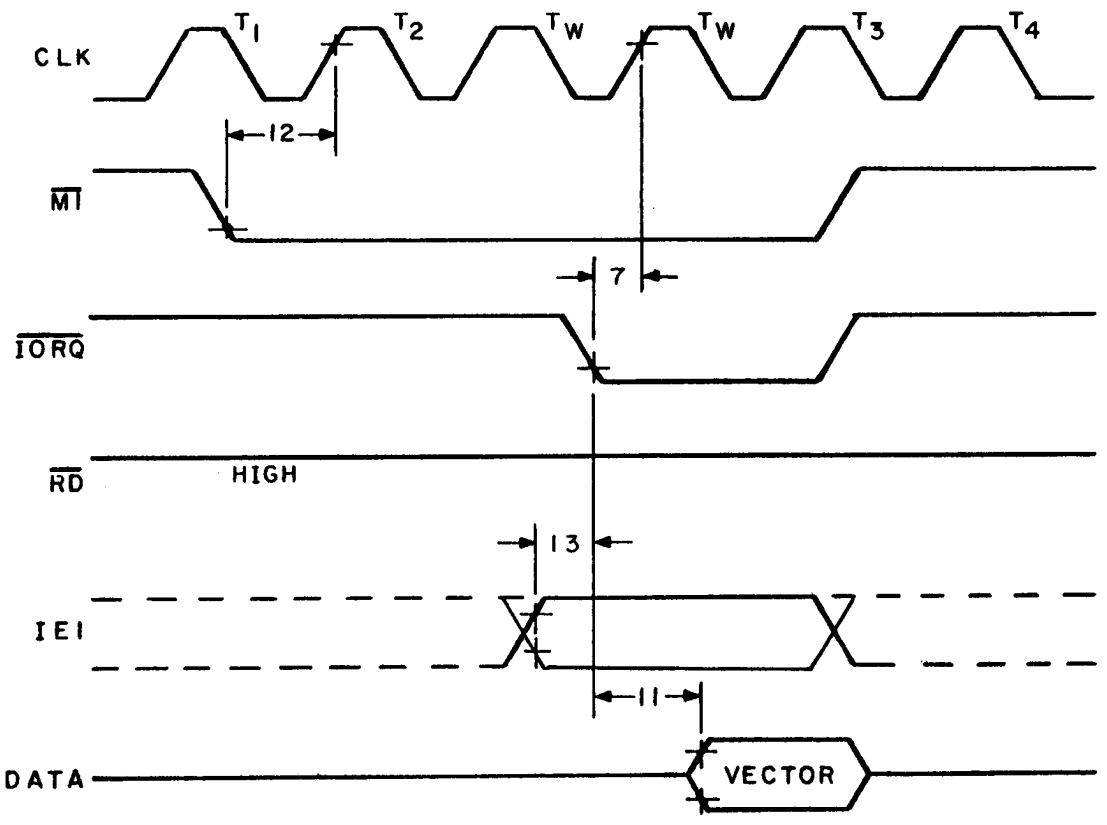
Transmitter serial data and modem control

FIGURE 2. Switching test circuits and waveforms - Continued.



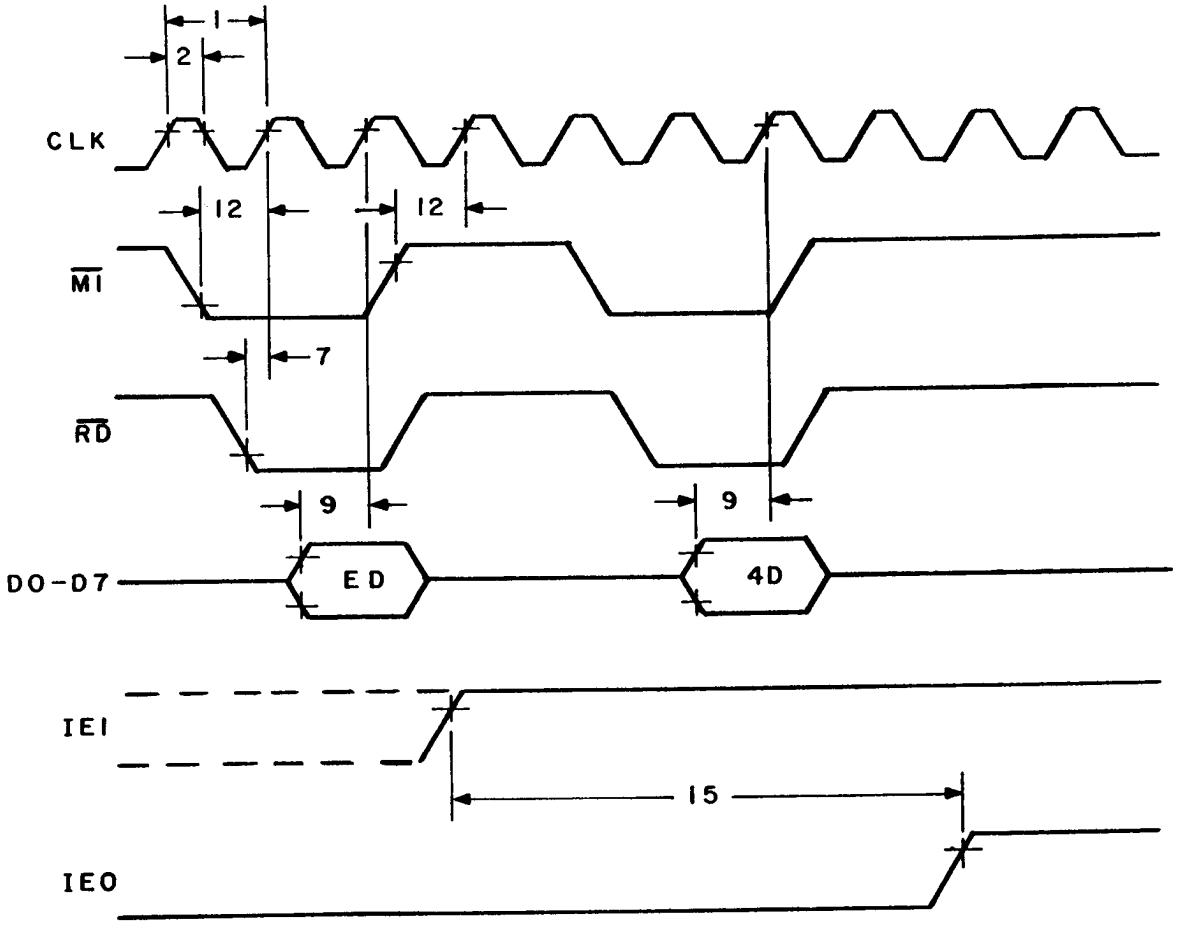
Interrupt request

FIGURE 2. Switching test circuits and waveforms - Continued.



Interrupt acknowledge cycle

FIGURE 2. Switching test circuits and waveforms - Continued.



Return from interrupt cycle

FIGURE 2. Switching test circuits and waveforms - Continued.

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{CLK}, C_I, and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects is required.

d. Subgroup 7 and 8 functional testing shall include verification of instruction set. These tests form a part of the manufacturers test tape and shall be maintained and available from approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883 conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional description for this device shall be as follows:

System definitions

Symbol	Function
B/$\overline{A}$ (Channel A or B select)	Input, high selects channel B. This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.
C/$\overline{D}$ (Control or Data Select)	Input, high selects control. This input defines the type of information transfer performed between the CPU and the SIO. A high at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by the B/$\overline{A}$. A low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.
$\overline{CE}$ (Chip Enable)	Input, active low. A low level at this input enables the SIO to accept command or data input from the CPU during a write cycle, or to transmit data to the CPU during a ready cycle.
CLK (System Clock)	Input. The SIO uses the standard System Clock to synchronize internal signals. This is a single-phase clock.
$\overline{CTSA}$, $\overline{CTSB}$ (Clear to Send)	Inputs, active low. When programmed as Auto Enables, a low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-rise time signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.
D_0 - D_7 (System Data Bus)	Bidirectional, three-state. The system data bus transfers data and commands between the CPU and the SIO. D_0 is the least significant bit.
$\overline{DCDA}$, $\overline{DCDB}$ (Data Carrier Detect)	Inputs, active low. These pins function as Receiver Enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-rise time signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffering does not guarantee a specific noise-level margin.
$\overline{DTRA}$, $\overline{DTRB}$ (Data Terminal Ready)	Outputs, active low. These outputs follow the state programmed into SIO. They can also be programmed as general-purpose outputs.

IEI (Interrupt Enable In)	Input, active high. This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A high on this line indicates that no other device of high priority is being serviced by a CPU interrupt service routine.
IEO (Interrupt Enable Out)	Output, active high. IEO is high only if IEI is high and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.
$\overline{INT}$ (Interrupt Request)	Output, open drain, active low. When the SIO is requesting an interrupt, it pulls $\overline{INT}$ low.
$\overline{IORQ}$ (Input/Output Request)	Input from CPU, active low. $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$ and $\overline{RD}$ to transfer commands and data between the CPU and the SIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active, but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$. As mentioned previously, if $\overline{IORQ}$ and $\overline{MI}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.
$\overline{MI}$ (Machine Cycle)	Input from CPU, active low. When $\overline{MI}$ is active and $\overline{RD}$ is also active, the CPU is fetching an instruction from memory; when $\overline{MI}$ is active while $\overline{IORQ}$ is active, the SIO accepts $\overline{MI}$ and $\overline{IORQ}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the CPU.
$\overline{RxCA}$, $\overline{RxCB}$ (Receiver Clocks)	Inputs. Receive data is sampled on the rising edge of $\overline{RxC}$. The Receiver Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).
$\overline{RD}$ (Read Cycle Status)	Input from CPU, active low. If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with B/$\overline{A}$, $\overline{CE}$ and $\overline{IORQ}$ to transfer data from the SIO to the CPU.
RxDA, RxDB (Receive Data)	Inputs, active high. Serial data at TTL levels.
$\overline{RESET}$ (Reset)	Input, active low. A low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls high and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.

RTSA, RTSB (Request to Send)	Outputs, active low. When the RTS bit in Write Register 5 is set, the RTS output goes low. When the RTS bit is reset in the asynchronous mode, the output goes high after the transmitter is empty. In synchronous modes, the RTS pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.
SYNCA (Synchronization)	Input/output, active low. This pin can act either as input or output. In the asynchronous receive mode, it is an input similar to CTS and DCD. In this mode, the transitions on this line affect the state of the Sync/Hunt status bits in Read Register 0, but have no other function. In the External Sync mode, this line also acts as input. When external synchronization is achieved, SYNC must be driven low on the second rising edge or RxC after that rising edge of RxC on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for the two full Receive Clock cycles to activate the SYNC input. Once SYNC is forced low, it should be kept low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of RxC that immediately precedes the falling edge of SYNC in the External Sync mode. In the internal synchronization mode (Monosync and Bisync), this pin acts as an output that is active during the part of the receive clock (RxC) cycle in which sync characters are recognized. The sync condition is not latched, so this output is active each time a sync pattern is recognized, regardless of character boundaries.
TxCA, TxCB (Transmitter Clocks)	TxD changes from the falling edge of TxC. In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the CTC Counter Timer Circuit for programmable baud rate generation.
TxDA, TxDB (Transmit Data)	Outputs, active high. Serial data at TTL levels.
W/RDYA, W/RDYB (Wait/Ready A, Wait/Ready B)	Outputs, open drain, when programmed for Wait function; driven high and low when programmed for Ready function. These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number 2/
8301501QX	56708	Z0844204CMB 3/	M38510/48101BQX
8301502QX	56708	Z0844202CMB 4/	M38510/48102BQX

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Qualification requirement has been removed from this specification. (See MIL-STD-1562.)
3/ This part was previously designated as Z8442ACMB.
4/ This part was previously designated as Z8442CMB.

Vendor CAGE number	Vendor name and address
56708	Zilog, Incorporated 210 Hacienda Avenue Campbell, CA 95008

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