



Integrated Device Technology, Inc.

**CMOS STATIC RAM**  
**64K (8K x 8-BIT)**
**IDT7164S**  
**IDT7164L**

T-46-23-12

**FEATURES:**

- High-speed address/chip select access time
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (L Version only)
- Produced with advanced CMOS high-performance technology
- Inputs and outputs directly TTL-compatible
- Three-state outputs
- Available in:
  - 28-pin DIP, SOIC, SOJ, LCC and CERPACK
  - 32-pin LCC, and PLCC
- Military product compliant to MIL-STD-883, Class B

**DESCRIPTION:**

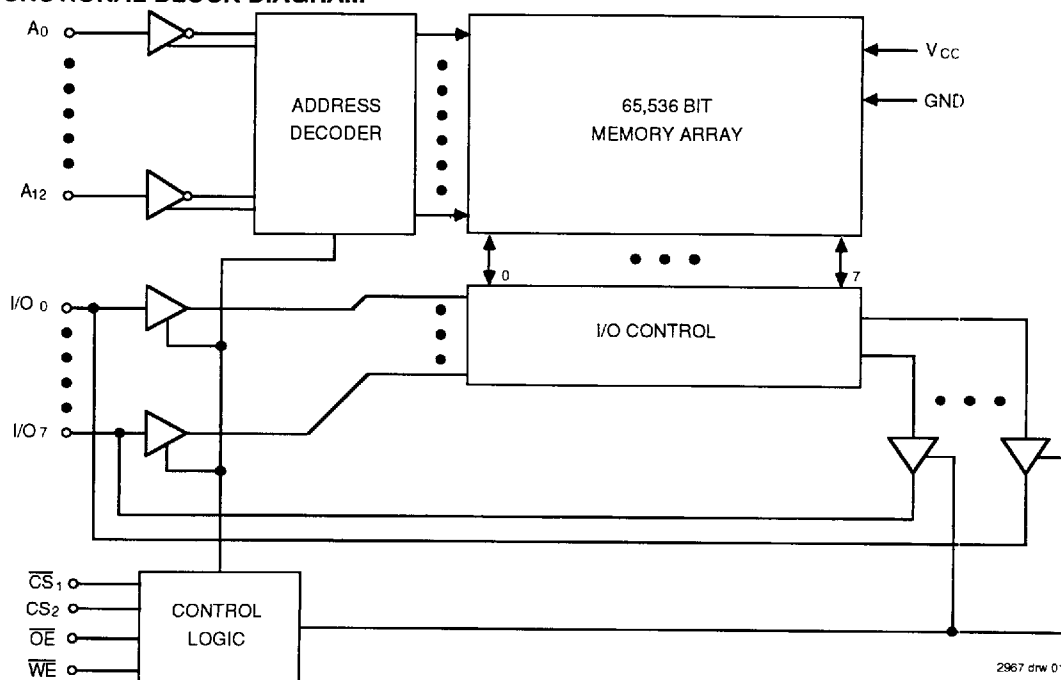
The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 15ns are available and the circuit offers a reduced power standby mode. When  $\overline{CS}_1$  goes high or  $\overline{CS}_2$  goes low, the circuit will automatically go to, and remain in, a low-power stand by mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ; 28-pin 330 mil SOIC; 28-pin 600 mil DIP; 32-pin PLCC and LCC; 28-pin LCC and 28-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

**FUNCTIONAL BLOCK DIAGRAM**

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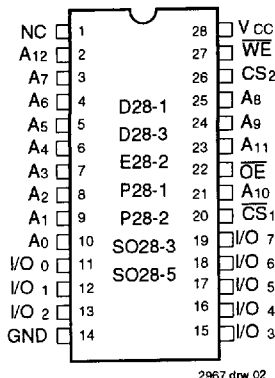
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**MILITARY AND COMMERCIAL TEMPERATURE RANGES****AUGUST 1992**

IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

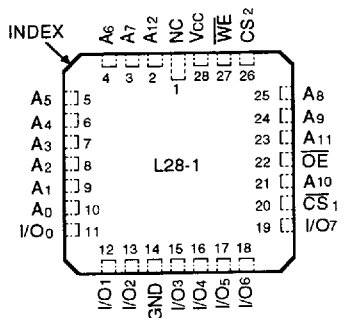
MILITARY AND COMMERCIAL TEMPERATURE RANGES

## PIN CONFIGURATIONS



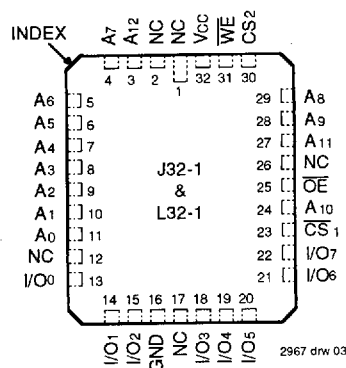
2967 drw 02

DIP/SOIC/SOJ/CERPACK  
TOP VIEW



2967 drw 04

28-PIN LCC  
TOP VIEW



2967 drw 03

32-PIN LCC/PLCC  
TOP VIEW

## PIN DESCRIPTIONS

| Name      | Description       |
|-----------|-------------------|
| A0-A12    | Address           |
| I/O0-I/O7 | Data Input/Output |
| CS1       | Chip Select       |
| CS2       | Chip Select       |
| WE        | Write Enable      |
| OE        | Output Enable     |
| GND       | Ground            |
| VCC       | Power             |

2967 tbl 01

## TRUTH TABLE (1,2,3)

| WE | CS1 | CS2        | OE | I/O     | Function                    |
|----|-----|------------|----|---------|-----------------------------|
| X  | H   | X          | X  | High-Z  | Deselected - Standby (ISB)  |
| X  | X   | L          | X  | High-Z  | Deselected - Standby (ISB)  |
| X  | VHC | VHC or VLC | X  | High-Z  | Deselected - Standby (ISB1) |
| X  | X   | VLC        | X  | High-Z  | Deselected - Standby (ISB1) |
| H  | L   | H          | H  | High-Z  | Output Disabled             |
| H  | L   | H          | L  | DataOUT | Read Data                   |
| L  | L   | H          | X  | DataIN  | Write Data                  |

NOTE:

2967 tbl 02

- CS2 will power-down CS1, but CS1 will not power-down CS2.
- H = VIH, L = VIL, X = don't care.
- VLC = 0.2V, VHC = VCC - 0.2V

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol               | Rating                               | Com'l.       | Mil.         | Unit |
|----------------------|--------------------------------------|--------------|--------------|------|
| VTERM <sup>(2)</sup> | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V    |
| TA                   | Operating Temperature                | 0 to +70     | -55 to +125  | °C   |
| TBIAS                | Temperature Under Bias               | -55 to +125  | -65 to +135  | °C   |
| TSTG                 | Storage Temperature                  | -55 to +125  | -65 to +150  | °C   |
| PT                   | Power Dissipation                    | 1.0          | 1.0          | W    |
| IOUT                 | DC Output Current                    | 50           | 50           | mA   |

NOTE:

2967 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed VCC + 0.5V.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade      | Temperature     | GND | VCC      |
|------------|-----------------|-----|----------|
| Military   | -55°C to +125°C | 0V  | 5V ± 10% |
| Commercial | 0°C to +70°C    | 0V  | 5V ± 10% |

2967 tbl 05

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter          | Min.                | Typ. | Max.      | Unit |
|--------|--------------------|---------------------|------|-----------|------|
| VCC    | Supply Voltage     | 4.5                 | 5.0  | 5.5       | V    |
| GND    | Supply Voltage     | 0                   | 0    | 0         | V    |
| VIH    | Input HIGH Voltage | 2.2                 | —    | VCC + 0.5 | V    |
| VIL    | Input LOW Voltage  | -0.5 <sup>(1)</sup> | —    | 0.8       | V    |

NOTE:

2967 tbl 06

- VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

IDT7164S, IDT7164L

CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

**CAPACITANCE** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

| Symbol | Parameter <sup>(1)</sup> | Conditions | Max. | Unit |
|--------|--------------------------|------------|------|------|
| CIN    | Input Capacitance        | VIN = 0V   | 8    | pF   |
| COU    | Output Capacitance       | VOUT = 0V  | 8    | pF   |

**NOTE:**

2967 tbi 04

1. This parameter is determined by device characterization, but is not production tested.

**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**(VCC = 5.0V  $\pm$  10%, VLC = 0.2V, VHC = VCC - 0.2V)

| Symbol | Parameter                                                                                                                                                           | Power | 7164S15<br>7164L15 |      | 7164S20<br>7164L20 |      | 7164S25<br>7164L25 |      | 7164S30<br>7164L30 |      | Unit |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------------|------|--------------------|------|--------------------|------|--------------------|------|------|
|        |                                                                                                                                                                     |       | Com'l.             | Mil. | Com'l.             | Mil. | Com'l.             | Mil. | Com'l.             | Mil. |      |
| ICC1   | Operating Power Supply Current, $\overline{CS}_1 = V_{IL}$ , $CS_2 = V_{IH}$ , Outputs Open, VCC = Max., $f = 0^{(3)}$                                              | S     | 110                | —    | 100                | 110  | 90                 | 110  | 90                 | 100  | mA   |
|        |                                                                                                                                                                     | L     | 100                | —    | 90                 | 100  | 80                 | 100  | 80                 | 90   |      |
| ICC2   | Dynamic Operating Current $\overline{CS}_1 = V_{IL}$ , $CS_2 = V_{IH}$ , Outputs Open, VCC = Max., $f = f_{MAX}^{(3)}$                                              | S     | 180                | —    | 170                | 180  | 170                | 180  | 160                | 170  | mA   |
|        |                                                                                                                                                                     | L     | 150                | —    | 150                | 160  | 150                | 160  | 140                | 150  |      |
| ISB    | Standby Power Supply Current (TTL Level), $\overline{CS}_1 \geq V_{IH}$ or $CS_2 \leq V_{IL}$ , VCC = Max., Outputs Open, $f = f_{MAX}^{(3)}$                       | S     | 20                 | —    | 20                 | 20   | 20                 | 20   | 20                 | 20   | mA   |
|        |                                                                                                                                                                     | L     | 3                  | —    | 3                  | 5    | 3                  | 5    | 3                  | 5    |      |
| ISB1   | Full Standby Power Supply Current (CMOS Level), $f = 0^{(3)}$ , VCC = Max.<br>1. $\overline{CS}_1 \geq V_{HC}$ and $CS_2 \geq V_{HC}$ , or<br>2. $CS_2 \leq V_{LC}$ | S     | 15                 | —    | 15                 | 20   | 15                 | 20   | 15                 | 20   | mA   |
|        |                                                                                                                                                                     | L     | 0.2                | —    | 0.2                | 1    | 0.2                | 1    | 0.2                | 1    |      |

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**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup> (Continued)**(VCC = 5.0V  $\pm$  10%, VLC = 0.2V, VHC = VCC - 0.2V)

| Symbol | Parameter                                                                                                                                                           | Power | 7164S35<br>7164L35 |      | 7164S45<br>7164L45 |      | 7164S55<br>7164L55 |      | 7164S70/85 <sup>(2)</sup><br>7164L70/85 <sup>(2)</sup> |      | Unit |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------------|------|--------------------|------|--------------------|------|--------------------------------------------------------|------|------|
|        |                                                                                                                                                                     |       | Com'l.             | Mil. | Com'l.             | Mil. | Com'l.             | Mil. | Com'l.                                                 | Mil. |      |
| ICC1   | Operating Power Supply Current, $\overline{CS}_1 = V_{IL}$ , $CS_2 = V_{IH}$ , Outputs Open, VCC = Max., $f = 0^{(3)}$                                              | S     | 90                 | 100  | —                  | 100  | —                  | 100  | —                                                      | 100  | mA   |
|        |                                                                                                                                                                     | L     | 80                 | 90   | —                  | 90   | —                  | 90   | —                                                      | 90   |      |
| ICC2   | Dynamic Operating Current $\overline{CS}_1 = V_{IL}$ , $CS_2 = V_{IH}$ , Outputs Open, VCC = Max., $f = f_{MAX}^{(3)}$                                              | S     | 150                | 160  | —                  | 160  | —                  | 160  | —                                                      | 160  | mA   |
|        |                                                                                                                                                                     | L     | 130                | 140  | —                  | 130  | —                  | 125  | —                                                      | 120  |      |
| ISB    | Standby Power Supply Current (TTL Level), $\overline{CS}_1 \geq V_{IH}$ or $CS_2 \leq V_{IL}$ , VCC = Max., Outputs Open, $f = f_{MAX}^{(3)}$                       | S     | 20                 | 20   | —                  | 20   | —                  | 20   | —                                                      | 20   | mA   |
|        |                                                                                                                                                                     | L     | 3                  | 5    | —                  | 5    | —                  | 5    | —                                                      | 5    |      |
| ISB1   | Full Standby Power Supply Current (CMOS Level), $f = 0^{(3)}$ , VCC = Max.<br>1. $\overline{CS}_1 \geq V_{HC}$ and $CS_2 \geq V_{HC}$ , or<br>2. $CS_2 \leq V_{LC}$ | S     | 15                 | 20   | —                  | 20   | —                  | 20   | —                                                      | 20   | mA   |
|        |                                                                                                                                                                     | L     | 0.2                | 1    | —                  | 1    | —                  | 1    | —                                                      | 1    |      |

**NOTES:**

2967 tbi 07

1. All values are maximum guaranteed values.

2. Also available: 100, 120, 150 and 200ns military devices.

3.  $f_{MAX} = 1/t_{sc}$  (all address inputs are cycling at  $f_{MAX}$ );  $f = 0$  means no address input lines are changing.

IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

## DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 5.0V ± 10%

| Symbol          | Parameter              | Test Condition                                                                                    | IDT7164S       |              | IDT7164L    |             | Unit |
|-----------------|------------------------|---------------------------------------------------------------------------------------------------|----------------|--------------|-------------|-------------|------|
|                 |                        |                                                                                                   | Min.           | Max.         | Min.        | Max.        |      |
| I <sub>LI</sub> | Input Leakage Current  | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = GND to V <sub>CC</sub>                               | MIL.<br>COM'L. | —<br>10<br>5 | —<br>5<br>2 | —<br>5<br>2 | μA   |
| I <sub>LO</sub> | Output Leakage Current | V <sub>CC</sub> = Max., $\overline{CS}_1 = V_{IH}$ ,<br>V <sub>OUT</sub> = GND to V <sub>CC</sub> | MIL.<br>COM'L. | —<br>10<br>5 | —<br>5<br>2 | —<br>5<br>2 | μA   |
| V <sub>OL</sub> | Output Low Voltage     | I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.                                                     |                | 0.4          | —           | 0.4         | V    |
|                 |                        | I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.                                                    |                | 0.5          | —           | 0.5         | V    |
| V <sub>OH</sub> | Output High Voltage    | I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.                                                    |                | 2.4          | —           | 2.4         | V    |

## DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

| Symbol                           | Parameter                            | Test Condition                                                         | Min.                           | Typ. <sup>(1)</sup><br>V <sub>CC</sub> @ |          | Max.<br>V <sub>CC</sub> @ |           | Unit |
|----------------------------------|--------------------------------------|------------------------------------------------------------------------|--------------------------------|------------------------------------------|----------|---------------------------|-----------|------|
|                                  |                                      |                                                                        |                                | 2.0V                                     | 3.0V     | 2.0V                      | 3.0V      |      |
| V <sub>DR</sub>                  | V <sub>CC</sub> for Data Retention   | —                                                                      | 2.0                            | —                                        | —        | —                         | —         | V    |
| I <sub>CCDR</sub>                | Data Retention Current               | MIL.<br>COM'L.                                                         | —<br>—                         | 10<br>10                                 | 15<br>15 | 200<br>60                 | 300<br>90 | μA   |
| t <sub>CDR</sub> <sup>(3)</sup>  | Chip Deselect to Data Retention Time | 1. $\overline{CS}_1 \geq V_{HC}$<br>$\overline{CS}_2 \geq V_{HC}$ , or | 0                              | —                                        | —        | —                         | —         | ns   |
| t <sub>R</sub> <sup>(3)</sup>    | Operation Recovery Time              | 2. $\overline{CS}_2 \leq V_{LC}$                                       | t <sub>RC</sub> <sup>(2)</sup> | —                                        | —        | —                         | —         | ns   |
| I <sub>LI</sub>   <sup>(3)</sup> | Input Leakage Current                |                                                                        | —                              | —                                        | —        | 2                         | 2         | μA   |

### NOTES:

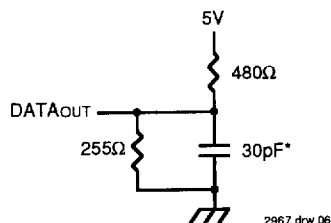
- TA = +25°C.
- t<sub>RC</sub> = Read Cycle Time.
- This parameter is guaranteed by device characterization, but is not production tested.

2967 tbl 10

## AC TEST CONDITIONS

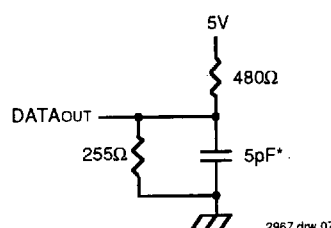
|                               |                     |
|-------------------------------|---------------------|
| Input Pulse Levels            | GND to 3.0V         |
| Input Rise/Fall Times         | 5ns                 |
| Input Timing Reference Levels | 1.5V                |
| Output Reference Levels       | 1.5V                |
| AC Test Load                  | See Figures 1 and 2 |

2967 tbl 08



2967 drw 06

Figure 1. AC Test Load



2967 drw 07

Figure 2. AC Test Load  
(for t<sub>CLZ1</sub>, t<sub>CLZ2</sub>, t<sub>OLZ</sub>, t<sub>CHZ1</sub>, t<sub>CHZ2</sub>, t<sub>OHZ</sub>, t<sub>OW</sub>, and t<sub>WHZ</sub>)

\*Includes scope and jig capacitances

**AC ELECTRICAL CHARACTERISTICS** (Vcc = 5.0V ± 10%, All Temperature Ranges)

| Symbol      | Parameter                                           | 7164S15 <sup>(1)</sup><br>7164L15 <sup>(1)</sup> |      | 7164S20<br>7164L20 |      | 7164S25<br>7164L25 |      | 7164S30<br>7164L30 |      | Unit |
|-------------|-----------------------------------------------------|--------------------------------------------------|------|--------------------|------|--------------------|------|--------------------|------|------|
|             |                                                     | Min.                                             | Max. | Min.               | Max. | Min.               | Max. | Min.               | Max. |      |
| Read Cycle  |                                                     |                                                  |      |                    |      |                    |      |                    |      |      |
| tRC         | Read Cycle Time                                     | 15                                               | —    | 20                 | —    | 25                 | —    | 30                 | —    | ns   |
| tAA         | Address Access Time                                 | —                                                | 15   | —                  | 19   | —                  | 25   | —                  | 29   | ns   |
| tACS1       | Chip Select-1 Access Time <sup>(3)</sup>            | —                                                | 15   | —                  | 20   | —                  | 25   | —                  | 30   | ns   |
| tACS2       | Chip Select-2 Access Time <sup>(3)</sup>            | —                                                | 20   | —                  | 25   | —                  | 30   | —                  | 35   | ns   |
| tCLZ1,2     | Chip Select-1, 2 to Output in Low-Z <sup>(4)</sup>  | 5                                                | —    | 5                  | —    | 5                  | —    | 5                  | —    | ns   |
| tOE         | Output Enable to Output Valid                       | —                                                | 7    | —                  | 8    | —                  | 12   | —                  | 15   | ns   |
| tOLZ        | Output Enable to Output in Low-Z <sup>(4)</sup>     | 3                                                | —    | 3                  | —    | 3                  | —    | 3                  | —    | ns   |
| tCHZ1,2     | Chip Select-1, 2 to Output in High-Z <sup>(4)</sup> | —                                                | 8    | —                  | 9    | —                  | 13   | —                  | 13   | ns   |
| tOHZ        | Output Disable to Output in High-Z <sup>(4)</sup>   | —                                                | 7    | —                  | 8    | —                  | 10   | —                  | 12   | ns   |
| tOH         | Output Hold from Address Change                     | 5                                                | —    | 5                  | —    | 5                  | —    | 5                  | —    | ns   |
| tPU         | Chip Select to Power Up Time <sup>(4)</sup>         | 0                                                | —    | 0                  | —    | 0                  | —    | 0                  | —    | ns   |
| tPD         | Chip Deselect to Power Down Time <sup>(4)</sup>     | —                                                | 15   | —                  | 20   | —                  | 25   | —                  | 30   | ns   |
| Write Cycle |                                                     |                                                  |      |                    |      |                    |      |                    |      |      |
| tWC         | Write Cycle Time                                    | 15                                               | —    | 20                 | —    | 25                 | —    | 30                 | —    | ns   |
| tCW1, 2     | Chip Select to End-of-Write                         | 14                                               | —    | 15                 | —    | 18                 | —    | 22                 | —    | ns   |
| tAW         | Address Valid to End-of-Write                       | 14                                               | —    | 15                 | —    | 18                 | —    | 22                 | —    | ns   |
| tAS         | Address Set-up Time                                 | 0                                                | —    | 0                  | —    | 0                  | —    | 0                  | —    | ns   |
| tWP         | Write Pulse Width                                   | 14                                               | —    | 15                 | —    | 21                 | —    | 23                 | —    | ns   |
| tWR1        | Write Recovery Time (CS <sub>1</sub> , WE)          | 0                                                | —    | 0                  | —    | 0                  | —    | 0                  | —    | ns   |
| tWR2        | Write Recovery Time (CS <sub>2</sub> )              | 5                                                | —    | 5                  | —    | 5                  | —    | 5                  | —    | ns   |
| tWHZ        | Write Enable to Output in High-Z <sup>(4)</sup>     | —                                                | 6    | —                  | 8    | —                  | 10   | —                  | 12   | ns   |
| tDW         | Data to Write Time Overlap                          | 8                                                | —    | 10                 | —    | 13                 | —    | 13                 | —    | ns   |
| tDH1        | Data Hold from Write Time (CS <sub>1</sub> , WE)    | 0                                                | —    | 0                  | —    | 0                  | —    | 0                  | —    | ns   |
| tDH2        | Data Hold from Write Time (CS <sub>2</sub> )        | 5                                                | —    | 5                  | —    | 5                  | —    | 5                  | —    | ns   |
| tOW         | Output Active from End-of-Write <sup>(4)</sup>      | 5                                                | —    | 5                  | —    | 5                  | —    | 5                  | —    | ns   |

**NOTES:**

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
- Both chip selects must be active for the device to be selected.
- This parameter is guaranteed by device characterization, but is not production tested.

2967 tbl 11

IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

# AC ELECTRICAL CHARACTERISTICS (Continued) (V<sub>CC</sub> = 5.0V ± 10%, All Temperature Ranges)

| Symbol      | Parameter                                           | 7164S35<br>7164L35 |      | 7164S45 <sup>(2)</sup><br>7164L45 <sup>(2)</sup> |      | 7164S55 <sup>(2)</sup><br>7164L55 <sup>(2)</sup> |      | 7164S70 <sup>(2)/85<sup>(2)</sup></sup><br>7164L70 <sup>(2)/85<sup>(2)</sup></sup> |       | Unit |
|-------------|-----------------------------------------------------|--------------------|------|--------------------------------------------------|------|--------------------------------------------------|------|------------------------------------------------------------------------------------|-------|------|
|             |                                                     | Min.               | Max. | Min.                                             | Max. | Min.                                             | Max. | Min.                                                                               | Max.  |      |
| Read Cycle  |                                                     |                    |      |                                                  |      |                                                  |      |                                                                                    |       |      |
| tRC         | Read Cycle Time                                     | 35                 | —    | 45                                               | —    | 55                                               | —    | 70/85                                                                              | —     | ns   |
| tAA         | Address Access Time                                 | —                  | 35   | —                                                | 45   | —                                                | 55   | —                                                                                  | 70/85 | ns   |
| tACS1       | Chip Select-1 Access Time <sup>(3)</sup>            | —                  | 35   | —                                                | 45   | —                                                | 55   | —                                                                                  | 70/85 | ns   |
| tACS2       | Chip Select-2 Access Time <sup>(3)</sup>            | —                  | 40   | —                                                | 45   | —                                                | 55   | —                                                                                  | 70/85 | ns   |
| tCLZ1,2     | Chip Select-1, 2 to Output in Low-Z <sup>(4)</sup>  | 5                  | —    | 5                                                | —    | 5                                                | —    | 5                                                                                  | —     | ns   |
| tOE         | Output Enable to Output Valid                       | —                  | 18   | —                                                | 25   | —                                                | 30   | —                                                                                  | 35/40 | ns   |
| tOLZ        | Output Enable to Output in Low-Z <sup>(4)</sup>     | 3                  | —    | 3                                                | —    | 3                                                | —    | 3                                                                                  | —     | ns   |
| tCHZ1,2     | Chip Select-1, 2 to Output in High-Z <sup>(4)</sup> | —                  | 15   | —                                                | 20   | —                                                | 25   | —                                                                                  | 30/35 | ns   |
| tOHZ        | Output Disable to Output in High-Z <sup>(4)</sup>   | —                  | 15   | —                                                | 20   | —                                                | 25   | —                                                                                  | 30/35 | ns   |
| tOH         | Output Hold from Address Change                     | 5                  | —    | 5                                                | —    | 5                                                | —    | 5                                                                                  | —     | ns   |
| tPU         | Chip Select to Power Up Time <sup>(4)</sup>         | 0                  | —    | 0                                                | —    | 0                                                | —    | 0                                                                                  | —     | ns   |
| tPD         | Chip Deselect to Power Down Time <sup>(4)</sup>     | —                  | 35   | —                                                | 45   | —                                                | 55   | —                                                                                  | 70/85 | ns   |
| Write Cycle |                                                     |                    |      |                                                  |      |                                                  |      |                                                                                    |       |      |
| tWC         | Write Cycle Time                                    | 35                 | —    | 45                                               | —    | 55                                               | —    | 70/85                                                                              | —     | ns   |
| tCW1, 2     | Chip Select to End-of-Write                         | 25                 | —    | 33                                               | —    | 50                                               | —    | 60/75                                                                              | —     | ns   |
| tAW         | Address Valid to End-of-Write                       | 25                 | —    | 33                                               | —    | 50                                               | —    | 60/75                                                                              | —     | ns   |
| tAS         | Address Set-up Time                                 | 0                  | —    | 0                                                | —    | 0                                                | —    | 0                                                                                  | —     | ns   |
| tWP         | Write Pulse Width                                   | 25                 | —    | 25                                               | —    | 50                                               | —    | 60/75                                                                              | —     | ns   |
| tWR1        | Write Recovery Time (CS1, WE)                       | 0                  | —    | 0                                                | —    | 0                                                | —    | 0                                                                                  | —     | ns   |
| tWR2        | Write Recovery Time (CS2)                           | 5                  | —    | 5                                                | —    | 5                                                | —    | 5                                                                                  | —     | ns   |
| tWHZ        | Write Enable to Output in High-Z <sup>(4)</sup>     | —                  | 14   | —                                                | 18   | —                                                | 25   | —                                                                                  | 30/35 | ns   |
| tDW         | Data to Write Time Overlap                          | 15                 | —    | 20                                               | —    | 25                                               | —    | 30/35                                                                              | —     | ns   |
| tDH1        | Data Hold from Write Time (CS1, WE)                 | 0                  | —    | 0                                                | —    | 0                                                | —    | 0                                                                                  | —     | ns   |
| tDH2        | Data Hold from Write Time (CS2)                     | 5                  | —    | 5                                                | —    | 5                                                | —    | 5                                                                                  | —     | ns   |
| tOW         | Output Active from End-of-Write <sup>(4)</sup>      | 5                  | —    | 5                                                | —    | 5                                                | —    | 5                                                                                  | —     | ns   |

## NOTES:

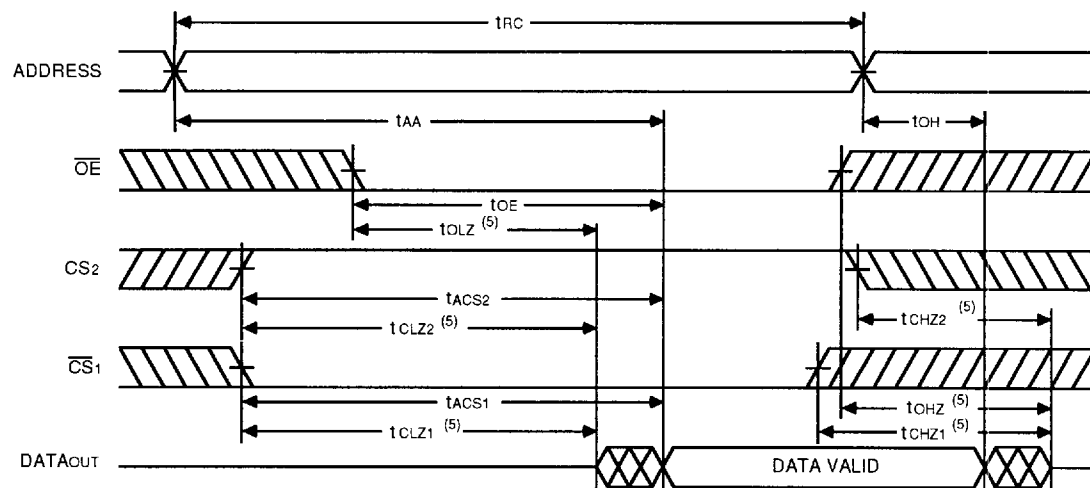
- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only. Also available: 100, 120, 150, and 200ns military devices.
- Both chip selects must be active for the device to be selected.
- This parameter is guaranteed by device characterization, but is not production tested.

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IDT7164S, IDT7164L  
CMOS STATIC RAM 64K (8K x 8-BIT)

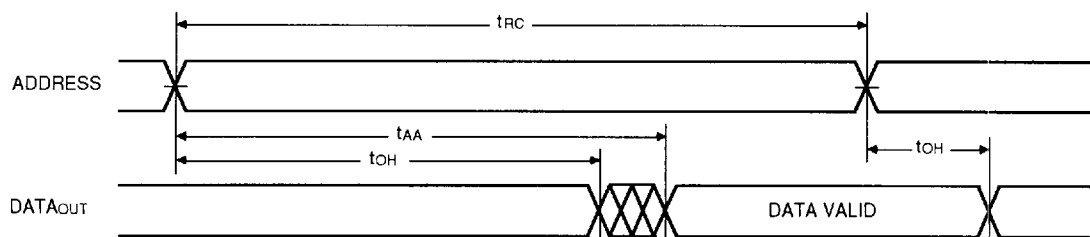
MILITARY AND COMMERCIAL TEMPERATURE RANGES

# TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>



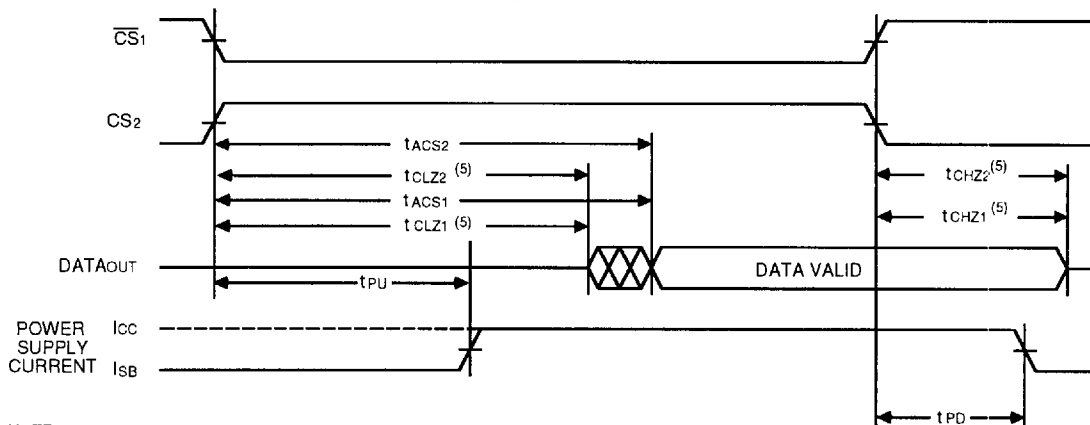
2967 drw 08

# TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>



2967 drw 09

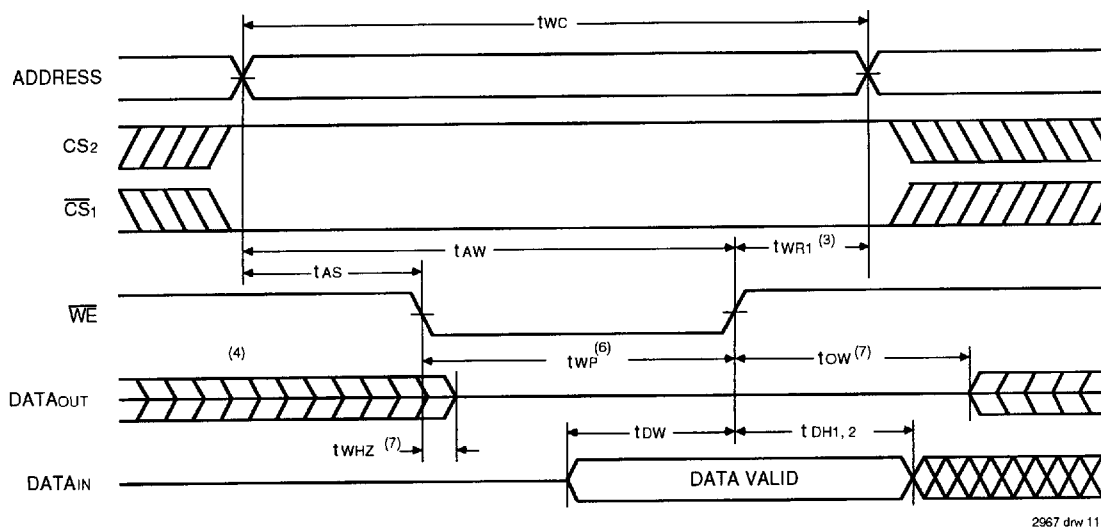
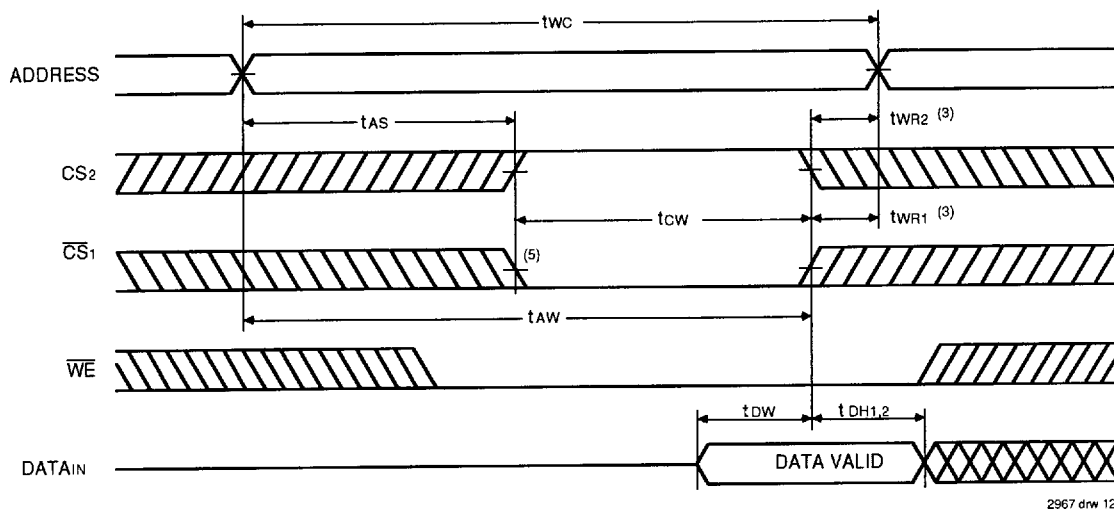
# TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1, 3, 4)</sup>



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## NOTES:

- WE is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS}_1 = V_{IL}$ ,  $CS_2 = V_{IH}$ .
- Address valid prior to or coincident with  $\overline{CS}_1$  transition LOW and  $CS_2$  transition HIGH.
- $\overline{OE}$  is LOW.
- Transition is measured  $\pm 200mV$  from steady state.

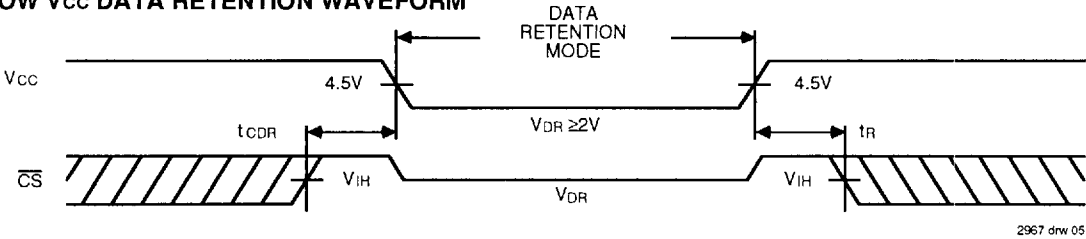
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1, 2, 6)</sup>TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1, 2)</sup>

## NOTES:

1.  $\overline{WE}$ ,  $\overline{CS1}$  or  $CS2$  must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW  $\overline{WE}$ , a LOW  $\overline{CS1}$  and a HIGH  $CS2$ .
3.  $tWR1, 2$  is measured from the earlier of  $\overline{CS1}$  or  $\overline{WE}$  going HIGH or  $CS2$  going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the  $\overline{CS1}$  LOW transition or  $CS2$  HIGH transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
6.  $\overline{OE}$  is continuously HIGH. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $tWP$  or  $(tWHZ + tOW)$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $tOW$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified  $tWP$ .
7. Transition is measured  $\pm 200mV$  from steady state.



LOW Vcc DATA RETENTION WAVEFORM



ORDERING INFORMATION

| IDT | 7164        | X     | XX    | XXX     | X                                |                                                                 |                      |
|-----|-------------|-------|-------|---------|----------------------------------|-----------------------------------------------------------------|----------------------|
|     | Device Type | Power | Speed | Package | Process/<br>Temperature<br>Range |                                                                 |                      |
|     |             |       |       |         | Blank                            | Commercial (0°C to +70°C)                                       |                      |
|     |             |       |       |         | B                                | Military (–55°C to +125°C)<br>Compliant to MIL-STD-883, Class B |                      |
|     |             |       |       |         | Y                                | 300 mil SOJ (SO28-5)                                            |                      |
|     |             |       |       |         | PE                               | 330 mil SOIC (SO28-3)                                           |                      |
|     |             |       |       |         | TD                               | 300 mil CERDIP (D28-3)                                          |                      |
|     |             |       |       |         | D                                | 600 mil CERDIP (D28-1)                                          |                      |
|     |             |       |       |         | P                                | 600 mil Plastic DIP (P28-1)                                     |                      |
|     |             |       |       |         | TP                               | 300 mil Plastic DIP (P28-2)                                     |                      |
|     |             |       |       |         | J                                | Plastic Leaded Chip Carrier (J32-1)                             |                      |
|     |             |       |       |         | L28                              | 28 Leadless Chip Carrier (L28-1)                                |                      |
|     |             |       |       |         | L32                              | 32 Leadless Chip Carrier (L32-1)                                |                      |
|     |             |       |       |         | XE                               | CERPACK F11 (E28-2)                                             |                      |
|     |             |       |       |         | 15                               | Commercial Only                                                 | Speed in Nanoseconds |
|     |             |       |       |         | 20                               |                                                                 |                      |
|     |             |       |       |         | 25                               |                                                                 |                      |
|     |             |       |       |         | 30                               |                                                                 |                      |
|     |             |       |       |         | 35                               |                                                                 |                      |
|     |             |       |       |         | 45                               | Military Only                                                   |                      |
|     |             |       |       |         | 55                               | Military Only                                                   |                      |
|     |             |       |       |         | 70                               | Military Only                                                   |                      |
|     |             |       |       |         | 85                               | Military Only                                                   |                      |
|     |             |       |       |         | S                                | Standard Power                                                  |                      |
|     |             |       |       |         | L                                | Low Power                                                       |                      |

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