AT&T
Microelectronics

CSP1084 Baseband Radio Interface
for IS-54 Dual-Mode Cellular Telephone Applications

Features

- Receive path
  - Decimation and postfiltering to 10 bits
  - Programmable gain amplifier with 0 dB to 18 dB gain in 2 dB steps
  - Simultaneous over sampling of in-phase and quadrature-phase channels using dual Σ-Δ converters
  - Root-raised-cosine ($\sqrt{RC}$) filter for digital mode
  - Two's complement output

- Transmit path
  - Dual 8-bit DACs for in-phase and quadrature-phase channels
  - π/4-shifted DQPSK modulation, root-raised-cosine filtering, and power ramping in digital mode
  - Differential peak-to-peak output of 2.5 V
  - Two's complement input

- Wideband data demodulator
  - Eight selectable bandwidths
  - Selectable 8- or 10-bit data storage register
  - 8-bit μP interface with four control pins

- RF control section outputs
  - 9-bit auxiliary D/A converter (AUX1)
  - Multiplexed 10-bit auxiliary D/A converter with two sample and holds

- Extensive use of differential design
  - High power supply rejection ratio
  - Low distortion
  - Low crosstalk

- Digital interface
  - 10-bit, parallel, bidirectional data bus
  - Digital I/O with CMOS compatibility
  - On-chip control and data registers

- Power
  - Single +5 V power supply, or +3.3 V digital/+5 V analog power supply
  - On-chip voltage references
  - Low average power dissipation
  - Independent powerdown modes for transmit, receive, and RF control sections

- Packaging
  - 64-pin and 100-pin low-profile, fine pitch TQFP, or 80-pin EIAJ/QFP

Description

The CSP1084 is a low-power, monolithic, CMOS data converter designed for use in North America dual-mode mobile telephone designs.

The device performs conversions (including modem/codec) and filtering functions for interfacing the IS-54 mobile cellular system IF/RF section to the digital signal processor or ASIC performing the modem function. The CSP1084 supports both analog and digital mode. When operating in the digital mode, the CSP1084 performs π/4-shifted DQPSK modulation and root-raised-cosine filtering on both the transmit and receive signals. Three auxiliary DAC outputs are provided for use as AGC, AFC, and RF power control signals. For transmission of data and control information, the CSP1084 uses a bidirectional parallel interface that is compatible with the external memory interface of the AT&T DSP1610/1616 digital signal processors.

In addition to providing these basic IF interface functions, the CSP1084 incorporates a wideband data demodulator (WBDD) for decoding the received FSK bits. In standby mode, use of this block in receiving forward control channel (FOCC) data results in significant power savings.

Continuing AT&T's tradition of providing signal processing with the highest performance in the industry, the CSP1084 draws less than 106 mW in analog mode, 76 mW in digital mode, and 16 mW in standby mode.

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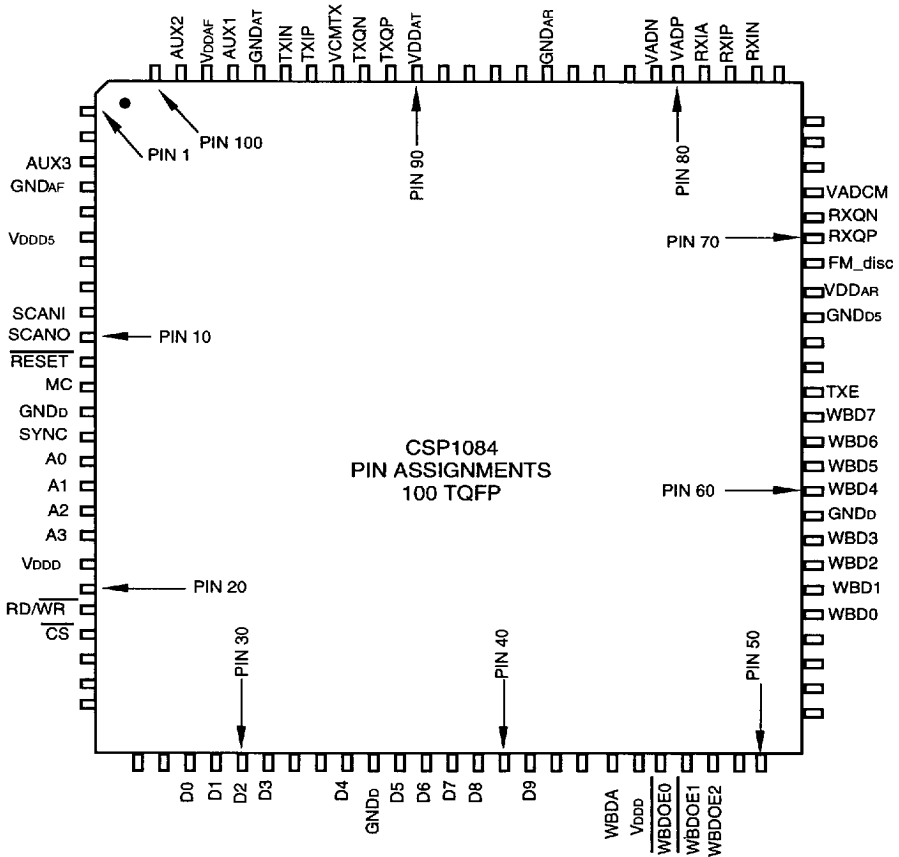**Note:** No pin label indicates no connection (reserved).

Figure 1. Pin Diagram, 100 TQFP

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Pin Information (continued)
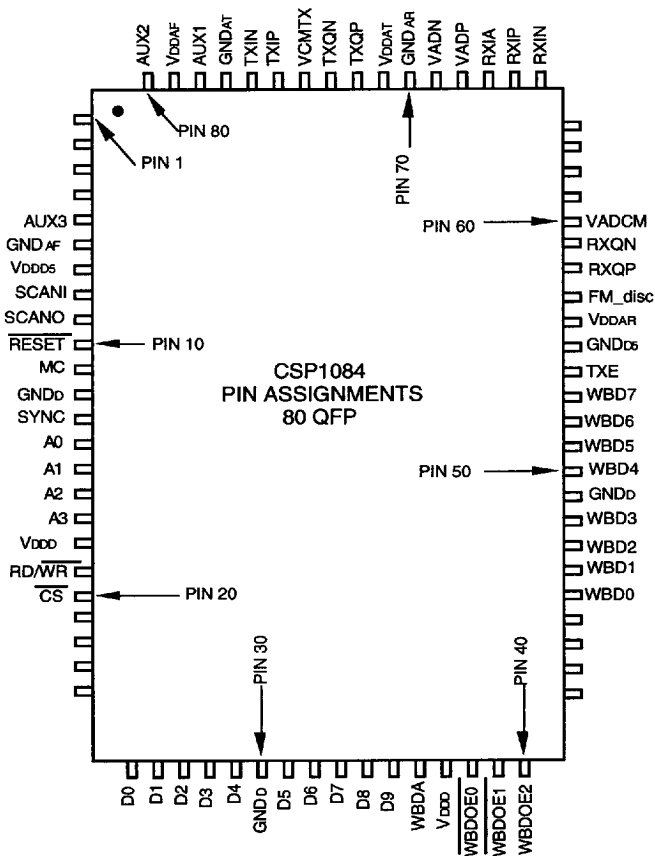
Note: No pin label indicates no connection (reserved).

Figure 2. Pin Diagram, 80 QFP
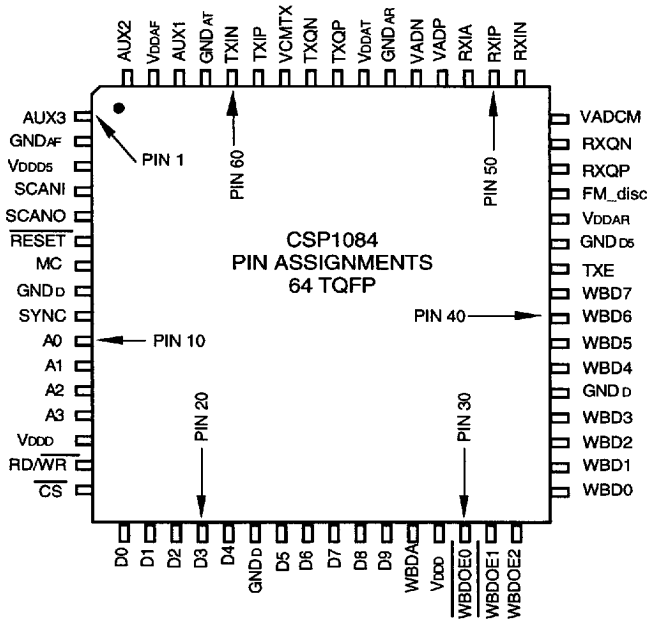
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Pin Information (continued)

Figure 3. Pin Diagram, 64 TQFP

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Pin Information (continued)

Table 1. Pin Descriptions

80-Pin EIAJ/ QFP	100-Pin TQFP	64-Pin TQFP	Symbol	Type*	Name/Description
1—4, 21—24, 41—44, 61—64	1, 2, 5, 7, 8, 20, 23—27, 32, 33, 40, 42, 43, 49—54, 65, 66, 73—76, 82—84, 86—89, 100	—	Reserved	NC	No connection. These pins are not tested; do not connect to these pins.
5	3	1	AUX3	O	Output of Auxiliary 10-Bit D/A converter.
6	4	2	GND$_{AF}$	GND	Analog Ground.
7	6	3	V$_{DDD5}$	PWR	5 V Digital/Analog Interface Supply.
8	9	4	SCANI	I†	Scan Path Test Input.
9	10	5	SCANO	O	Scan Path Test Output.
10	11	6	$\overline{RESET}$	I†	Device Reset Input.
11	12	7	MC	I	Master Clock.
12	13	8	GND$_D$	GND	Digital Ground.
13	14	9	SYNC	O	Data Bus Synchronization Signal.
14	15	10	A0	I	Address Bit 0.
15	16	11	A1	I	Address Bit 1.
16	17	12	A2	I	Address Bit 2.
17	18	13	A3	I	Address Bit 3.
18	19	14	V$_{DDD}$	PWR	5 V or 3.3 V Digital Supply.
19	21	15	RD / $\overline{WR}$	I	Read/Write Signal.
20	22	16	$\overline{CS}$	I†	Device Select Signal.
25	28	17	D0	I/O†	Data Bus—Bit 0.
26	29	18	D1	I/O†	Data Bus—Bit 1.
27	30	19	D2	I/O†	Data Bus—Bit 2.
28	31	20	D3	I/O†	Data Bus—Bit 3.
29	34	21	D4	I/O†	Data Bus—Bit 4.
30	35	22	GND$_D$	GND	Digital Ground.
31	36	23	D5	I/O†	Data Bus—Bit 5.
32	37	24	D6	I/O†	Data Bus—Bit 6.
33	38	25	D7	I/O†	Data Bus—Bit 7.
34	39	26	D8	I/O†	Data Bus—Bit 8.
35	41	27	D9	I/O†	Data Bus—Bit 9.
36	44	28	WBDA	O	Wideband Data Available Signal.
37	45	29	V$_{DDD}$	PWR	5 V or 3.3 V Digital Supply.
38	46	30	$\overline{WBDOE0}$	I†	Wideband Data Enable 0 (Active-Low).
39	47	31	$\overline{WBDOE1}$	I†	Wideband Data Enable 1 (Active-Low).
40	48	32	WBDOE2	I‡	Wideband Data Enable 2 (Active-High).
45	55	33	WBD0	O	Wideband Data—Bit 0.

* I = input, O = output, PWR = power, GND = ground, and NC = no connection.
† Indicates on-chip pull-up resistor, 100 kΩ minimum.
‡ Indicates on-chip pull-down resistor, 50 kΩ minimum.

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Pin Information (continued)

Table 1. Pin Descriptions (continued)

80-Pin EIAJ/ QFP	100-Pin TQFP	64-Pin TQFP	Symbol	Type*	Name/Description
46	56	34	WBD1	O	**Wideband Data—Bit 1.**
47	57	35	WBD2	O	**Wideband Data—Bit 2.**
48	58	36	WBD3	O	**Wideband Data—Bit 3.**
49	59	37	GNDD	GND	**Digital Ground.**
50	60	38	WBD4	O	**Wideband Data—Bit 4.**
51	61	39	WBD5	O	**Wideband Data—Bit 5.**
52	62	40	WBD6	O	**Wideband Data—Bit 6.**
53	63	41	WBD7	O	**Wideband Data—Bit 7.**
54	64	42	TXE	O	**Transmit Power Amplifier Enable.**
55	67	43	GNDD5	GND	**Digital/Analog Interface Ground.**
56	68	44	VDDAR	PWR	**+5 V Analog Supply.**
57	69	45	FM_disc	I	**FM Discriminated Receive Signal.**
58	70	46	RXQP	I	**Quadrature-Phase Receive Signal, Positive.**
59	71	47	RXQN	I	**Quadrature-Phase Receive Signal, Negative.**
60	72	48	VADCM		**2.4 V Analog Reference for A/D Converter.**
65	77	49	RXIN	I	**In-Phase Receive Signal, Negative.**
66	78	50	RXIP	I	**In-Phase Receive Signal, Positive.**
67	79	51	RXIA	I	**Single-Ended Auxiliary Input.**
68	80	52	VADP		**Positive Reference for A/D Converter.**
69	81	53	VADN		**Negative Reference for A/D Converter.**
70	85	54	GNDAR	GND	**Analog Ground.**
71	90	55	VDDAT	PWR	**+5 V Analog Supply.**
72	91	56	TXQP	O	**Quadrature-Phase Transmit Signal, Positive.**
73	92	57	TXQN	O	**Quadrature-Phase Transmit Signal, Negative.**
74	93	58	VCMTX	I	**External Reference for Transmitter.**
75	94	59	TXIP	O	**In-Phase Transmit Signal, Positive.**
76	95	60	TXIN	O	**In-Phase Transmit Signal, Negative.**
77	96	61	GNDAT	GND	**Analog Ground.**
78	97	62	AUX1	O	**Output of Auxiliary 9-Bit D/A Converter.**
79	98	63	VDDAF	PWR	**+5 V Analog Supply.**
80	99	64	AUX2	O	**Output of Auxiliary 10-Bit D/A Converter.**

* I = input, O = output, PWR = power, GND = ground, and NC = no connection.
† Indicates on-chip pull-up resistor, 100 kΩ minimum.
‡ Indicates on-chip pull-down resistor, 50 kΩ minimum.

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Block Diagram

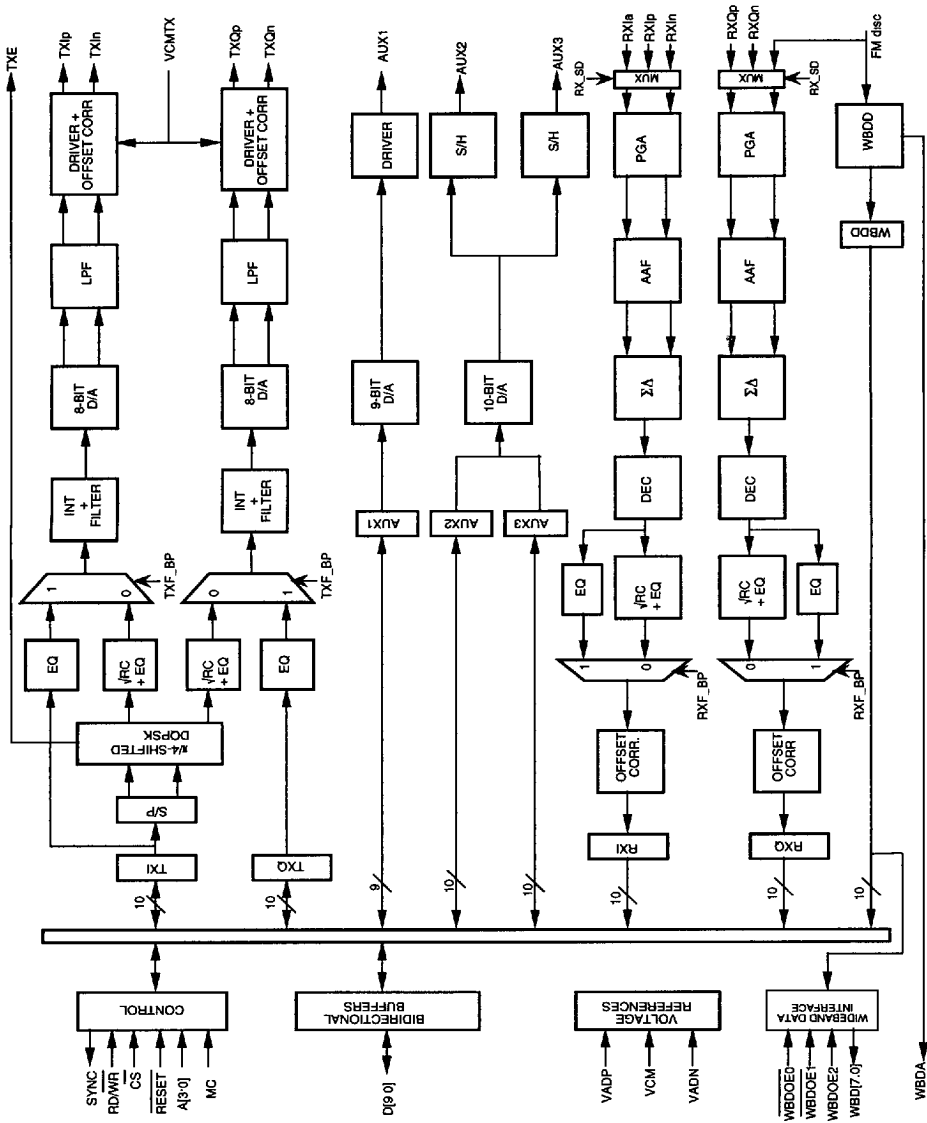**Figure 4. Block Diagram**

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Functional Overview

The block diagram of the CSP1084 is shown in Figure 3. The device can be divided into four major sections: transmit, RF control, receive, and digital interface. All control is via three on-chip registers (see Register Descriptions) that are accessible through the digital interface. The voltage reference circuits needed to operate each section are included in the device.

D/A and A/D Converter Rates

The sample rates of the various converters are shown in Table 2 as a function of the input master clock (MC) frequency. The device is designed to operate at a MC rate of 2.3328 MHz in the digital mode and at 2.5920 MHz in the analog mode.

Table 2. A/D and D/A Conversion Rates

Channel	Bits/Sample	Rate (samples per second)		
		Relative to MC	Digital Mode MC = 2.3328 MHz	Analog Mode MC = 2.5920 MHz
TXI, TXQ	8	MC/3	777.6 ks/s	864.0 ks/s
AUX1	9	MC/48	48.6 ks/s	54.0 ks/s
AUX2/AUX3	10	MC/48	48.6 ks/s	54.0 ks/s
RXI, RXQ	10	MC/48	48.6 ks/s	54.0 ks/s

Transmit

The transmit channel consists of a $\pi/4$-shifted DQPSK modulator and two identical paths, TXI and TXQ, for simultaneous generation of the in-phase and quadrature-phase signals. Power ramping for digital mode is also supported. The digital portion of each path is comprised of an input data register, an FIR filter (EQ), a linear interpolator (INT), and a low-pass filter. In the digital mode of operation, the FIR filter uses coefficients corresponding to a $\sqrt{RC}$ low-pass filter with pre-equalization to compensate for the passband roll-off of the interpolator and the low-pass filter. In the analog mode of operation, the modulator is bypassed, and the FIR filter uses coefficients for pre-equalization only.

The analog section of each transmit path consists of an 8-bit D/A converter, a reconstruction filter (LPF), and a line driver. The conversion rate for these converters is shown in Table 2. The TXI and TXQ outputs are designed to be dc-coupled to the external circuits and will drive a resistive load as low as 10 kΩ in parallel with a capacitive load as high as 50 pF. An external voltage may be applied to the VCMTX pin to set the common mode voltage of the TXI and TXQ outputs. When the VCMTX pin is left unconnected, the TXI and TXQ outputs will have an internally defined common-mode level of approximately 2.4 V. A dc offset correction circuit is provided for each path to minimize the offset when operating in the digital mode.

RF Control

AGC, AFC, and RF power control signals are provided by two auxiliary D/A converters. The AUX1 9-bit D/A converter operates synchronously with the TXI and TXQ converters but at one-sixteenth the rate (see Table 2). A multiplexed 10-bit D/A converter is shared between auxiliary outputs AUX2 and AUX3. Each auxiliary D/A channel has an input data register, and each converter's sample and hold output is designed to drive a maximum dc-coupled load of 50 kΩ in parallel with 50 pF (AUX1) or 20 pF (AUX2 and AUX3).

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Functional Overview (continued)

Receive

The receive channel consists of two identical paths, RXI and RXQ, for simultaneous processing of the in-phase and quadrature-phase signals. The analog processing is performed by a programmable gain amplifier (PGA), an anti-aliasing filter (AAF), and a sigma-delta (Σ-Δ) modulator. The RXQ path also has a multiplexer on its front-end to switch between the digital mode quadrature-phase signal (RXQP and RXQN) and the analog mode FM discriminated signal (FM_disc). The RXI path has a similar multiplexer, and its single-ended input (RXIA) can be used to sense parameters such as RSSI, temperature, or battery voltage.

The digital processing in the RXI and RXQ paths is performed by a decimation filter (DEC), an FIR filter (EQ), and a dc offset correction circuit. In the digital mode of operation, the FIR filter uses coefficients corresponding to a $\sqrt{RC}$ low-pass filter with a postequalizer to compensate for the passband roll-off of the decimation filter. In the analog mode, the FIR filter uses coefficients for equalization only.

The receive section contains a wideband data demodulator (WBDD) for recovering the forward analog correction channel (FOCC) and forward voice channel (FVC) data. It consists of an adjustable bandwidth digital phase-locked loop for timing recovery, a Manchester data decoder, and a 10-bit storage register. This data is normally available through the 10-bit parallel interface; however, this data can be provided through an 8-bit interface to a microprocessor for FOCC processing. This allows the DSP to be powered down in the standby mode for significant power savings.

Digital Interface

The on-chip data and control registers are accessed through an asynchronous interface consisting of a 10-bit data bus D[9:0], four address pins A[3:0], a read/write signal RD/$\overline{WR}$, a chip select signal $\overline{CS}$, a data bus synchronization signal SYNC, and a wideband data available signal, WBDA. See the Digital Interface Description section for details.

An 8-bit microprocessor interface for the WBDD circuits consists of an 8-bit data bus WBD[7:0], three chip select pins WBDOE2, $\overline{WBDOE1}$, $\overline{WBDOE0}$, and a wideband data available signal, WBDA. See the Wideband Data Demodulator Operation section for more information.

Other digital pins include the master clock input MC and the reset input $\overline{RESET}$. See the description on control register B for details about the RESET operation.

Register Descriptions

Table 3 lists the twelve on-chip registers that are accessible via the 10-bit bidirectional bus. Table 4 contains a bit map of the registers and indicates their value after a hardware or software reset. There are three control registers (CONTROLA, CONTROLB, and PGA/WCTRL), five data input registers (TXI, TXQ, AUX1, AUX2, and AUX3), and three data output registers (RXI, RXQ, and WBDD). There is also a test register (address 15) which is reserved for manufacture test and should always be set to 0 for normal operation. All registers may be both written and read except for RXI, RXQ, and WBDD, which are read-only. The register address is given by inputs A3, A2, A1, and A0 where A3 is the most significant bit (MSB). Addresses 11 through 14 are not used.

Note: Reserved or unused register bits should be written with zeros. Also, data written to the register does not take affect until a SYNC pulse occurs.

The registers CONTROLA (address 0), CONTROLB (address 8), and PGA/WCTRL (address 9) determine the operating state of the CSP1084. CONTROLA provides on/off functional control for the transmit path, the RF control section, and the receive path. CONTROLB supports control options for the dc offset correction, receive channel input multiplexers, the $\sqrt{RC}$ filters, and a software reset. PGA/WCTRL holds the setting for the programmable gain amplifiers and control bits for the wideband data demodulator. See the Control Register Descriptions section for details.

Register Descriptions (continued)

The transmit channel has two data input registers: TXI (address 1) and TXQ (address 2). In digital mode, bit 0 of TXI holds a single bit of the unmodulated transmit data, and TXQ is unused. In analog mode, these registers hold the 10-bit two's complement binary input data for the transmit paths.

The RF control section has three data registers: AUX1, AUX2, and AUX3 (addresses 3, 4, and 5, respectively). These registers hold the two's complement binary word inputs for the D/A converters.

The receive section has three data output registers: RXI, RXQ, and WBDD (addresses 6, 7, and 10, respectively). The RXI and RXQ registers hold the two's complement binary outputs of the A/D converters, and the WBDD register holds either 8 or 10 bits of decoded wideband data.

Several registers contain less than 10 bits, and this is indicated in the register bit map table (Table 4) with an X. These bits of the data bus should be zero during a write to these registers and should be treated as unknowns during a read.

Table 3. Register Address Table

Address	A(3:0)	Name	Description
0	0000	CONTROLA	Control register A
1	0001	TXI	Unmodulated transmit data/Transmit in-phase signal
2	0010	TXQ	Transmit quadrature-phase signal
3	0011	AUX1	9-bit D/A input for AUX1
4	0100	AUX2	10-bit D/A input for AUX2
5	0101	AUX3	10-bit D/A input for AUX3
6	0110	RXI	Received in-phase signal A/D result
7	0111	RXQ	Received quadrature-phase signal A/D result
8	1000	CONTROLB	Control register B
9	1001	PGA/WCTRL	Programmable gain amplifier setting; WBDD control
10	1010	WBDD	8 bits/10 bits of Manchester decoded data
11—14	—	—	Reserved
15	1111	TESTREG	Reserved for manufacture tests

Table 4. Register Bit Map

NOTE: Bits marked reserved should be written to 0 and treated as unknowns when read.

Name	Reg #	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
CONTROLA	0	RXQ_GO	RXQ_ON	RXI_GO	RXI_ON	AUX3_ON	AUX2_ON	AUX1_ON	TX_GO	TX_ON	SMODE
Reset Value		0	0	0	0	0	0	0	0	0	0
TXI	1	Unmodulated Transmit Data (Bit 0 when TXF_BP = 0); TXI Transmit Data (TXF_BP = 1)									
Reset Value		0	0	0	0	0	0	0	0	0	0
TXQ	2	Unused (TXF_BP = 0); TXQ Transmit Data (TXF_BP = 1)									
Reset Value		0	0	0	0	0	0	0	0	0	0
AUX1	3	Reserved	Auxiliary #1 input								
Reset Value		X	1	0	0	0	0	0	0	0	0
AUX2	4	Auxiliary #2 input									
Reset Value		0	0	0	0	0	0	0	0	0	0
AUX3	5	Auxiliary #3 input									
Reset Value		0	0	0	0	0	0	0	0	0	0
RXI	6	Received in-phase signal A/D result									
Reset Value		0	0	0	0	0	0	0	0	0	0
RXQ	7	Received quadrature-phase signal A/D result									
Reset Value		0	0	0	0	0	0	0	0	0	0
CONTROLB	8	Reserved	W_LOCK	Reserved	RXC1	RXC0	RXF_BP	RX_SD	TX_OC	TXF_BP	RESET
Reset Value		X	0	X	0	0	0	0	0	0	0
PGA/WCTRL	9	Reserved	W_SEL8	W_BW2	W_BW1	W_BW0	W_ON	PGA3	PGA2	PGA1	PGA0
Reset Value		X	0	0	0	0	0	0	0	0	0
WBDD	10	8 bits/10 bits of Manchester decoded data									
Reset Value		0	0	0	0	0	0	0	0	0	0
TESTREG	15	Reserved for manufacture test									
Reset Value		0	0	0	0	0	0	0	0	0	0

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Control Register Descriptions

The control registers (CONTROLA, CONTROLB, and PGA/WCTRL) determine the operating state of the CSP1084 device. Each bit of CONTROLA is listed in Table 5 and described in detail following Table 5. The bits of CONTROLB are listed in Table 6 and described in detail following Table 6. The control of the receive channel dc offset correction block is summarized in Table 7. Tables 8, 9, and 10 detail the function of the bits in the PGA/WCTRL register. An example of the control registers' bit status during various operational modes is given in Table 11. See the Digital Interface Description section for information about accessing these registers.

CONTROLA Register (Address 0)

Table 5. CONTROLA Register A (Address 0)

Bit	Name	Function
0	SMODE	When set = 1, indicates standby mode.
1	TX_ON	When set = 1, transmit (TXI and TXQ) converter circuits powered on.
2	TX_GO	When set = 1, start (stop when = 0) TXI and TXQ D/A conversions.
3	AUX1_ON	When set = 1, 9-bit D/A powered on and performing data conversion.
4	AUX2_ON	When set = 1, 10-bit D/A powered on and performing data conversion for AUX2.
5	AUX3_ON	When set = 1, 10-bit D/A powered on and performing data conversion for AUX3.
6	RXI_ON	When set = 1, RXI A/D circuits powered on.
7	RXI_GO	When set = 1, start (stop when = 0) RXI A/D conversions.
8	RXQ_ON	When set = 1, RXQ A/D circuits powered on.
9	RXQ_GO	When set = 1, start (stop when = 0) RXQ A/D conversions.

Bit 0 SMODE

This bit should be set to 1 to enter the standby mode. When SMODE = 1, the voltage references, the transmit channel, the RF control D/A converters, and the receive channel are powered down. This is accomplished without affecting the remaining bits of the CONTROLA register . The state of the wideband data demodulator is independent of SMODE and determined by the bits in the PGA/WCTRL register. SMODE should be set to 0 for normal operation and when initializing the dc offset correction circuit.

When entering the standby mode, the following procedure is recommended:

1. Set the SMODE bit in the CONTROLA register to 1. This causes the TX/RX channels, AUX DACs, and voltage references to be powered down. Note that the SMODE bit supersedes the other bits in the CONTROLA register. Hence, as long as SMODE = 1, the status of the other bits (like TX_ON, TX_GO, etc.) will have no effect.

2. Set TX_BP = 0. When TX_BP = 1, the device operates in the analog mode. In analog mode, TXE stays high to enable the power amp. For standby mode, setting TX_BP = 0 disables the power amp.

3. Do a dummy write of 0xFFFF to an unused system address to charge the bus high. This prevents high current in the CSP1084 input buffers caused by a slow ramp via the pull-up resistors.

Bit 1 TX_ON (SMODE = 0)

When TX_ON = 1, all of the analog circuits associated with the TXI and TXQ D/A converters are powered on. When TX_ON = 0, these circuits are in powerdown mode, and no reference dc level is maintained on the transmit channel outputs.

Bit 2 TX_GO (SMODE = 0)

When TX_GO = 1 (and TX_ON = 1), the transmit channel (TXI, TXQ) is operational. When TX_GO = 0, data conversions are stopped. See Transmit Channel (TXI, TXQ) Operation for details.

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Control Register Descriptions (continued)

CONTROLA Register (Address 0) (continued)

Bit 3 AUX1_ON (SMODE = 0)
When AUX1_ON = 1, all the circuits associated with the 9-bit D/A converter are powered on and data conversions are performed. When AUX1_ON = 0, these circuits are in powerdown mode and output AUX1 is switched to GNDAF. See AUX1 9-bit D/A Converter Operation for further details.

Bits 4 and 5 AUX2_ON and AUX3_ON (SMODE = 0)
When AUX2_ON = 1 or AUX3_ON = 1, all the circuits associated with the 10-bit D/A converter are powered on and data conversions are performed. When AUX2_ON = 0 and AUX3_ON = 0, these circuits are in powerdown mode. AUX2 is switched to VCMTX (2.375 V nominal), and AUX3 is switched to GNDAF. See the description under AUX2/AUX3 10-Bit D/A Converter Operation for further details.

Bits 6 and 8 RXI_ON and RXQ_ON (SMODE = 0)
When RXI_ON = 1, all of the analog circuits associated with the RXI A/D converter are powered on. When RXI_ON = 0, these circuits are in powerdown mode and a reference dc level is maintained on the RXI input. RXI_ON should be set to 1 at least one SYNC cycle before RXI_GO = 1. RXQ_ON controls the analog circuits of the RXQ channel in the same manner.

Bits 7 and 9 RXI_GO and RXQ_GO (SMODE = 0)
When RXI_GO = 1 (and RXI_ON = 1), the RXI channel is operational. When RXI_GO = 0, no data conversions are performed. RXQ_GO controls the RXQ channel in the same manner. See Receive Channel (RXI, RXQ) Operation for details.

CONTROLB Register (Address 8)

Table 6. CONTROLB Register (Address 8)

Bit	Name	Function
0	RESET	When set = 1, reset registers to default values.
1	TXF_BP	When set = 1, the transmit channel modulator and filters are bypassed (for analog mode).
2	TX_OC	When set = 1, transmit channel dc offset correction is enabled (use in digital mode only).
3	RX_SD	Receive channel input multiplexer control.
4	RXF_BP	When set = 1, the receive channel filters are bypassed (for analog mode).
5	RXC0	Receive A/D dc offset correction control bit 0.
6	RXC1	Receive A/D dc offset correction control bit 1.
7	—	Reserved, write to 0.
8	W_LOCK	When set to 1, the WBDD stays locked to the FOCC/FVC signal.
9	—	Reserved, write to 0.

Bit 0 RESET
Setting RESET = 1 forces the device into the reset state, as specified in the register bit map (Table 4). This bit may be set to 1 by writing the control register or by a hardware reset accomplished by holding the $\overline{\text{RESET}}$ pin low for at least six MC cycles. The master clock input (MC) must be active to reset the device. The RESET bit will remain set to 1 for the duration of the reset sequence. RESET will be automatically cleared (set to 0) once the reset sequence is complete. Therefore, the RESET bit in the control register may be read to determine if the device has completed its reset sequence. The reset sequence lasts for 96 MC cycles following the first SYNC rising edge after setting RESET = 1.

Bit 1 TXF_BP
TXF_BP controls the data path of the transmit channel. For analog mode, set TXF_BP = 1 to bypass the $\pi/4$--shifted DQPSK modulator and the $\sqrt{\text{RC}}$ filters so that the equalizer receives data directly from the TXI and TXQ registers. TXF_BP should be set to 0 during the digital mode of operation.

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Control Register Descriptions (continued)

CONTROLB Register (Address 8) (continued)

Bit 2 TX_OC
For digital mode, setting TX_OC = 1 enables the transmit channel dc offset correction circuits. The offset correction is performed at the beginning of each transmit slot. Set TX_OC = 0 for analog mode.

BIT 3 RX_SD
For analog mode (or to use RXIA), set RX_SD = 1 to select the single-ended inputs RXIA and FM_disc as the active inputs to the receive channels. For digital mode, set RX_SD = 0 to select the differential inputs RXIP, RXIN, RXQP, and RXQN as the active inputs to the receive channels.

Bit 4 RXF_BP
For analog mode, set RXF_BP = 1 to bypass the $\sqrt{RC}$ receive channel filters so only equalization is performed. RXF_BP should be set to 0 during the digital mode of operation.

Bits 5 and 6 RXC0 and RXC1
The values of RXC0 and RXC1 determine the operating mode of the digital dc offset correction circuit (see Table 7). In order for the dc offset correction circuit to work properly, it must be initialized before use in the normal operating mode, and the references must be powered on (SMODE = 0) and settled. In initialization mode (RXC0 = 1 and RXC1 = 0), the circuit automatically measures the dc offset for each channel and each PGA setting and stores these values for use in normal operation. Initialization mode is activated by writing RXC[1:0] = 01, RXI_ON = 1, and RXQ_ON = 1 in the same SYNC interval and by writing RXI_GO = 1 and RXP_GO = 1 in the next SYNC interval. Upon completion of the initialization process, RXI_GO and RXQ_GO will be automatically cleared to 0. The values of RXC0 and RXC1 should be modified only after initialization is complete (specified as a maximum of 14,000 MC cycles).

In normal operation (RXC0 = 0 and RXC1 = 0), the dc offset value determined during initialization is automatically subtracted from each A/D conversion result, thereby canceling the dc offset.

In the manual mode (RXC0 = 0 and RXC1 = 1), the PGA inputs are internally disconnected from the receive channel input pins so that the A/D converter result will be a measurement of the dc offset.

In the off mode (RXC0 = 1 and RXC1 = 1), the PGA inputs are connected normally to the receive channel inputs and no dc offset cancellation is performed on the A/D conversion result.

When operating in digital mode (RX_SD = 0), the dc offset correction should be enabled. When operating in analog mode (RX_SD = 1), it is recommended that the offset correction block be placed in off mode. If the dc offset correction is used in both modes, it must be reinitialized each time the mode is switched.

During all of these three modes (normal, manual, and off), the processed data is available after an initial delay. See the receive A/D synchronization diagram (Figure 12) for further details.

The values of RXC0 and RXC1 should only be modified when RXI_GO = 0 and RXQ_GO = 0 in order to ensure proper functioning of the dc offset correction circuit.

Bit 8 W_LOCK
When W_LOCK = 1, the WBDD is locked with respect to the incoming FOCC signal. When W_LOCK = 0 (the default state), the WBDD is not locked with respect to the incoming signal. For more detail, see the Wideband Data Demodulation Operation section.

Table 7. dc Offset Correction Control Bits

Register 8, Bit 6 RXC1	Register 8, Bit 5 RXC0	Mode	Function
0	0	Normal	Automatic dc offset correction enabled
0	1	Initialization	Automatic dc offset correction initialization
1	0	Manual	Setup PGA for manual dc offset measurement
1	1	Off	dc offset correction disabled

Control Register Descriptions (continued)

PGA/WCTRL Register (Address 9)

Table 8. PGA/WCTRL Register (Address 9)

Bit	Name	Function
0	PGA0	Programmable gain amplifier control bit 0.
1	PGA1	Programmable gain amplifier control bit 1.
2	PGA2	Programmable gain amplifier control bit 2.
3	PGA3	Programmable gain amplifier control bit 3.
4	W_ON	When set = 1, wideband data demodulator is active.
5	W_BW0	Wideband data demodulator bandwidth control bit 0.
6	W_BW1	Wideband data demodulator bandwidth control bit 1.
7	W_BW2	Wideband data demodulator bandwidth control bit 2.
8	W_SEL8	Selects an 8-bit or 10-bit output word from WBDD.
9	—	Reserved, write to 0.

Bit 0—3 PGA0, PGA1, PGA2, and PGA3
The values of PGA0, PGA1, PGA2, and PGA3 determine the gain of the PGA in the receive channel as shown in Table 9.

Bit 4 W_ON
When W_ON = 1, the wideband data demodulator is active. It is deactivated by setting W_ON = 0.

Bits 5—7 W_BW0, W_BW1, and W_BW2
The values of W_BW0, W_BW1, and W_BW2 determine the bandwidth of the DPLL loop filter (see Table 10). For tracking the continuous FOCC data stream, the setting W_BW[2:0] = 111 is recommended. To receive the blank and burst control messages (FVC) while in analog mode, the setting W_BW[2:0] = 100 is recommended.

Bit 8 W_SEL8
When W_SEL8 = 1, the WBDD register is configured to output 8-bit words via the 8-bit microprocessor interface. When W_SEL8 = 0, the WBDD register is configured to output 10-bit words via the 10-bit DSP interface, and the 8-bit microprocessor interface is 3-stated.

Table 9. PGA/WCTRL Register (Address 9): PGA Settings

PGA3	PGA2	PGA1	PGA0	Gain
Bit 3	Bit 2	Bit 1	Bit 0	(dB)
0	0	0	0	0
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
0	1	0	1	10
0	1	1	0	12
0	1	1	1	14
1	0	0	0	16
1	0	0	1	18
1	0	1	0	18
1	0	1	1	18
1	1	0	0	18
1	1	0	1	18
1	1	1	0	18
1	1	1	1	18

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Control Register Descriptions (continued)

PGA/WCTRL Register (Address 9)

Table 10. PGA/WCTRL Register (Address 9): WBDD Bandwidth Control

W_BW2 Bit 7	W_BW1 Bit 6	W_BW0 Bit 5	−3 dB Bandwidth (Hz)	Bandwidth Function
1	1	1	12.4	Recommended for receiving FOCC data.
1	1	0	25.1	
1	0	1	50.5	
1	0	0	102.8	Recommended for receiving FVC data.
0	1	1	212.8	
0	1	0	461.1	
0	0	1	1150.3	
0	0	0	10000.0	Maximum.

Table 11. Control Registers' Bit Status vs. Operating Mode

MODE	Block/Channel WBDD	TXI, TXQ	AUX1	AUX2, AUX3	RXI	RXQ	RXI, RXQ
STANDBY SMODE = 1	W_ON = 1 W_BW[2:0] = 111	TX_ON = X TX_GO = X TXF_BP = 0 TX_OC = X	AUX1_ON = X	AUX2_ON = X AUX3_ON = X	RXI_ON = X RXI_GO = X	RXQ_ON = X RXQ_GO = X	RX_SD = X RXF_BP = X RXC[1:0] = XX
ANALOG SMODE = 0	W_ON = 1 W_BW[2:0] = 100	TX_ON = X TX_GO = 1 TXF_BP = 1 TX_OC = 0	AUX1_ON = 0	AUX2_ON = 0 AUX3_ON = 0	RXI_ON = 0 RXI_GO = 0	RXQ_ON = 1 RXQ_GO = 1	RX_SD = 1 RXF_BP = 1 RXC[1:0] = 11
DIGITAL ACQUISITION SMODE = 0	W_ON = 0 W_BW[2:0] = XXX	TX_ON = 0 TX_GO = 0 TXF_BP = X TX_OC = X	AUX1_ON = 0	AUX2_ON = 1 AUX3_ON = 1	RXI_ON = 1 RXI_GO = 1	RXQ_ON = 1 RXQ_GO = 1	RX_SD = 0 RXF_BP = 0 RXC[1:0] = 00
DIGITAL TX SMODE = 0	W_ON = 0 W_BW[2:0] = XXX	TX_ON = 1 TX_GO = 1 TXF_BP = 0 TX_OC = 1	AUX1_ON = 0	AUX2_ON = 1 AUX3_ON = 1	RXI_ON = 0 RXI_GO = 0	RXQ_ON = 0 RXQ_GO = 0	RX_SD = X RXF_BP = X RXC[1:0] = XX
DIGITAL RX SMODE = 0	W_ON = 0 W_BW[2:0] = XXX	TX_ON = 0 TX_GO = 0 TXF_BP = X TX_OC = X	AUX1_ON = 0	AUX2_ON = 1 AUX3_ON = 1	RXI_ON = 1 RXI_GO = 1	RXQ_ON = 1 RXQ_GO = 1	RX_SD = 0 RXF_BP = 0 RXC[1:0] = 00
DIGITAL IDLE SMODE = 0	W_ON = 0 W_BW[2:0] = XXX	TX_ON = 0 TX_GO = 0 TXF_BP = X TX_OC = X	AUX1_ON = 0	AUX2_ON = 1 AUX3_ON = 1	RXI_ON = 1(0) RXI_GO = 1(0)	RXQ_ON = 1(0) RXQ_GO = 1(0)	RX_SD = 0 RXF_BP = 0 RXC[1:0] = 00

Notes:
X = irrelevant under indicated conditions.

Assume AUX2 = AFC, and AUX3 = AGC.

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Digital Interface Description
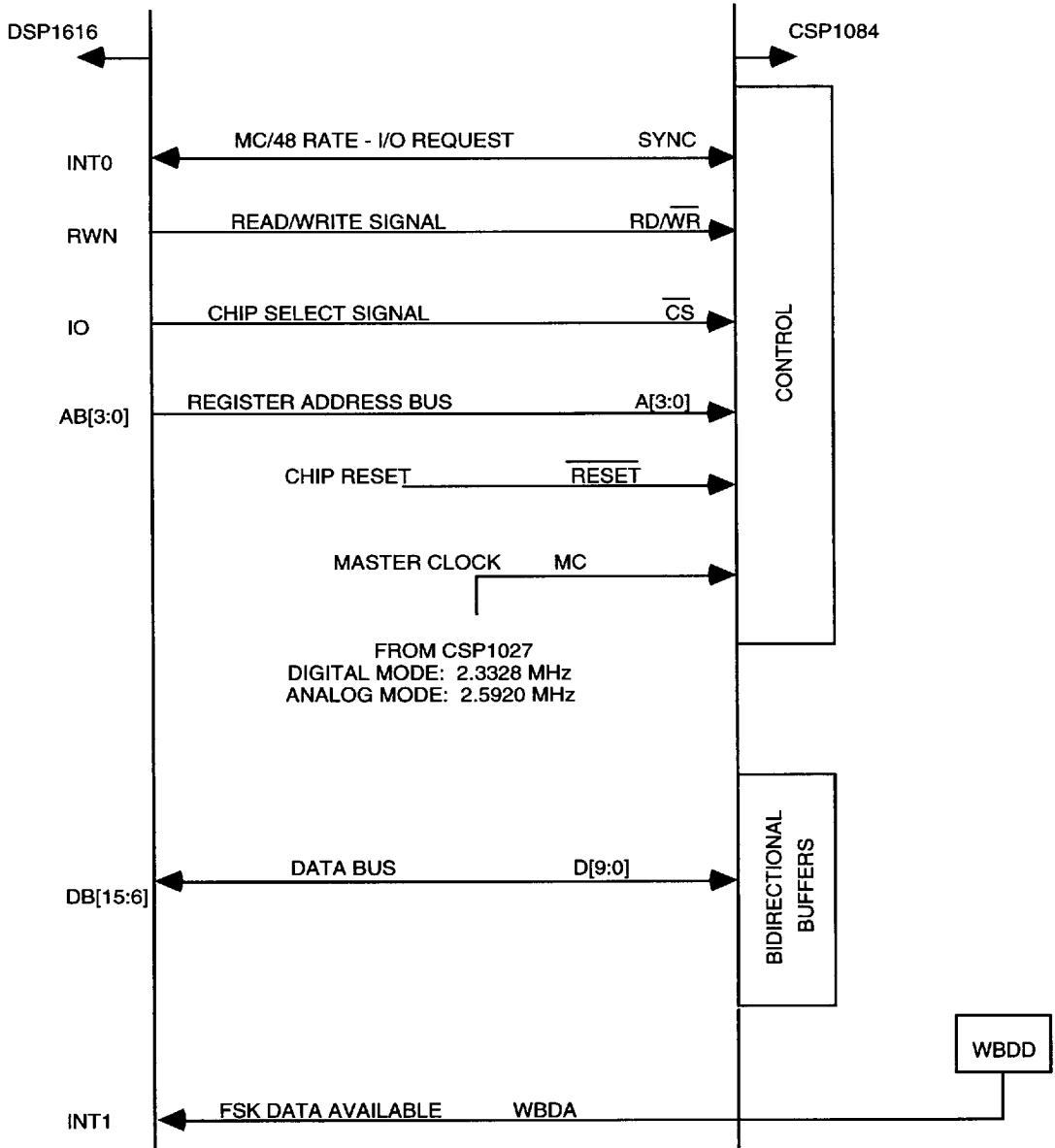
Figure 5. Digital Interface

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Digital Interface Description (continued)

The CSP1084 digital interface consists of the master clock input (MC), the 10-bit bidirectional bus interface (D[9:0], A[3:0], RD/$\overline{\text{WR}}$, $\overline{\text{CS}}$, SYNC, and WBDA), and the reset input ($\overline{\text{RESET}}$). The bus interface is compatible with the AT&T DSP1610/1616 digital signal processors. An example of how the CSP1084 interfaces with a DSP1616 and CSP1027 handset interface is shown in Figure 4.

During normal operation (SMODE = 0), the data synchronization signal SYNC is active and pulses once every 48 MC cycles for a duration of 1 MC cycle[*]. The period between two consecutive SYNC pulses defines one set of I/O operations in which multiple reads (except from WBDD) and/or multiple writes may occur (see Figure 5). The occurrence of a SYNC pulse is generally used to initiate an interrupt routine (lasting at least 1 MC cycle) that performs the necessary I/O operations. The registers that need to be accessed can be determined by keeping track of the operational state of the device. Data written to a register during I/O operation N is not used until the SYNC pulse defining I/O operation N + 1 occurs.

When W_ON = 1, the wideband data demodulator is active and WBDA pulses once approximately every 1 ms (assuming W_SEL8 = 0) for a duration of 1 MC cycle. These pulses indicate that the WBDD register is full with new data and that it should be read before the next WBDA pulse (see Figure 5). The occurrence of a WBDA pulse is generally used to initiate an interrupt routine (lasting at least 1 MC cycle) that performs the necessary read operations.

Note: No I/O operations should occur during the two MC cycles preceding a SYNC pulse.
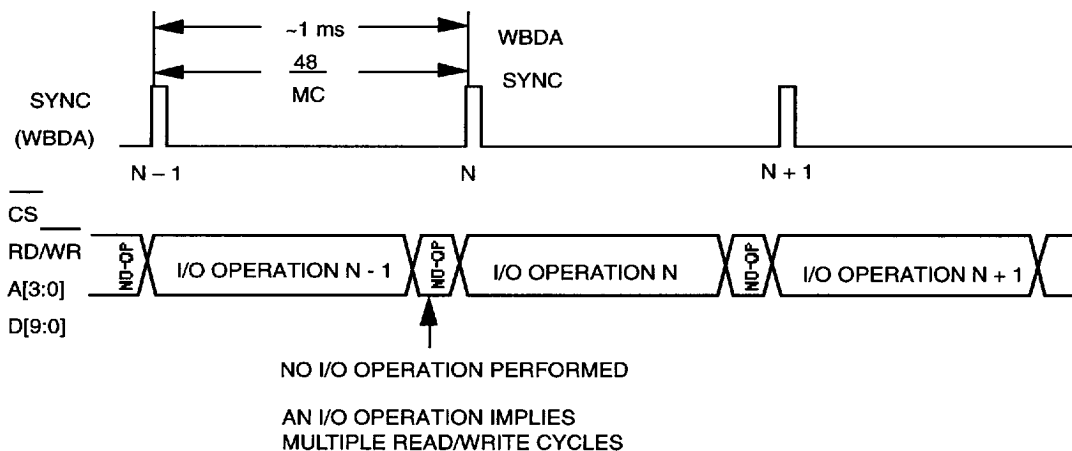
NOTE: Figure is not drawn to scale.

Figure 6. I/O Synchronization

[*] The duration in units of time of 1 MC cycle is 1/MC, where MC is the frequency of the master clock.

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Digital Interface Description (continued)

Write Operation

The CSP1084 register write cycle is shown in Figure 6. The write cycle is initiated when $\overline{CS}$ goes low and RD/$\overline{WR}$ is low. The address of the register and the data to be written are applied to the device as shown. The data is latched when the RD/$\overline{WR}$ signal changes from low to high. All registers except RXI, RXQ, and WBDD (addresses 6, 7, and 10, respectively) can be written. The write operation shown corresponds to a AT&T DSP1616 write cycle with two wait-states. For detailed timing information, see Figure 42 and Table 22.
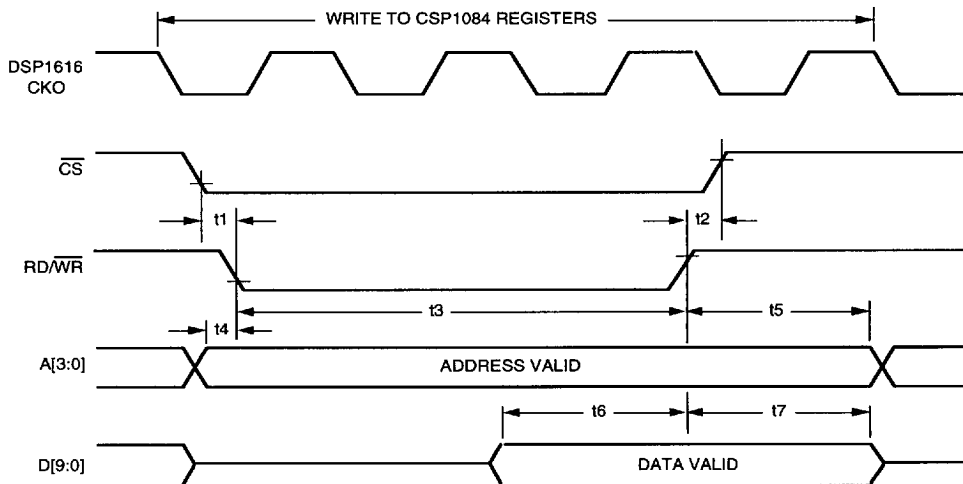
Figure 7. Write Cycle

Digital Interface Description (continued)

Read Operation

The CSP1084 read cycle is shown in Figure 7. During the read cycle, the chip select signal $\overline{CS}$ must go low, the read/write signal RD/$\overline{WR}$ must be high, and the address should be held valid as shown below. The read operation corresponds to a AT&T DSP1616 read cycle with two wait-states. For detailed timing information, see Figure 43 and Table 23.
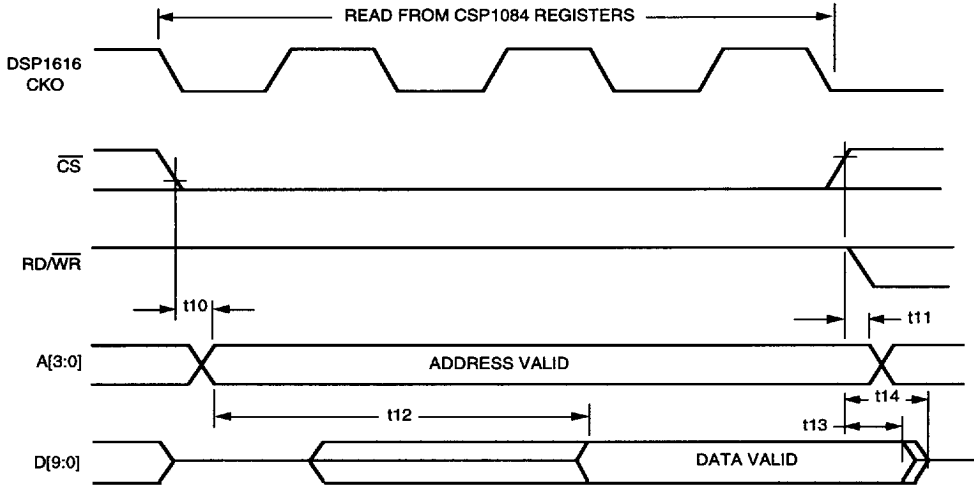
Figure 8. Read Operation

Transmit Channel (TXI, TXQ) Operation

Figure 8 shows the ramping operation performed by the TXI/TXQ channel when in digital TX mode. The TXE signal can be used to turn on the power amplifier circuit in the RF section. Since the analog RF circuits typically take 10 μs to respond, the beginning of TXI/TXQ ramp-up has been delayed to prevent any abrupt increase in transmitted signal power. At the end of the TX time slot, the TXI/TXQ levels will ramp down. The end of ramp-down and the falling edge of the TXE signal allow for the power amplifier circuits to turn off completely before the start of the power ramp-up in the next time slot. The detailed timing specifications of this operation are in Figure 9, TXI/TXQ Digital Mode Ramp-Up Synchronization.

156 SYMBOL PERIODS
157 MAXIMUM EFFECT POINTS

TXI, TXQ RAMPING

0 1 2 3 4 5 6 7 8 161 162 0 1 2 3 4

TXE
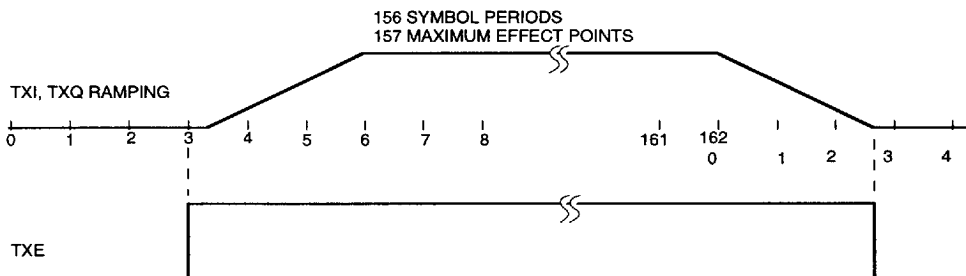
Figure 9. TX Channel Power Ramping

The transmit channel (TXI, TXQ) is controlled by bits 1 and 2 (TX_ON and TX_GO) of the CONTROLA register (see Table 5) and by bits 1 and 2 (TXF_BP and TX_OC) of the CONTROLB register (see Table 6). When the D/A converter circuits are powered on, Figure 9 shows that conversions begin when TX_GO is set to 1. SYNC will pulse once every 48 MC cycles to indicate the request for new data. Data can be written at any time between SYNC pulses as shown in Figure 5.

When operating in the digital mode (TXF_BP = 0), the π/4-shifted DQPSK modulator receives data (via bit 0 of TXI) at an MC/48 rate and presents the in-phase and quadrature-phase symbols to the FIR filters at an MC/96 rate. The outputs of these filters are interpolated by a factor of eight and filtered at the TXI and TXQ data conversion rate of MC/3. In analog mode (TXF_BP = 1), the FIR filters receive 10-bit data directly from the TXI and TXQ registers at the MC/48 rate.

In digital mode, TXE is held low and the outputs of the transmit channel are held at a differential zero level for 538 MC cycles during which the dc offset correction is performed and the power-ramping is initialized. Power ramp-up begins 14 μs after the TXE rising edge and lasts for 256 MC cycles. Precise timing is shown in Figures 9 and 10. Due to temperature and manufacturing process variations, however, the power ramp-up and hence the maximum effect point of the first transmitted symbol could be delayed by no more than 4.8 μs. Subsequent symbols will have maximum effect points that are separated by one symbol period (or 2 x 48 MC cycles).

Transmit Channel (TXI, TXQ) Operation (continued)

Figure 10. TXI and TXQ Digital Mode Ramp-Up Synchronization
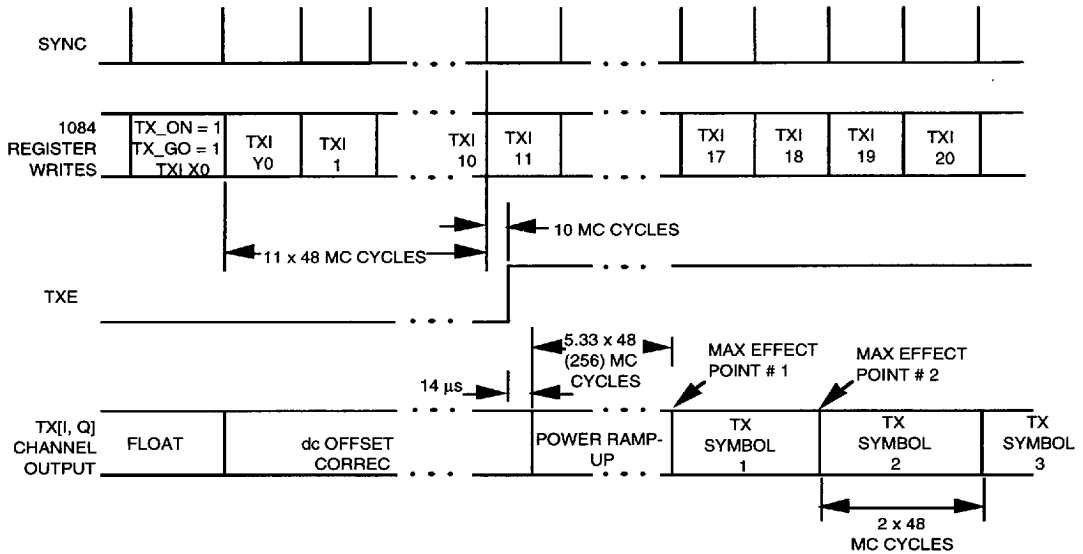
Notes:

The initial state of TX modulator (maximum effect point #1) is determined by TXI input bits X0 and Y0. If no data is written, the current value of TXI is used.

The first two data bits, TXI1 and TXI2, determine the phase change during TX symbol period 1 and the state at maximum effect point #2.

$TXF\_BP = 0$, $TX\_OC = 1$.

MC = 2.3328 MHz.

TXE depends on MC and SYNC only.

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Transmit Channel (TXI, TXQ) Operation (continued)
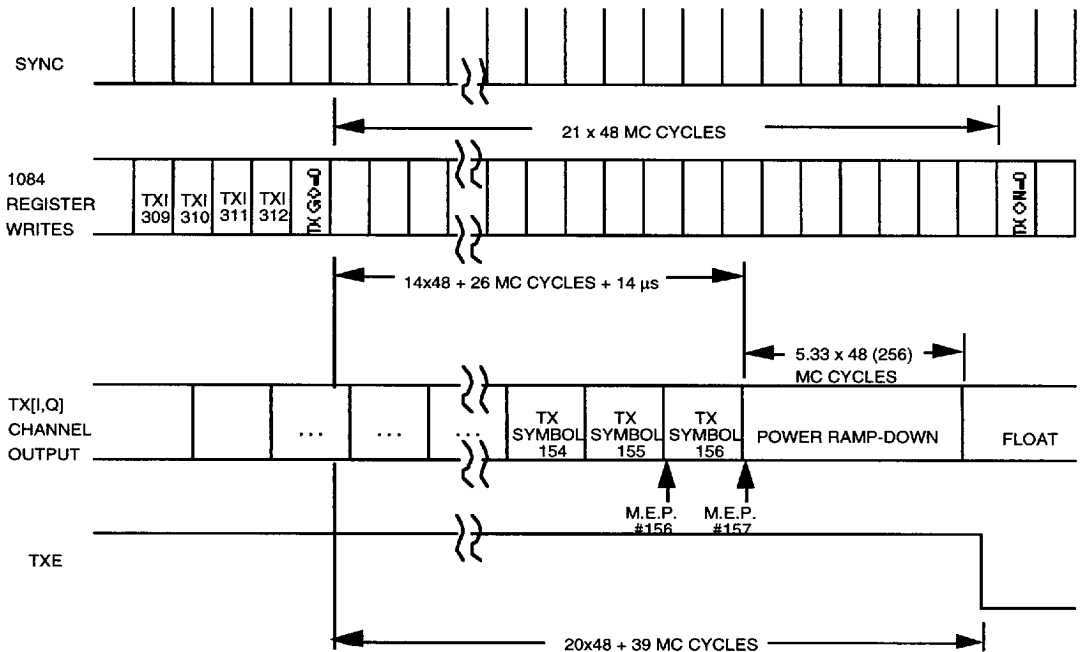
Figure 11. TXI and TXQ Ramp-Down Synchronization

The power ramp-down lasts 256 MC cycles (32 less than three symbol periods) from the m.e.p. of the last transmitted symbol. Even in the worst-case situation of an analog delay of eleven MC cycles in m.e.p. timing of the first symbol, the power ramp-down will end at the same time as the TXE falling edge.

AUX1 9-Bit D/A Converter Operation

The AUX1 D/A converter operation is controlled by AUX1_ON, bit 3 of the CONTROLA register (see Table 5). When AUX1_ON = 0, the AUX1 D/A converter circuits are in powerdown mode, and the AUX1 output is switched to GNDAF. When AUX1_ON = 1, the D/A converter circuits are powered on, and data conversions are performed at the rate of MC/48.

The data input to the converter is buffered internally, and, if new data is written into the AUX1 register (address 3), it gets loaded at the beginning of the next conversion cycle. Therefore, the delay from a write of data to the AUX1 register until the converted value is present at the AUX1 output will be less than one conversion cycle (<48 MC cycles).

If desired, this D/A converter can be used for transmit power level control.

AUX2/AUX3 10-Bit D/A Converter Operation

The AUX2/AUX3 D/A converter operation is controlled by AUX2_ON and AUX3_ON, bits 4 and 5 of the CONTROLA register (see Table 5). When AUX2_ON and AUX3_ON are set to 0, the AUX2 D/A converter circuits are in powerdown mode. In powerdown mode, AUX2 maintains a dc level of VCMTX, and AUX3 is held at GNDAF. If only one of AUX2_ON and AUX3_ON is set to 1, the D/A converter circuits are powered on and data conversions are performed at an MC/48 rate for the active output. When both AUX2_ON and AUX3_ON are set to 1, the D/A converter circuits are powered on and the 10-bit D/A converter alternately performs data conversions for each output at an MC/96 rate.

The data input to the converter is buffered internally, and, if new data is written into the AUX2 register (address 4) or the AUX3 register (address 5), it gets loaded at the beginning of the next conversion cycle. Therefore, the delay from a write of data to the AUX2 (AUX3) register until the converted value is present at the AUX2 (AUX3) output will be between one and two conversion cycles.

The use of AUX2 is recommended for producing the AFC signal, and AUX3 is recommended for the AGC signal. Since these signals are not required to vary in the analog and standby modes, the 10-bit converter may be turned off by setting AUX2_ON and AUX3_ON to zero. With the D/A converter off, AUX2 maintains a midpoint reference and AUX3 maintains a ground reference.

A circuit such as that in Figure 11 can be used on the outputs of AUX2 and AUX3 for suppression of transients caused by the switching of the output sample-and-hold circuit.
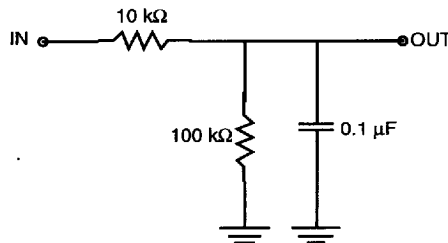
Figure 12. AUX2 and AUX3 Output Filter

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Receive Channel (RXI, RXQ) Operation

The receive channel operation is controlled by bits 6 through 9 (RXI_ON, RXI_GO, RXQ_ON, RXQ_GO) of the CONTROLA register and by bits 3 through 6 (RX_SD, RXF_BP, RXC0, RXC1) of the CONTROLB register (see Tables 5 and 7 and associated text for details).

Figure 12 shows the timing and synchronization for the receive channel. This applies to the normal, manual, and off modes of the dc offset correction circuit (see Control Register Descriptions and Table 6).

RX[I, Q]_ON should be set to 1 at least one cycle before RX[I, Q]_GO = 1. Assuming RX[I, Q]_ON = 1, the RX[I, Q] receive channel will start up when RX[I,Q]_GO is set to a 1. The output of the channel is blocked for 21 decimation cycles to allow extraneous values in the decimator and postfilter to clear. The RXI and RXQ registers are loaded simultaneously, once every 48 MC cycles, as shown in Figure 12. The RXI and RXQ registers may be read anytime during each conversion cycle between the SYNC pulse and the load of the next A/D result. If RX_SD = 1, the FM_disc input is multiplexed into the RXQ path and the quadrature-phase input (RXQP and RXQN), if any, is ignored. Also, if RX_SD = 1, the RXIA input is multiplexed into the RXI path and the quadrature-phase input (RXIP and RXIN), if any, is ignored.
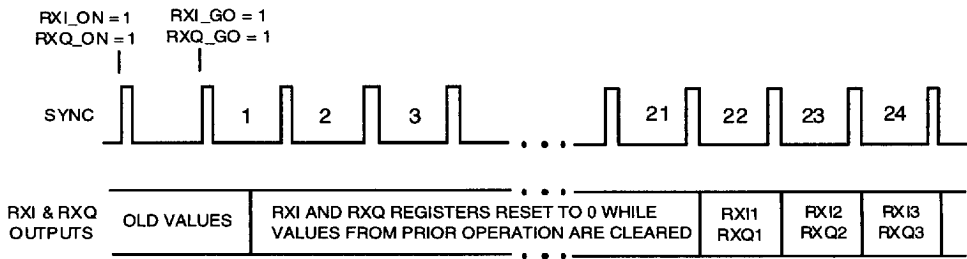
Figure 13. Receive A/D Synchronization

Wideband Data Demodulator (WBDD) Operation

The wideband data demodulator (WBDD) is controlled by bits 4—8 (W_ON, W_BW0, W_BW1, W_BW2, and W_SEL8) of register 9 (see Tables 8 and 10 and associated text for details). WBDD uses an internal 10 kHz clock generated by a first-order digital PLL to capture and decode the received Manchester coded data. The digital PLL consists of a phase detector, a gain stage, and a digital VCO. After decoding and storing ten (eight if W_SEL8 = 1) bits of data in the WBDD register, the status signal WBDA will pulse high to indicate that new data is available. The bit WBD0 (LSB) is first in time. The WBDD register can be read anytime between the pulses which are synchronous with the internal 10 kHz clock generated by the digital PLL (see Figure 3 and Digital Interface Description).

When entering the initialization/idle mode, the WBDD bandwidth should be set at 102.8 Hz and W_LOCK = 0. This allows the PLL to lock onto the incoming signal quickly. Once the device processing the FOCC data stream has found two consecutive WORD_SYNC patterns (11100010010) separated by 452 bits, it should set WBDD bandwidth to 12.4 Hz and W_LOCK to 1. This ensures that the WBDD timing recovery mechanism stays locked with respect to the incoming FOCC signal. If WORD_SYNC is lost, the procedure should be repeated as if the initialization/idle mode was being re-entered. Once the device processing the FOCC data has found the SYNC pattern, the bandwidth may be changed to the minimum setting, where it is maintained for FOCC reception.

When entering the analog mode, the bandwidth should be changed to 102.8 Hz and W LOCK to 0 and maintained in that state for FVC reception.

A microprocessor may be used to process FOCC data in idle mode via the 8-bit interface. In that case, the processor controlling the CSP1084 must first go through the initialization/idle mode. After setting the WBDD bandwidth to 12.4 Hz and W_LOCK to 1, it should set W_SEL8 to 1. This results in WBDD output appearing at the 8-bit interface where it can be read by the microprocessor. The timing requirements for the 8-bit interface are shown in Table 12 and Figure 13.

Note: No read operations should be performed on the WBDD register during the two MC cycles preceding a WBDA pulse.
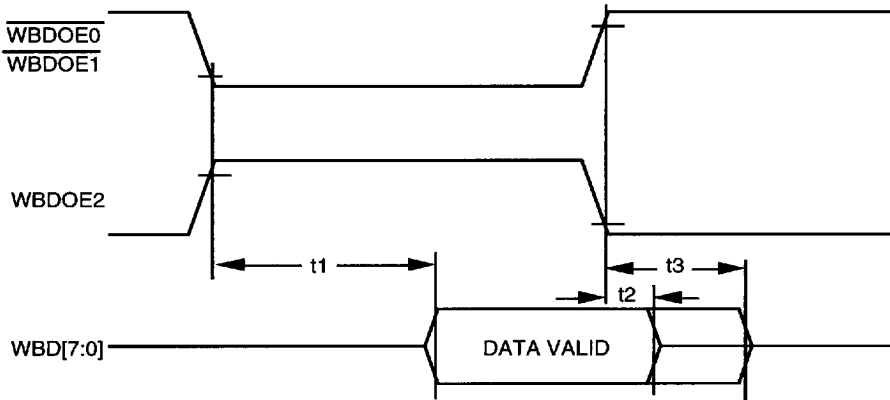
Figure 14. WBDD Microprocessor Interface Timing

Table 12. WBDD Microprocessor Interface Timing

Label	Description	Min	Max	Unit
t1	Enable Valid to Data Valid	—	70	ns
t2	Data Valid After Enable Invalid	0	—	ns
t3	Enable Invalid to Data 3-state	—	50	ns

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External Configuration

The CSP1084 has six power pins and seven ground pins. The two V$_{DDD}$ and the three GND$_D$ pins are for the digital portions of the device. The V$_{DDD5}$ and GND$_{D5}$ pins are for the digital portion of the device that interfaces directly to analog blocks. The V$_{DDAT}$, GND$_{AT}$, V$_{DDAF}$, GND$_{AF}$, V$_{DDAR}$, and GND$_{AR}$ pins are for the analog portions of the device. The digital inputs and outputs are fully TTL compatible.

The SCANI, $\overline{RESET}$, $\overline{CS}$, $\overline{WBDOE0}$, $\overline{WBDOE1}$, and D[9:0] pins have internal pull-up devices with a minimum value of 100 kΩ. The WBDOE2 pin has an internal pull-down device with a minimum value of 50 kΩ.

The TXI and TXQ pins are designed to be dc coupled to external circuits, while the RXI and RXQ pins are designed to be capacitively coupled. The capacitor values are chosen based on the lowest frequency that is to be processed. On the receive channels, the guaranteed minimum input resistance is 100 kΩ. Therefore, a coupling capacitor of 0.1 μF on RXI and RXQ results in a corner frequency of less than 16 Hz.

The following pins require external bypassing capacitors: VADP, VADN, VCM, V$_{DDD}$, V$_{DDD5}$, V$_{DDAF}$, V$_{DDAR}$, and V$_{DDAT}$. The V$_{DDD}$ pins should be bypassed with a 4.7 μF tantalum capacitor and a 0.1 μF ceramic capacitor connected in parallel to GND$_D$. V$_{DDD5}$ should be bypassed with a 4.7 μF tantalum capacitor and a 0.1 μF ceramic capacitor connected in parallel to GND$_{D5}$. VADP, VADN, VCM, and VDDAR should each be bypassed with a 4.7 μF tantalum capacitor and a 0.1 μF ceramic capacitor connected in parallel to GND$_{AR}$. V$_{DDAT}$ should be bypassed with a 4.7 μF tantalum capacitor and a 0.1 μF ceramic capacitor connected in parallel to GND$_{AT}$. V$_{DDAF}$ should be bypassed with a 4.7 μF tantalum capacitor and a 0.1 μF ceramic capacitor connected in parallel to GND$_{AF}$.

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Device Characteristics

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Table 13. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	55	125	°C
Lead Temperature	—	—	300	°C
Voltage on Any Digital Pin to GNDD	—	$V_{DDD} - 0.5$	$V_{DDD} + 0.5$	V

Maximum ratings are the limiting conditions which can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

Handling Precautions

All MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Although input protection circuitry has been incorporated into the devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting. AT&T employs a human-body model for ESD susceptibility testing. Since the failure voltage of electronic devices is dependent on the current, voltage, and, hence, the resistance and capacitance, it is important that standard values be employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the AT&T human-body model test circuit. The breakdown voltage for the CSP1084 is greater than 1000 V.

Recommended Operating Conditions

Table 14. Operational Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A	−40	—	85	°C
Any Digital Supply: V_{DDD}	—	3.0	5.0	5.25	V
Digital Supply: V_{DDD5}	—	4.75	5.0	5.25	V
Any V_{DDA} Supply: V_{DDAT}, V_{DDAR}, V_{DDAF}	—	4.75	5.0	5.25	V
V_{DDA} to V_{DDA}: Any V_{DDAT}, V_{DDAR}, V_{DDAF}	—	−30	—	30	mV
Ground to Ground: Any GND_{AT}, GND_{AF}, GND_{AR}, GND_D	—	−10	—	10	mV

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Electrical Characteristics and Requirements

Table 15. Typical Power Consumption

These values assume the conditions shown in Table 11.
AUX2 = AFC, AUX3 = AGC, and AUX1_ON = 0.

Mode	Analog Supply Power				Digital Supply Power							
	V_{DDD5} = 5.0 V, V_{DDAF} = 5.0 V V_{DDAR} = 5.0 V, V_{DDAT} = 5.0 V				V_{DDD} = 5.0 V				V_{DDD} = 3.3 V			
	Typ	Unit	Typ	Unit	Typ	Unit	Typ	Unit	Typ	Unit	Typ	Unit
Digital	14.0	mA	70	mW	3.0	mA	15.0	mW	1.6	mA	5.3	mW
Analog	19.8	mA	99	mW	3.7	mA	18.5	mW	1.9	mA	6.3	mW
Standby	2.6	mA	13	mW	1.9	mA	9.5	mW	0.9	mA	3.0	mW

Table 16. dc Characteristics (over Operating Ranges) of Digital I/O

V_{DDD} = 5.0 V, V_{DDAF} = 5.0 V, V_{DDAR} = 5.0 V, V_{DDAT} = 5.0 V, V_{DDD5} = 5.0 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage:						
Low	V_{IL}	—	—	—	0.8	V
High	V_{IH}	—	2.0			V
Output Voltage:						
Low	V_{OL}	I_{OL} = +1.0 mA	—	—	0.4	V
High	V_{OH}	I_{OH} = −1.0 mA	2.4	—		V
Digital Input Capacitance	CIN			10		pF
Input Leakage Current:						
Low	I_{IL}	V_{IL} = 0	10	—	—	μA
High	I_{IH}	V_{IH} = V_{DDD}	—	—	10	μA

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Circuit Characteristics

Operational characteristics as specified in Table 14. $T_A = -40°C$ to $+85°C$, $V_{DDD} = 3.0$ to 5.25 V, $GND_D = 0.0$ V, $V_{DDAF} = 5$ V $\pm 5\%$, $GND_{AF} = 0.0$ V, $V_{DDAR} = 5$ V $\pm 5\%$, $GND_{AR} = 0.0$ V, $V_{DDAT} = 5$ V $\pm 5\%$, $GND_{AT} = 0.0$ V, $V_{DDD5} = 5$ V $\pm 5\%$, $GND_{D5} = 0.0$ V

Two's complement format is used for the A/D and D/A circuits.

Table 17. Transmit Channel Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Word Length	—	—	—		8	bits
Differential Output Voltage Range	—	2 < VCMTX < 3	—	2.5	—	Vpp
Differential Offset: TXIP to TXIN or TXQP to TXQN	—	Without correction	—	±10	±20	mV
Differential Offset: TXIP to TXIN or TXQP to TXQN	—	With correction	—	—	±2.5	mV
Pass Band	—	Analog mode	—	16	—	kHz
Pass Band Ripple	—	Analog mode	—	±0.4	±1	dB
Pass Band Delay Distortion	—	—	—		0.5	μs
I and Q Mismatch	—	Full-scale amplitude	—	0.1	0.3	dB
Differential Nonlinearity	DNL	—	—	±0.5	±1	LSB
Integral Nonlinearity	INL	—	—	±0.5	±1	LSB
Sample Rate	—	—	—	—	MC/3	Hz
I and Q Sampling Mismatch	—	Guaranteed by design	—	—	20	ns
Load Resistance	—	dc coupled	10	—	—	kΩ
Load Capacitance	—		—	—	50	pF

Table 18. 9-Bit (AUX1) D/A Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Word Length	—	—	—	—	9	bits
Minimum Voltage	—	—	0.25	0.5	0.75	V
Maximum Voltage	—	—	4.0	4.25	4.5	V
AUX1 Powerdown	—	—	—	0	—	V
Sample Rate	—	—	—	MC/48	—	Hz
Differential Nonlinearity	DNL	—	—	—	±1	LSB
Integral Nonlinearity	INL	—	—	—	±2	LSB
Idle Voltage	—	AUX1_ON = 0	—	—	50	mV
Load Resistance	—	—	50	—	—	kΩ
Load Capacitance	—	—	—	—	50	pF

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Circuit Characteristics (continued)

Table 19. 10-Bit (AUX2 & AUX3) D/A Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Word Length	—	—	—	—	10	bits
Minimum Voltage	—	—	0.25	0.5	0.75	V
Maximum Voltage	—	—	4.0	4.25	4.5	V
AUX2 Powerdown	—	—	2.25	2.375	2.5	V
AUX3 Powerdown	—	—	—	0	—	V
Sample Rate: Either AUX2 or AUX3 Active	—	—	—	MC/48	—	Hz
Sample Rate: Both AUX2 and AUX3 Active	—	—	—	MC/96	—	Hz
Differential Nonlinearity	DNL	—	—	—	±1.0	LSB
Integral Nonlinearity	INL	—	—	±2	±4	LSB
Output Impedance	—	At dc	—	—	1	kΩ
Load Resistance	—	—	50	—	—	kΩ
Load Capacitance	—	—	—	—	20	pF

Table 20. Receive Channel Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Word Length	—	—	—	10	bits
Output Word Rate per Channel	—	—	—	MC/48	Hz
Sampling Mismatch	Guaranteed by design	—	—	20	ns
RXI, RXQ Differential Input Voltage	Capacitively coupled input *	—	—	2.8	Vpp
Nominal Gain Range	—	0	—	18	dB
Step Size	—	—	2.0	—	dB
Relative Gain Error	—	—	—	± 0.5	dB
Absolute Gain Error	—	—	—	± 1.0	dB
Input Resistance	—	100	—	—	kΩ
Input Capacitance	—	—	20	100	pF
Pass Band	Analog mode	—	16	—	kHz
Pass Band Ripple	Analog mode	—	± 0.4	±1	dB
Passband Delay Distortion	—	—	—	1.0	µs
Gain Match between I and Q	—	—	—	0.4	dB
Signal to Noise + Distortion Ratio	Input 0 dB †	55	60	—	dB
dc Offset with Correction	—	−1	0	1	LSB
RXIA Input Voltage	Single-ended, capacitively coupled, PGA = 0 dB	—	—	3	Vpp
RXIA Input Resistance	—	20	—	—	kΩ
FM_disc Input Voltage	Single-ended, capacitively coupled, PGA = 0 dB	—	—	1.4	Vpp
FM_disc Input Resistance	—	20	—	—	kΩ

* PGA gain set to 0 dB.
† Input signal 1.4 V peak differential and PGA gain set to 0 dB.

Frequency Response Characteristics

The frequency response plots of the transmit (D/A) and receive (A/D) channels are provided for both digital and analog modes of operation. During analog mode, the $\sqrt{RC}$ filters in the transmit and receive paths are bypassed. Some variation in the frequency response is expected because the low-pass filter (LPF) in the transmit path and the anti maliasing filter (AAF) in the receive path are implemented by using analog circuit techniques. The variation in the transmit path LPF primarily affects the stop-band response. Figures 14—21 show the worst-case situation with the minimum stop-band attenuation.

The variation in the receive path AAF can affect both in-band and stop-band response. Therefore, Figures 22—41 are frequency response plots grouped in pairs. On each page, the top plot is for the lowest 3 dB cutoff frequency and the bottom plot is for the highest 3 dB cutoff frequency.
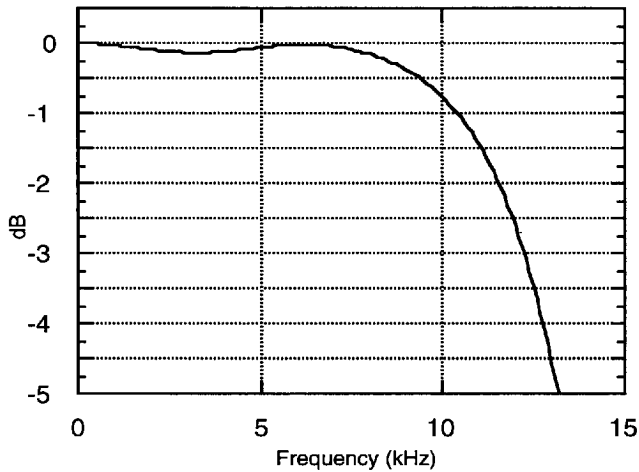
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Frequency Response Characteristics (continued)

Transmit Channel Frequency Response — Digital Mode
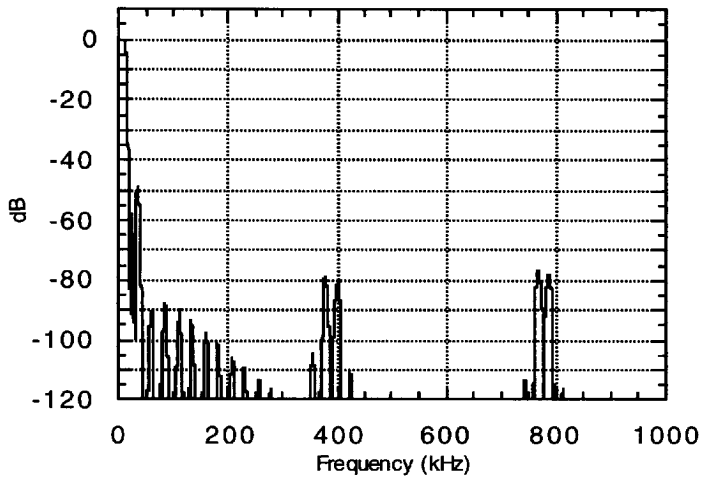
Figure 15. CSP1084 Transmit Channel Frequency Response, Digital Mode, 1000 kHz Frequency Range
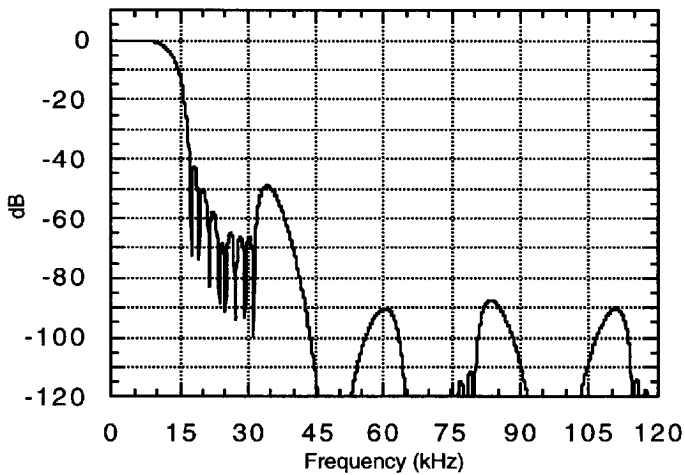
**Figure 16. CSP1084 Transmit Channel Frequency Response, Digital Mode, 120 kHz Frequency Range**

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Frequency Response Characteristics (continued)

Transmit Channel Frequency Response — Digital Mode (continued)
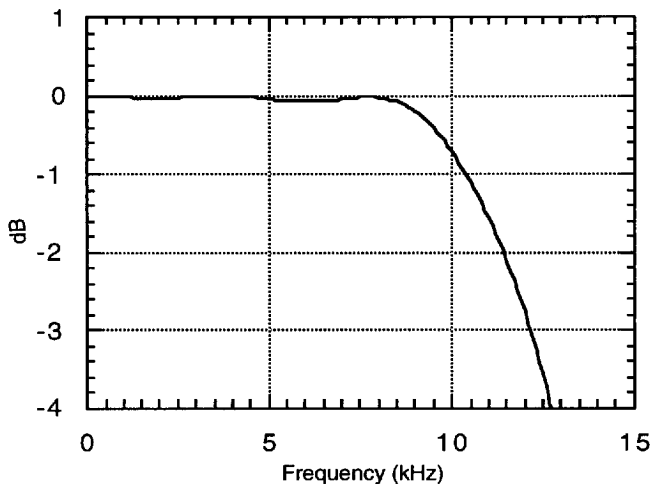
**Figure 17. CSP1084 Transmit Channel Frequency Response,
Digital Mode, 15 kHz Frequency Range**
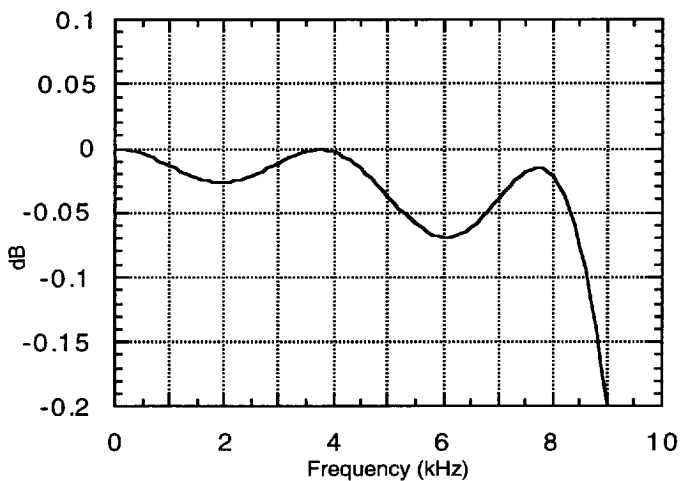
**Figure 18. CSP1084 Transmit Channel Frequency Response,
Digital Mode, 10 kHz Frequency Range**

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Frequency Response Characteristics (continued)

Transmit Channel Frequency Response — Analog Mode
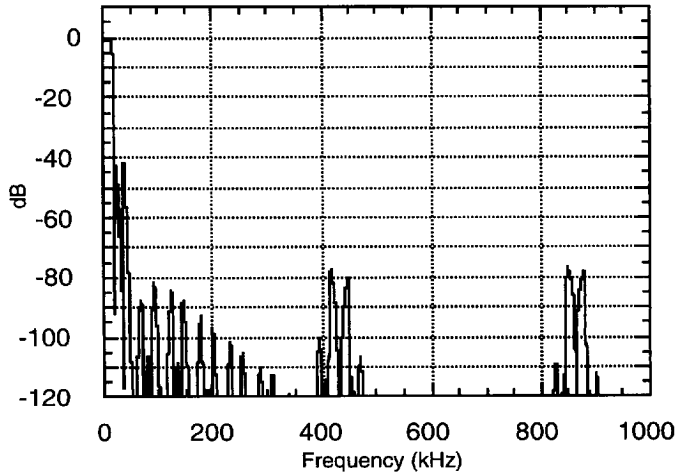
Figure 19. CSP1084 Transmit Channel Frequency Response, Analog Mode, 1000 kHz Frequency Range
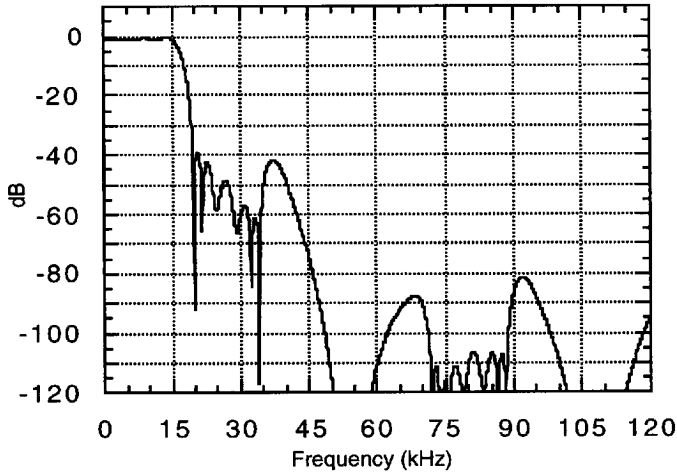
Figure 20. CSP1084 Transmit Channel Frequency Response, Analog Mode, 120 kHz Frequency Range

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Frequency Response Characteristics (continued)

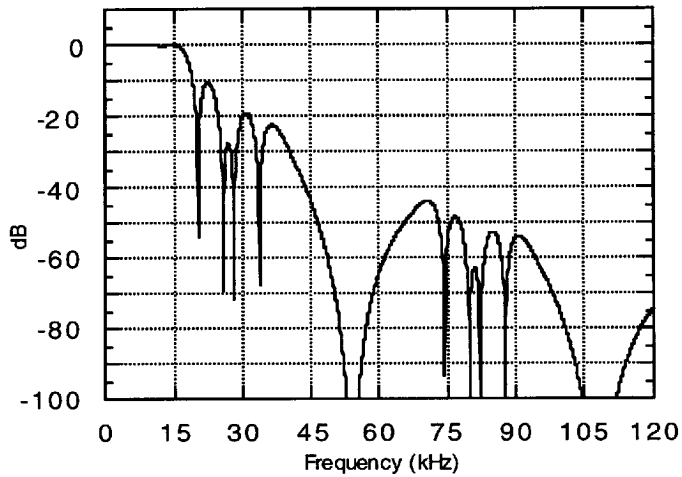## Transmit Channel Frequency Response — Analog Mode (continued)
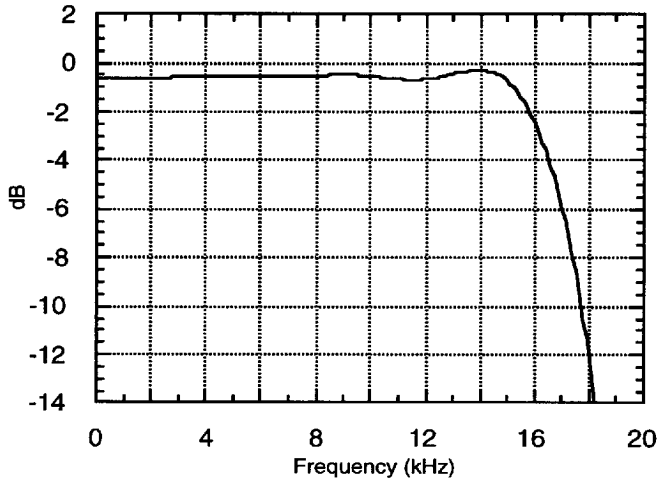
Figure 21. CSP1084 Transmit Channel Frequency Response, Analog Mode, 20 kHz Frequency Range
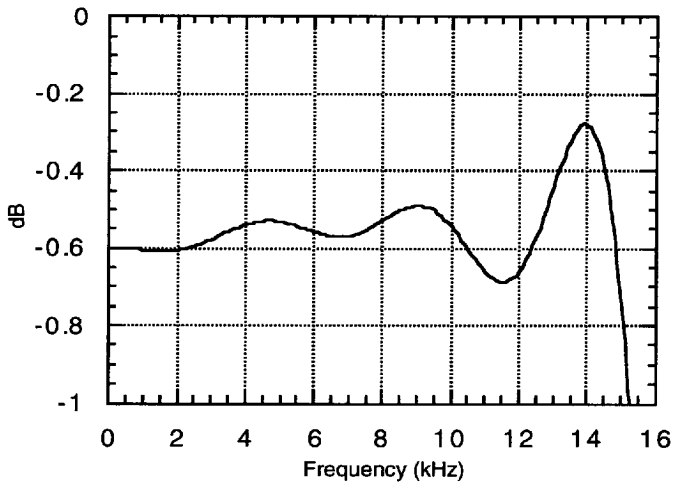
Figure 22. CSP1084 Transmit Channel Frequency Response, Analog Mode, 16 kHz Frequency Range

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Frequency Response Characteristics (continued)

Receive Channel Frequency Response — Digital Mode
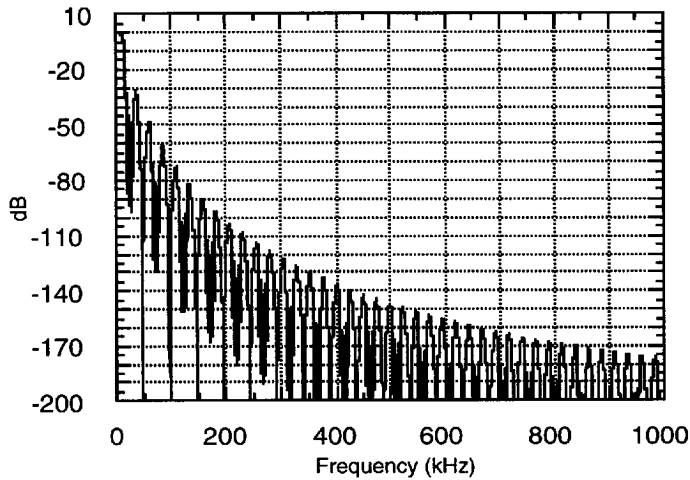
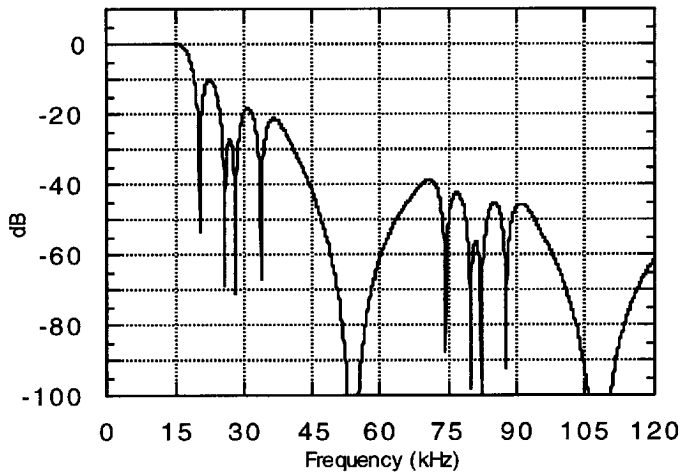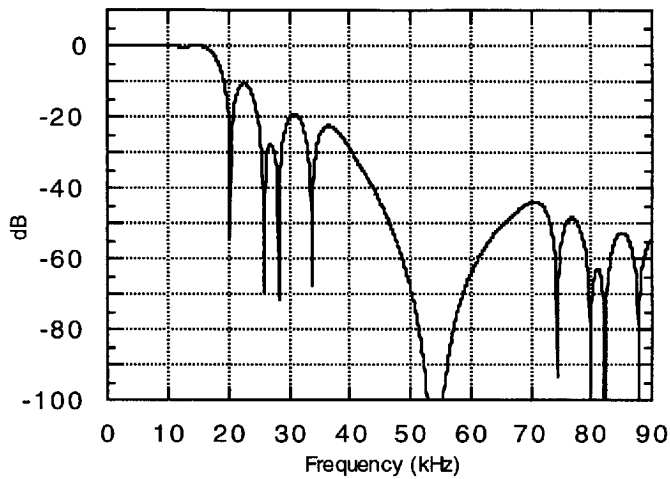**Figure 23. Receive Channel Frequency Response, Digital Mode, AAF 3 dB Frequency 53 kHz**
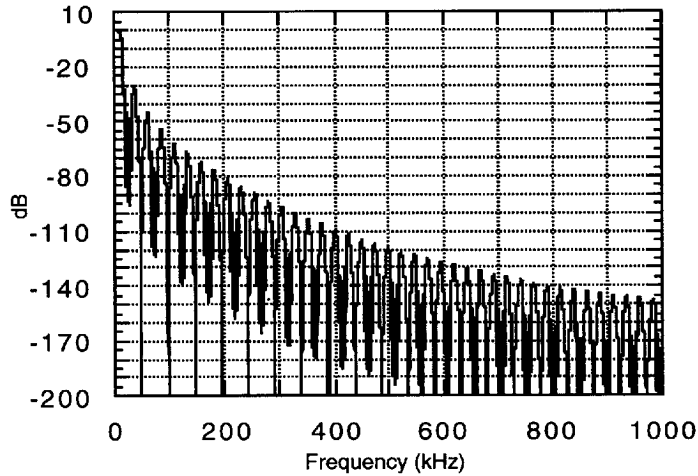
Figure 24. Receive Channel Frequency Response, Digital Mode, AAF 3 dB Frequency 160 kHz

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Frequency Response Characteristics (continued)

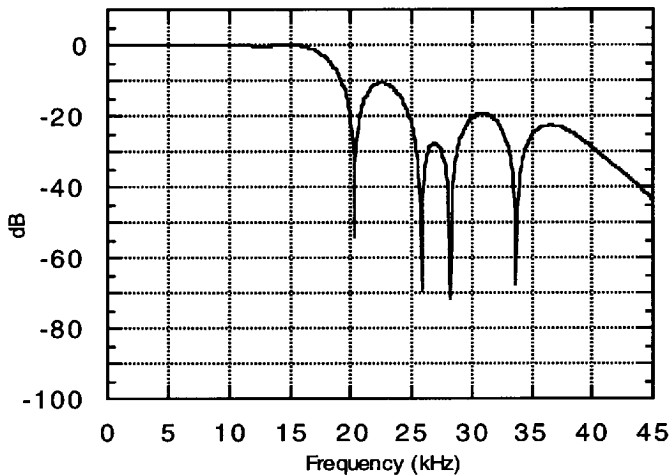### Receive Channel Frequency Response —Digital Mode (continued)
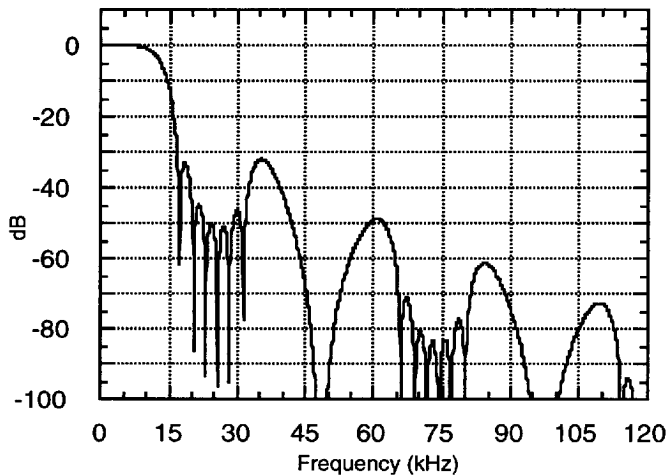
Figure 25. Receive Channel Frequency Response, Digital Mode, AAF 3 dB Frequency 53 kHz
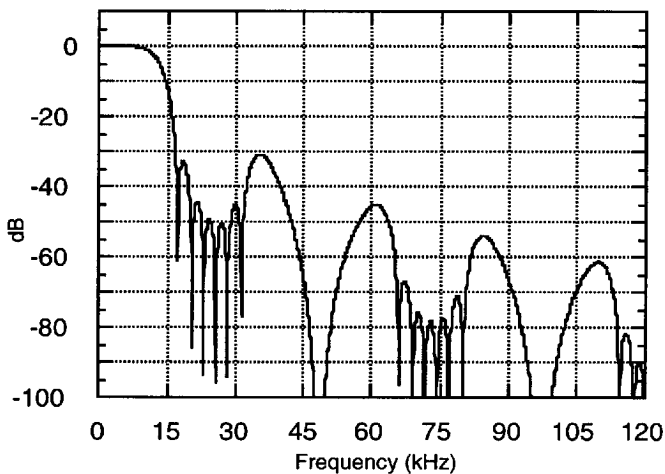
Figure 26. Receive Channel Frequency Response, Digital Mode, AAF 3 dB Frequency 160 kHz

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Frequency Response Characteristics (continued)

Receive Channel Frequency Response — Digital Mode (continued)
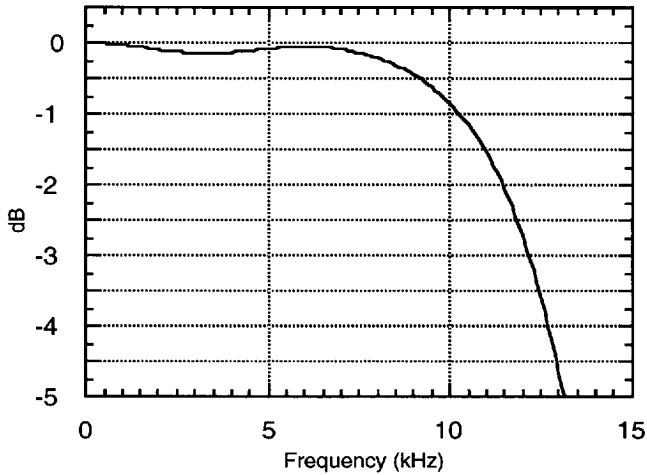
Figure 27. Receive Channel Frequency Response, Digital Mode, AAF 3 dB Frequency 53 kHz
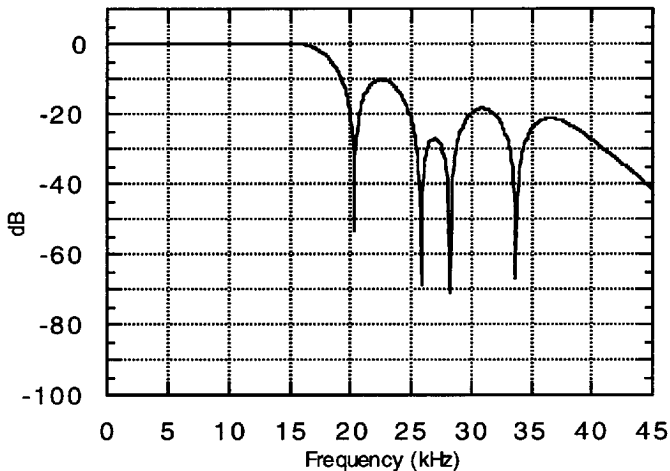

Figure 28. Receive Channel Frequency Response, Digital Mode, AAF 3 dB Frequency 160 kHz

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Frequency Response Characteristics (continued)

Receive Channel Frequency Response — Digital Mode (continued)
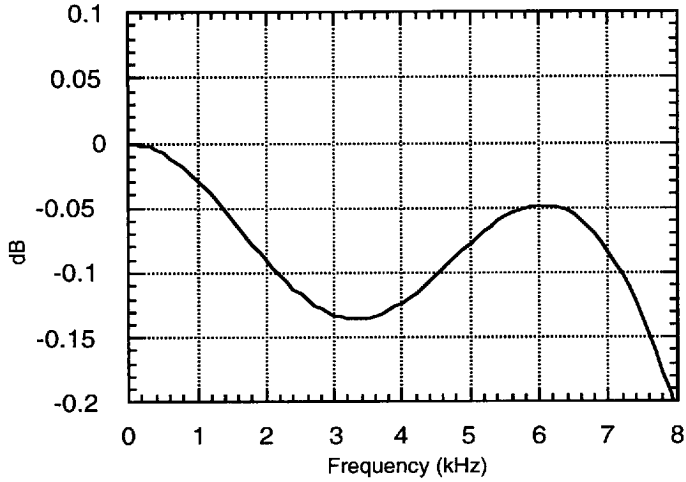
Figure 29. Receive Channel Frequency Response, Digital Mode, AAF 3 dB Frequency 53 kHz
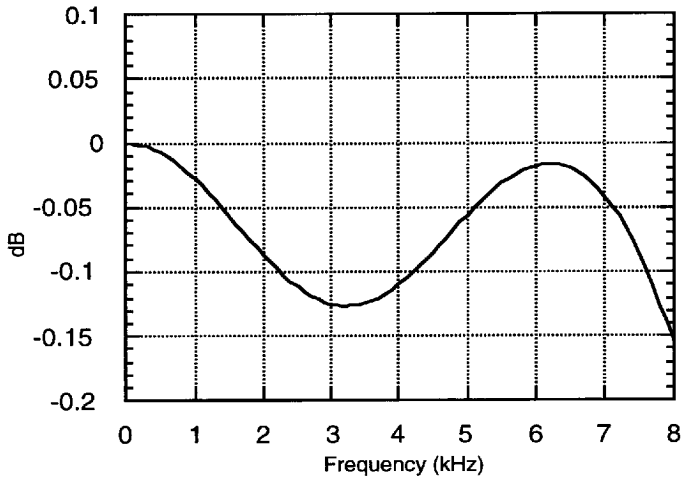
Figure 30. Receive Channel Frequency Response, Digital Mode, AAF 3 dB Frequency 160 kHz

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Frequency Response Characteristics (continued)

Receive Channel Frequency Response — Analog Mode
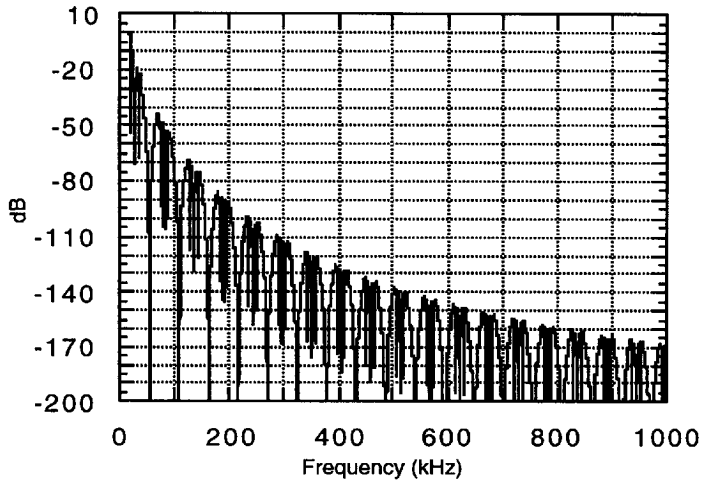
Figure 31. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 53 kHz
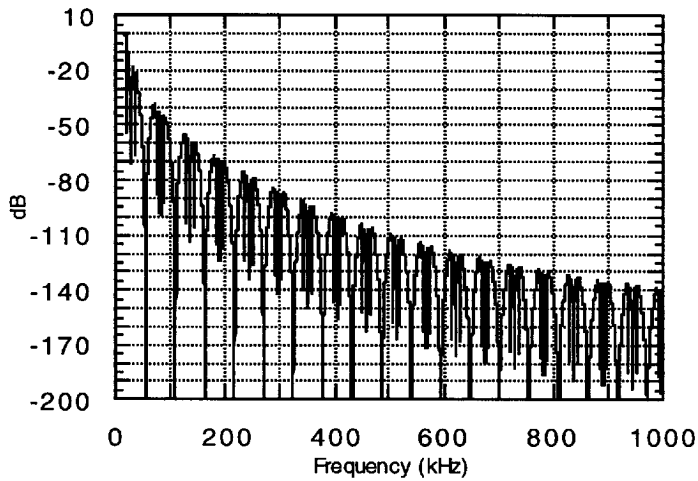
Figure 32. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 160 kHz
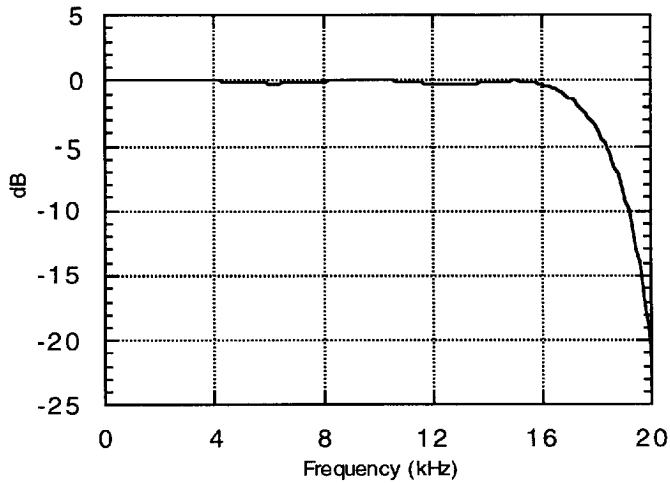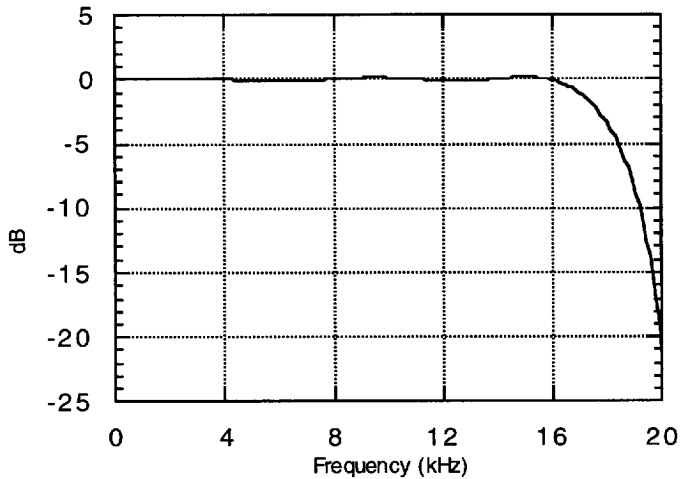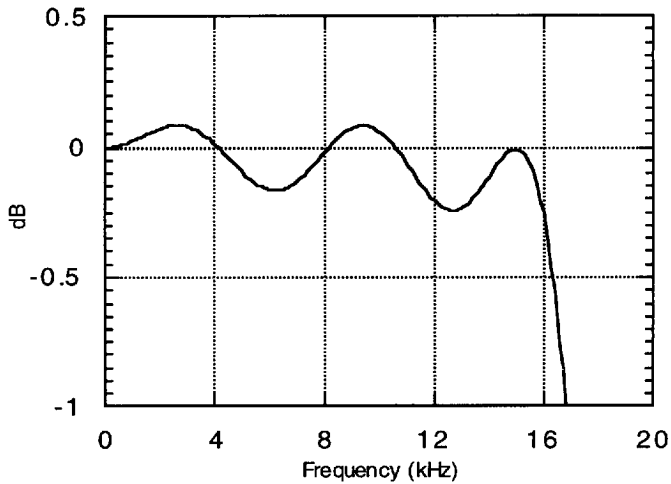
Frequency Response Characteristics (continued)

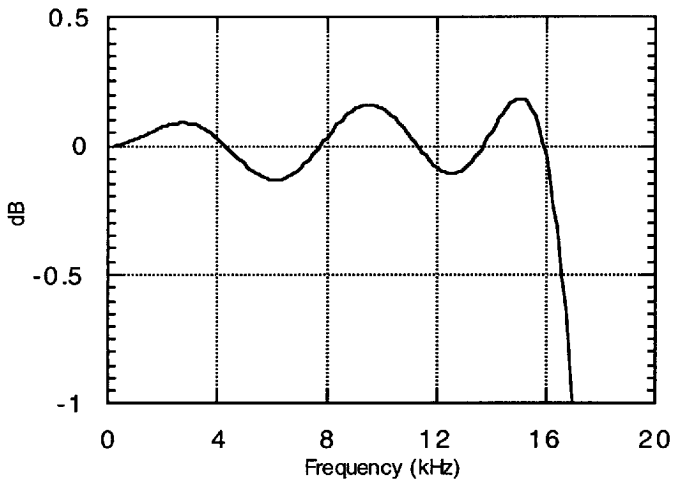## Receive Channel Frequency Response — Analog Mode (continued)

Figure 33. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 53 kHz

Figure 34. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 160 kHz

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Frequency Response Characteristics (continued)

Receive Channel Frequency Response — Analog Mode (continued)

Figure 35. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 53 kHz
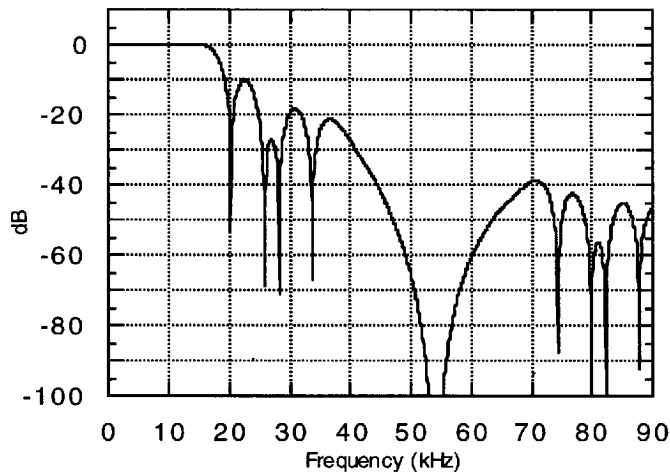
Figure 36. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 160 kHz

Frequency Response Characteristics (continued)

Receive Channel Frequency Response — Analog Mode (continued)

Figure 37. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 53 kHz

Figure 38. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 160 kHz

Frequency Response Characteristics (continued)

Receive Channel Frequency Response — Analog Mode (continued)

Figure 39. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 53 kHz

Figure 40. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 160 kHz

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Frequency Response Characteristics (continued)

Receive Channel Frequency Response — Analog Mode (continued)

Figure 41. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 53 kHz

Figure 42. Receive Channel Frequency Response, Analog Mode, AAF 3 dB Frequency 160 kHz

Timing Characteristics

Table 21. Master Clock Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Frequency: Digital Mode	—	—	2.3328	—	MHz
Frequency: Analog Mode	—	—	2.5920	—	MHz
Duty Cycle	—	47	—	53	%
Rise Time	rt	—	—	5	ns
Fall Time	ft	—	—	5	ns

Write Timing
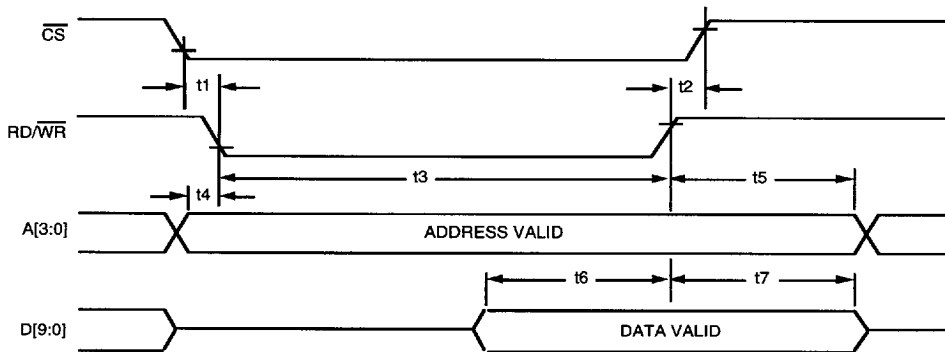
Figure 43. Write Cycle Timing

Table 22. Write Cycle Timing

Label	Description	Min	Max	Unit
t1	$\overline{CS}$ Low to RD/$\overline{WR}$ Low	—	8	ns
t2	RD/$\overline{WR}$ High to $\overline{CS}$ High	—	8	ns
t3	RD/$\overline{WR}$ Width (low to high)	90	—	ns
t4	Address Valid to RD/$\overline{WR}$ Low	0	—	ns
t5	Address Valid After RD/$\overline{WR}$ High	20	—	ns
t6	Data Valid to RD/$\overline{WR}$ High	40	—	ns
t7	Data Valid After RD/$\overline{WR}$ High	20	—	ns

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Timing Characteristics (continued)

Read Timing
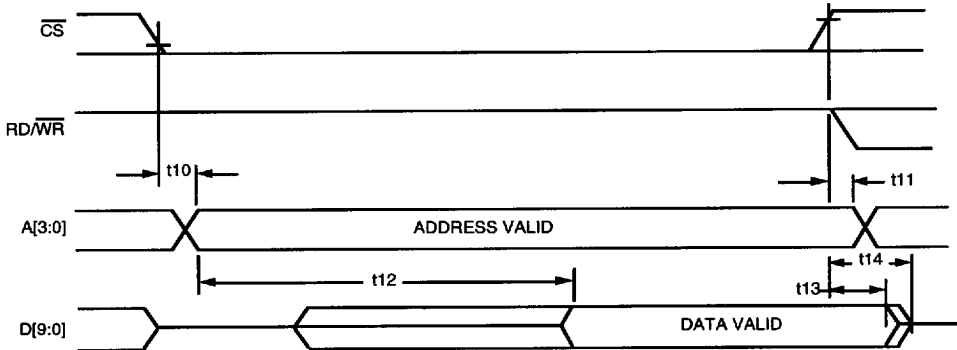
Figure 44. Read Cycle Timing

Table 23. Read Cycle Timing

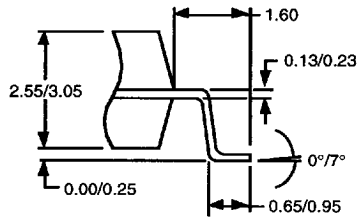| Label	Description	Min	Max	Unit
t10	$\overline{CS}$ Low to Address Valid	—	2	ns
t11	$\overline{CS}$ High to Address Valid	0	—	ns
t12	Address Valid to Data Valid	70	—	ns
t13	Data Valid After $\overline{CS}$ High	0	—	ns
t14	$\overline{CS}$ High to Data 3-State	—	—	ns

Outline Diagrams

80-Pin EIAJ Package

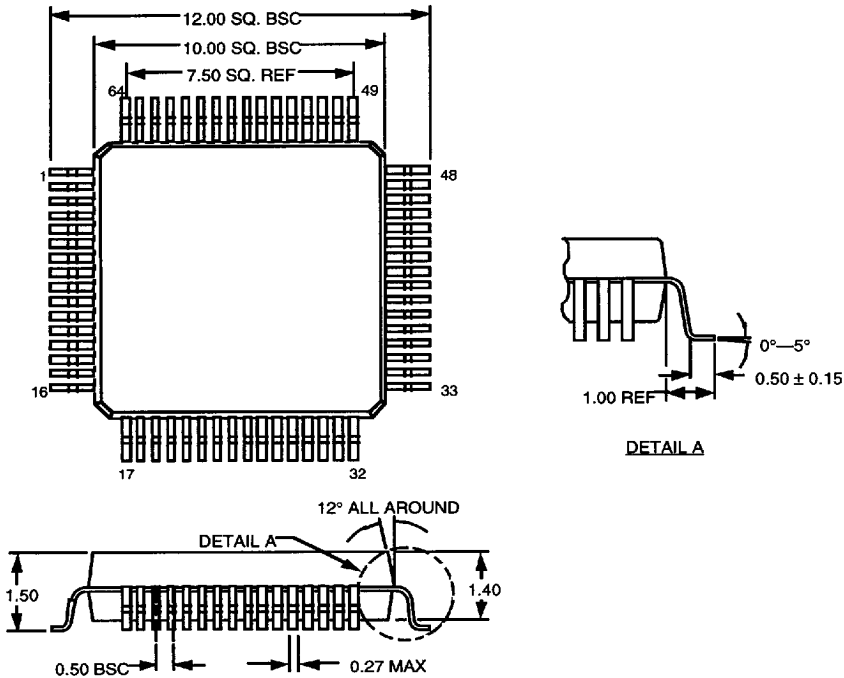All dimensions are in millimeters.
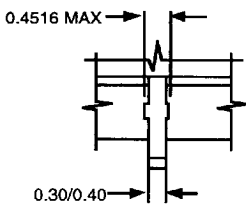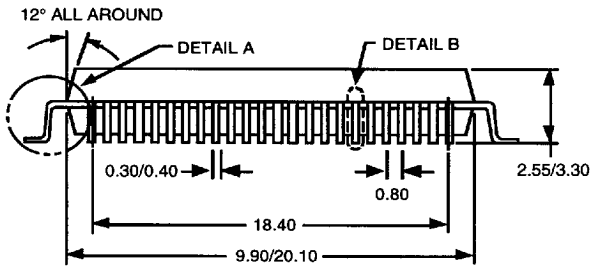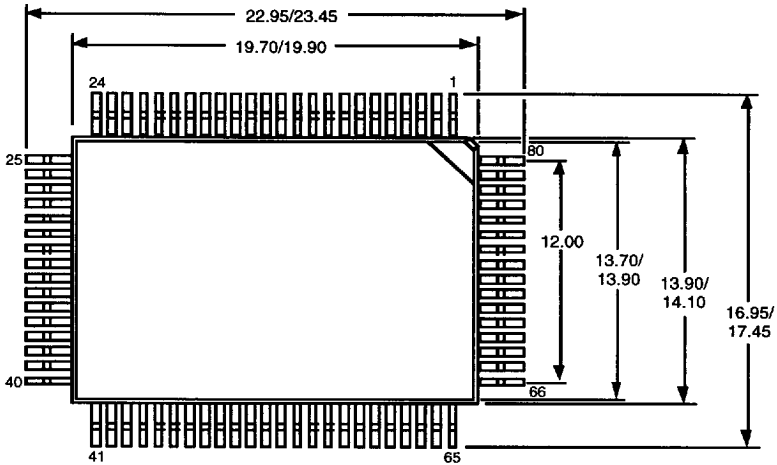
0050026 0017630 347

Outline Diagrams

64-Pin TQFP Package

All dimensions are millimeters.

DETAIL A

0050026 0017631 283

Outline Diagrams (continued)

100-Pin TQFP Thin Quad Flat Pack

All dimensions are in millimeters.

DETAIL A

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