REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Page 4: Correct table I to correspond with military specification requirements.	5-08-79	
B	Change from suggested source drawing to approved source drawing. Editorial changes throughout.	4 May 86	
C	Change to military drawing format. Add alternate group A programmability sample test. Update vendors part number. Make changes to screening and group A inspection.	2 June 1987	
D	Add device 02. Editorial changes throughout.	22 Jan. 1988	

REV																											
PAGE																											
REV STATUS OF PAGES	REV	D	D	C	D	D	D	D	C	C	C	C	D	D	C	C	D	D									
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17									

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing: 20 Feb. 1979

AMSC N/A

PREPARED BY: Rick C. Office

CHECKED BY: DA Di Cenzo

APPROVED BY:

SIZE: A

CODE IDENT. NO.: 14933

REV: D

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, 4K SCHOTTKY BIPOLAR PROM, MONOLITHIC SILICON

DWG NO. 78016

PAGE 1 OF 17

5962-E711

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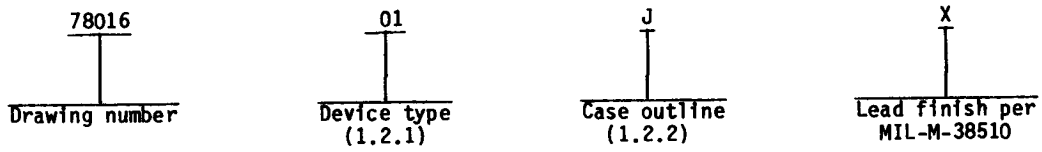
DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes the requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(see 6.4)	512X8-bit Schottky PROM	90
02	(see 6.4)	512X8-bit Schottky PROM	45

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 0.600" row spacing), dual-in-line package
K	F-6 (24-lead, 0.640" x 0.420" x 0.090", MAX), flat package
U	C-12 (32-terminal, 0.560" x 0.458" x 0.120", MAX), rectangular leadless chip carrier package
3	C-4 (28-terminal, 0.460" SQ. x 0.100", MAX), square leadless chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to 7.0 V dc
Input voltage range	-1.5 V dc to 5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.02 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}) 2/	(See MIL-M-38510, appendix C)
Maximum junction temperature (T_J)	+175°C
Output sink current	100 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc

1/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).
2/ Heat sinking is recommended to reduce the junction temperature.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -2 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	All	1,2,3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 8 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	All	1,2,3		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA	All	1,2,3		-1.2	V
High impedance (off-state) output high current	I_{OHZ}	V_{CC} = 5.5 V V_O = 5.2 V	All	1,2,3		100	µA
High impedance (off-state) output low current	I_{OLZ}	V_{CC} = 5.5 V V_O = 0.5 V	All	1,2,3		-100	µA
High level input current	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V	All	1,2,3		50	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.5 V	All	1,2,3	-1.0	-250	µA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V V_O = 0 V 1/	All	1,2,3	-10	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V V_{IN} = 0 V Outputs open	All	1,2,3		185	mA
Propagation delay time, address to output	t_{PHL1} t_{PLH1}	V_{CC} = 4.5 V and 5.5 V C_L = 30 pF	01 02	9,10,11		90 45	ns
Propagation delay time, enable to output	t_{PHL2} t_{PLH2}	V_{CC} = 4.5 V and 5.5 V C_L = 30 pF	01 02	9,10,11		50 25	ns

1/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

Device types 01 and 02

Cases J and K

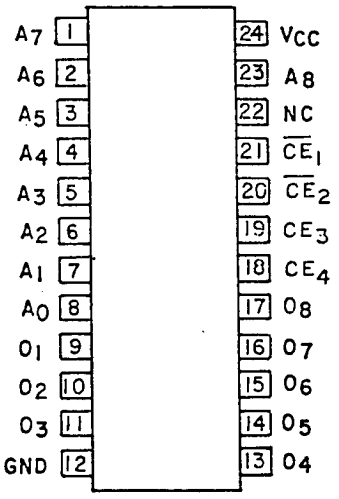


FIGURE 1. Terminal connections (top view).

Device types 01 and 02

Case U

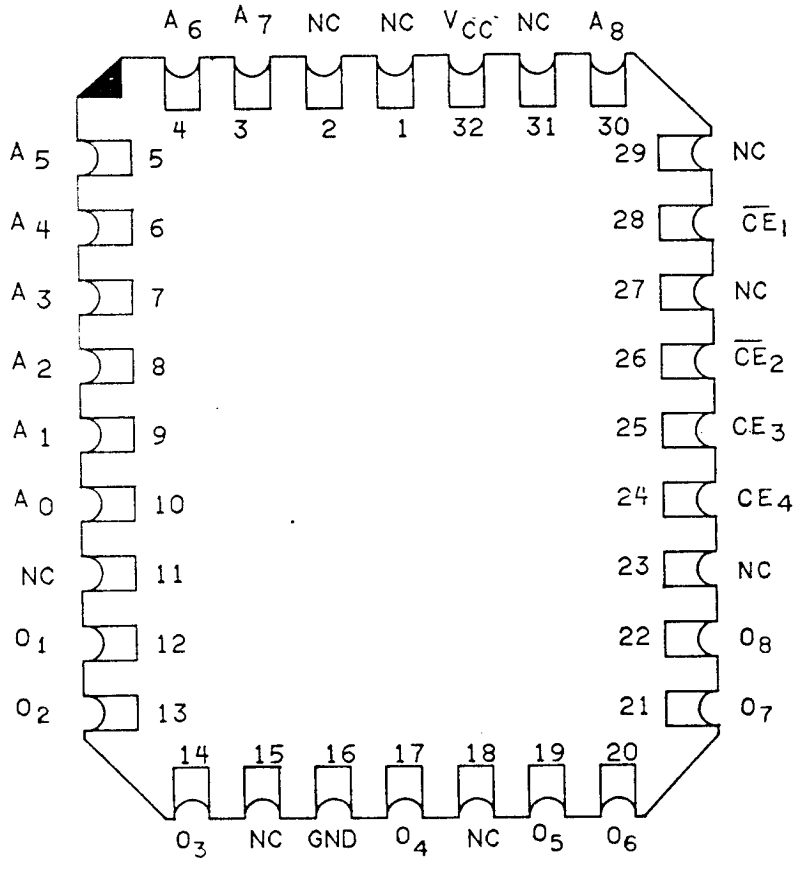


FIGURE 1. Terminal connections (top view) - Continued.

Device types 01 and 02

Case 3

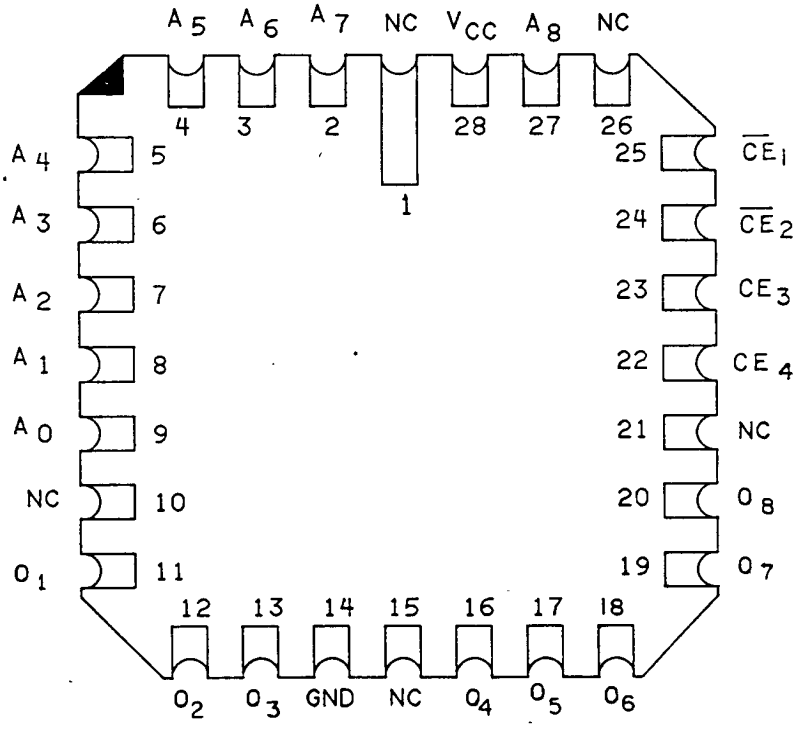


FIGURE 1. Terminal connections (top view) - Continued.

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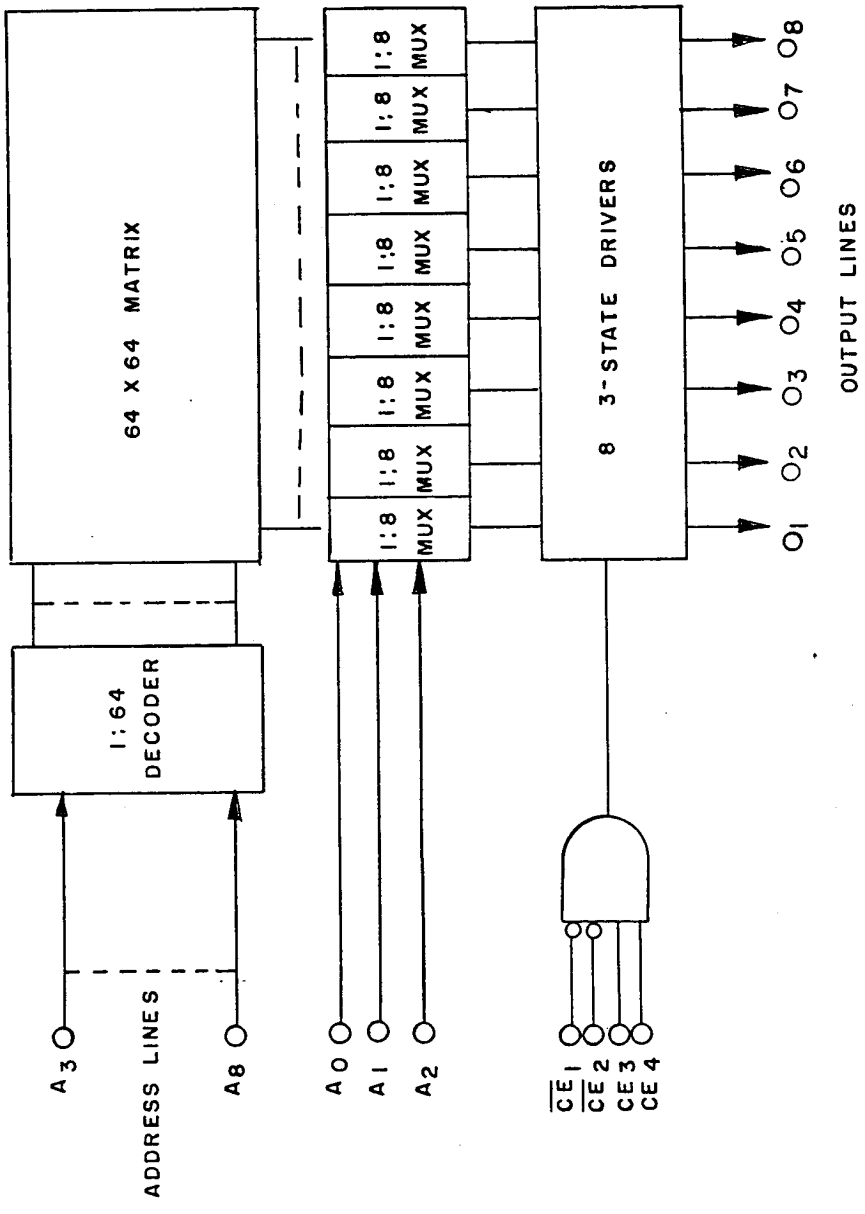
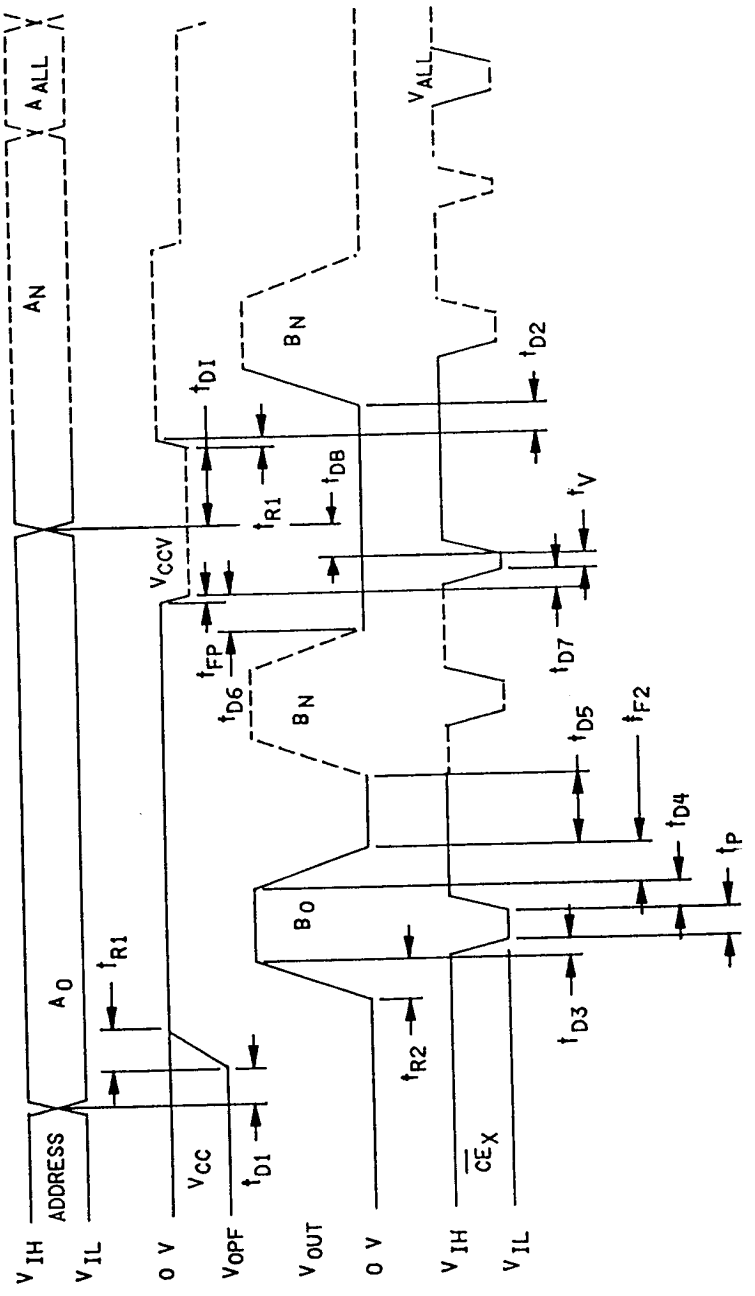
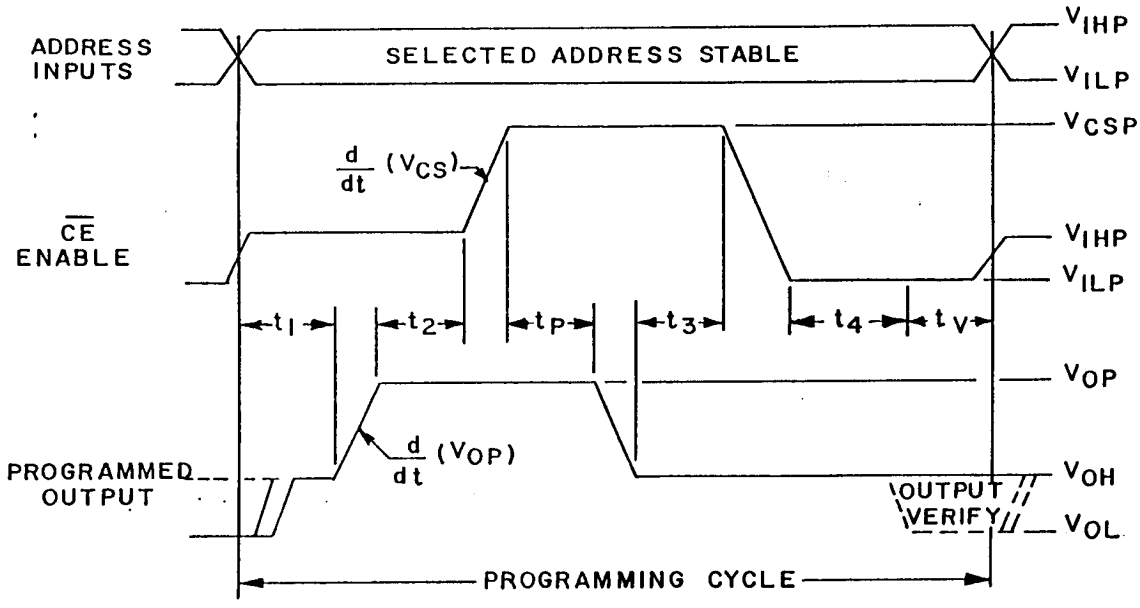


FIGURE 2. Logic diagram.



NOTE: All other waveform characteristics shall be as specified in table III.

FIGURE 3. Programming voltage waveforms during programming for circuit C.



NOTES:
1. All delays between edges are specified from completion of the first edge, not midpoints.
2. Delays t_1, t_2, t_3, and t_4 must be greater than 100 ns; maximum delays of 1 µs are recommended to minimize heating during programming.
3. During t_V the output being programmed is switched to the load R and verified.
4. Outputs not being programmed are connected to V_{ONP} through resistor which provides output current limiting.

FIGURE 4. Programming voltage waveforms during programming for circuit E.

3.9.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.9.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming. If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

d. Subgroups 7 and 8 must verify input to output logic combinations.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroups 1 and 7.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. The programmability sample (see 4.3.1c) shall be included in subgroup 1 tests.

4.4 Programming procedures for circuit C. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration for programming. The waveforms of figure 3 and the programming characteristics of table III shall apply to these procedures.

b. Terminate all device outputs with a 10 kΩ resistor to V_{CC}. Bypass V_{CC} to ground with a 0.01 µF capacitor. Apply $\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = \overline{CE}_X$, $\overline{CE}_3 = V_{IH}$ and $\overline{CE}_4 = V_{IH}$. Apply initial voltage of V_{IH} to $\overline{CE}_X$. Apply 0 volt to all other pins.

c. Select the word to be programmed by applying V_{IL} or V_{IH} on the appropriate address pins. After a T_{D1} delay, raise V_{CC} to V_{CCP}.

d. After a T_{D2} delay, raise the corresponding output pin to V_{OPF}.

e. After a T_{D3} delay, lower the programming control pin ($\overline{CE}_X$) to V_{IL} for a duration of t_p. Return the programming control pin ($\overline{CE}_X$) to V_{IH}.

f. After a T_{D4} delay, lower the output to 0 volt.

g. After a T_{D5} delay, repeat steps 4.4c through 4.4f for each output bit desired to be a logic one.

h. After a T_{D6} delay, apply V_{CCV} to V_{CC} pin.

i. After a T_{D7} delay, lower $\overline{CE}_X$ input to V_{IL} for a duration of T_V. A properly blown fuse will read V_{OH}, and an unblown fuse will read V_{OL}.

j. After a T_{D8} delay, select a new address.

k. After a T_{D1} delay, return V_{CC} to V_{CCP}.

l. Repeat steps 4.4c through 4.4k until all required addresses are programmed.

m. To verify programming, after a T_{D7} delay with V_{CC} at V_{CCV}, lower $\overline{CE}_X$ input to V_{IL}. Sequentially select all addresses in the memory. A properly blown fuse will read V_{OH}, and an unblown fuse will read V_{OL}.

n. If any bit does not verify as programmed, it shall be considered a programming reject.

4.5 Programming procedures for circuit E. The programming characteristics in table IV and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration for programming. The waveforms of figure 4 and the programming characteristics of table IV shall apply to these procedures.

b. Terminate all outputs with a 300Ω resistor to V_{ONP}. Apply V_{IHP} to the CE_3, and CE_4 inputs and V_{ILP} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs.

c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP}.

d. After a delay of t_1, apply only one V_{OP} pulse with a duration of t_p, t_2, and $d(V_{OP})/dt$ to the output selected for programming. After a delay of t_2 and $d(V_{OP})/dt$, pulse $\overline{CE}_1$ from V_{IHP} to V_{CEP} for the duration of t_p, $2d(V_{CE})/dt$, and t_3; $\overline{CE}_1$ is then to go to V_{ILP} level.

e. To verify programming after $\overline{CE}_1$ has been set to V_{ILP}, lower V_{CC} to V_{CCL} after a delay of t_4. The programmed output should remain in the logic '1' state.

f. The outputs should be programmed one output at a time, since the internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a low level logic output. Programming a fuse will cause the output to go to a high level logic in the verify mode.

g. Repeat steps 4.5b and 4.5f for all other bits to be programmed.

h. If any bit does not verify as programmed, it shall be considered a programming reject.

TABLE III. Programming characteristics for circuit C.

Parameter	Symbol	Conditions	Limits 1/			Unit
			Min	Recommended	Max	
Programming voltage to V_{CC}	V_{CCP} 1/	I_{CCP} = 425	8.5	8.75	9.0	V
Verify voltage	V_{CCV}		4.75	5.0	5.25	V
Forced output voltage (program)	V_{OPF} 2/ 3/	I_{OPF} = 300 µA	17.0	17.5	18.0	V
Output voltage, high level	V_{OH}		2.4		5.25	V
Output voltage, low level	V_{OL}		0		0.45	V
Input voltage, high level	V_{IH}	I_{IH} = 50 µA	2.4	3.0	5.5	V
Input voltage, low level	V_{IL}	I_{IL} = -500 µA	0	0	0.5	V
V_{CC} delay time	T_{D1}	50% Add to 10% V_{CCP}	10	10	25	µs
V_{OUT} delay time	T_{D2}	90% V_{CCP} to 10% V_{OPF}	1	1	5	µs
Pulse sequence delays	T_{D3}-T_{D8}	See figure 2	1	1	10	µs
$\overline{CE}$ verify pulse width	T_V 4/	10% to 10%	5	5	10	µs
$\overline{CE}$ programming pulse width	t_p 4/	10% to 10%	10	10	25	µs
V_{CC} rise time	T_{R1}	10% to 90%	2	7	20	µs
V_{OUT} rise time	T_{R2}	10% to 90%	17	20	35	µs
V_{CC} fall time	T_{F1}	90% to 10%	1	4	10	µs
V_{OUT} fall time	T_{F2}	90% to 10%	2	7	20	µs

1/ If the overall program/verify cycle exceeds the recommended times, a 25 percent duty cycle must be used for V_{CCP}.
2/ V_{OPF} supply should regulate to ±0.25 V at I_{OPF}.
3/ Maximum slew rate for V_{OPF} should be 1.0 V/µs.
4/ $\overline{CE}_X$ rise time slew rate should be 1.0 V/ns maximum. $\overline{CE}_X$ fall time slew rate should be 10.0 V/ns maximum.

TABLE IV. Programming characteristics for circuit E.

Parameter	Symbol	Conditions T_C = +25°C	Limits			Unit
			Min	Recommended	Max	
V_{CC} during programming	V_{CCP}		5.0		5.5	V
High level input voltage during programming	V_{IHP}		2.4		5.5	V
Low level input voltage during programming	V_{ILP}		0.0		0.45	V
Chip enable voltage during programming	V_{CEP}	$\overline{CE}_1$ pin	14.5		15.5	V
Output voltage during programming	V_{OP}		19.5		20.5	V
Voltage on outputs not to be programmed	V_{ONP}		0		V_{CCP} +0.3	V
Current on outputs not to be programmed	I_{ONP}				20	mA
Rate of output voltage change	$\frac{d(V_{OP})}{dt}$		20		250	V/µs
Rate of chip enable voltage change	$\frac{d(V_{CE})}{dt}$	$\overline{CE}_1$ pin	100		1,000	V/µs
Programming period	t_p		50		100	µs
V_{CC} during programming verification	V_{CCL}		4.5		5.0	µs

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/20802BXX.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, OH 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number	Programming method
7801601JX 2/	18324	82S141/BJA	M38510/20802BJX	C
	34335	AM27S31/BJA		E
7801601KX	18324	82S141/BKA	M38510/20802BKX	C
	34335	AM27S31/BKA		E
78016013X	34335	AM27S31/B3A		E
7801601UX	34335	AM27S31/BUA		E
7801602JX	34335	AM27S31A/BJA		E
7801602KX	34335	AM27S31A/BKA		E
78016023X	34335	AM27S31A/B3A		E
7801602UX	34335	AM27S31A/BUA		E

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not recommended for new design. Use M38510/20802BJX.

Vendor CAGE number	Vendor name and address
18324	Signetics Corporation 4130 S. Market Court Sacramento, CA 95834
34335	Advanced Micro Devices, Inc. 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088