Device Overview

The IDT70K2000 is a serial RapidIO^{TM} Pre-Processing Switch (PPS). The PPS is central to the "DSP Farms" processing architecture. It may also be used in serial RapidIO backplane switching. The PPS performs a variety of data processing on the payload of sample packets to accelerate the subsequent algorithmic operations of a receiving processor (DSP, CRP, FPGA). It supports serial RapidIO^{TM} packet switching (unicast, multicast, or broadcast) from any input to any output port. The PPS accelerates baseband processing in support of a variety of wireless standards. It may also be used for video imaging such as that in medical equipment, high-end surveillance, or similar signal processing-intensive applications.

Features

- ◆ **Interfaces - sRIO**
  - – *40 bidirectional serial RapidIO (sRIO) lanes v 1.3*
  - – *Port Speeds selectable; 3.125Gbps, 2.5Gbps, or 1.25Gbps*
  - – *Short haul or long haul reach for each PHY speed*
  - – *Configurable in up to 22 ports (1x and 4x link implementations)*
  - – *Error management supports standard and enhanced port operations*
- ◆ **Interfaces - I²C**
  - – *One I^{2}C port for maintenance and error reporting*
- ◆ **Switch**
  - – *10Gbps peak throughput*
- ◆ **Packet Processor**
  - – *100Gbps peak throughput*
  - – *10 Individual Packet Processing Scenarios (PPSc), each capable of:*

Within Sample Processing
- – Sign Extension/Deletion, Endian Change
- – Programmable number of bits per sample 2B; 4<=B<=32 bits
- – Sample Format; I/Q format or I only

Within Packet Processing
- – Any sample can be extracted from any 256 locations of any of 22 incoming sample packets
- – The chosen sample can be placed into any location of the resultant packet (up to 256 locations)
- – Up to 22 samples can be summed to give one sample ouput, which is placed in any location of resultant packet
- – Multiple packets can be generated from a single PPSc going to a single port
- – Up to 8 packets can be created by a single PPSc
- – Each packet can be assigned a specific 32-bit memory address (in sRIO header)
- – Multiple packets from a group of input sample packets can be generated by concurrently using multiple PPSc
- – SWRITE packets formed for Packet Processor Output Packets
- – Incoming packet header information will be used in the resultant packet

Summation of up to 22 packets
- – 37 bit summing of each I or Q sub-sample
- – Dynamic Range or saturation of Result to 4-32 bit range
- – 8 Group Scenarios each of which can address up to 4 Individual PPSc
- ◆ **Synchronization**
  - – *Non-TDM sychronization of packets from multiple ports*
- ◆ **Package: 676-ball grid array, 27mm x 27mm, 1.0mm ball pitch**

Block Diagram
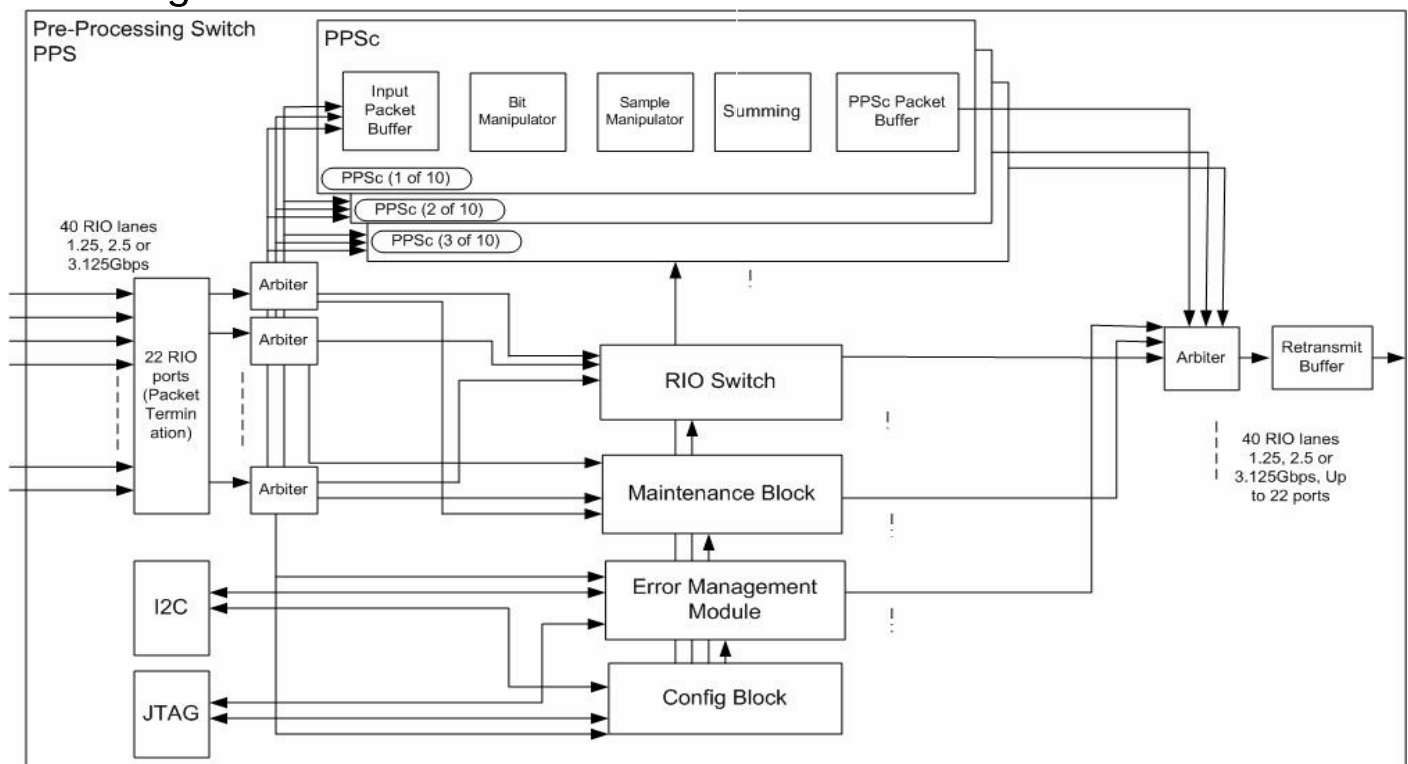
Functional Description

The Pre-Processing Switch (PPS) from IDT is optimized for DSP cluster applications at board level. Its main function is to have a backplane interface which can connect to a backplane switch or directly to multiple RF cards. On the line card side it can also connect to multiple ports. It supports up to 22 ports which are configurable as line card, or backplane ports. It is an end-point free (switch) device in an sRIO network.

If packets are addressed to a certain port or a range of addresses, the unprocessed data samples in their payload will be preprocessed to make them more "DSP-friendly". If not, the packets are switched as defined by the transport layer sRIO specification. The packet manipulation in the PPS is transparent to the sRIO protocol.

The PPS receives the packets from a total of 22 ports. Depending on the device ID field within a received packet, two functions can be performed by the PPS:

1) **Packet Processing**: If DestID in the sRIO transport layer is one of the Packet Processing Scenario (PPSc) addresses specified in the PPSc registers, the PPS terminates the sRIO packet and implements the sample preprocessing.

   The sample preprocessing operations are defined in Packet Processing Scenarios (PPSc). There are a total of 10 individual PPScs in the PPS. There are also 8 Group PPScs (GPPSc), each of which may be linked to 4 individual PPScs.

2) **Switching**: All other addresses are treated as regular sRIO destination addresses, and packets are switched accordingly.

Also three major options exist within this category:

    a.   Multicast:If a Multicast ID is received, the PPS performs a multicast as defined in the sRIO multicast registers.

    b.   Unicast: All other operations are performed as specified in sRIO.

    c.   Maintenance packets: As specified in sRIO.

The PPS can be programmed through a CPU or a DSP connected to one of the sRIO ports of the device or with a CPU connected to an I^2C or JTAG bus. This option is added to allow the user to use a conventional CPU instead of a sRIO interface.

The packets received from packet processing or switching are sent to re-transmit buffers, which are 8 maximum sized packets deep. 4 levels of priority can be assigned in sRIO packets for both sample packets and standard packets to adjust the transmission priority.

The packets are switched depending on the priority. The switched packet priority then is compared to sample packet priority, and the highest priority goes into the re-transmit buffer first. Once in the re-transmit buffer, the priorities do not affect the place in the buffer.

The Packet Processing Module can reach a peak throughput of 100Gbps, which is the line rate for 10 ports in 4x configuration, each at 3.125Gbps. It is programmed via the PPSc registers. Re-programming each PPSc dynamically is possible, and does not affect the operation of all other PPScs, but does incur a pause on the affected PPSc.

The sRIO Switch can sustain a peak throughput of 10Gbps, and switches dynamically in accordance with the packet headers.

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Pre-Processing Switch in Support of Baseband Processing Board, Cellular Base Station
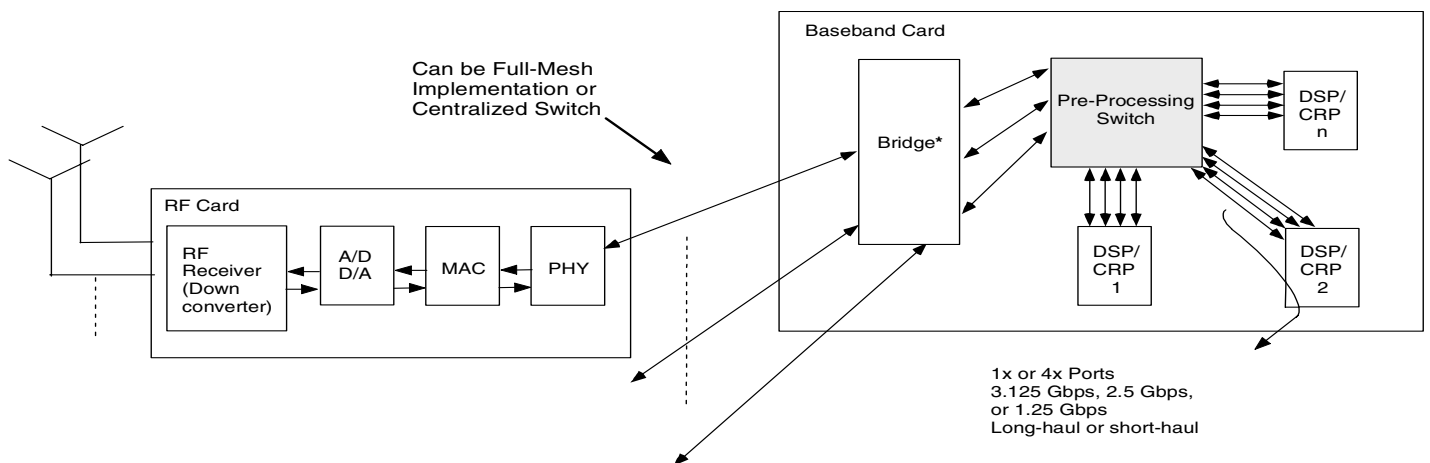
Figure 1 Interface Overview

   *The IDT70K2000 provides direct support for backplane connections using the serial RapidIO standard. The addition of an appropriate bridge allows for further backplane flexibility, accommodating designs based on a wide range of standards such as CPRI, OBSAI, GbE, PCIe, or ASI.