



# 4-Channel, 12-/10-Bit ADCs with I<sup>2</sup>C Compatible Interface in 16-Lead TSSOP

## Preliminary Technical Data

## AD7994/AD7993

### FEATURES

**12-Bit ADC with Fast Conversion Time: 2  $\mu$ s**  
**Four Single-Ended Analog Input Channels**  
**Specified for  $V_{DD}$  of 2.7 V to 5.5 V**  
**Low Power Consumption**  
**Fast Throughput Rate:- 188 KSPS**  
**Sequencer Operation**  
**Automatic Cycle Mode**  
**I<sup>2</sup>C<sup>R</sup> Compatible Serial Interface**  
**I<sup>2</sup>C<sup>R</sup> Interface supports:**  
**Standard, Fast, and High-Speed Modes**  
**Out of Range Indicator/Alert Function**  
**Pin-Selectable Addressing via AS**  
**Two Versions Allow Five I<sup>2</sup>C Addresses**  
**Shutdown Mode: 1 $\mu$ A max**  
**16-Lead TSSOP Package**

### GENERAL DESCRIPTION

The AD7994/AD7993 are 4 channel, 12-/10-bit, high speed, low power, successive-approximation ADCs respectively. They operate from a single 2.7 V to 5.5 V power supply and feature a conversion time of 2  $\mu$ s. The parts contain a four channel multiplexer and track/hold amplifier which can handle input frequencies in excess of TBD kHz.

The AD7994/AD7993 provide a two-wire serial interface which is compatible with I<sup>2</sup>C interfaces. The parts come in two versions, AD7994-0/AD7993-0 to AD7994-1/AD7993-1. Each version allows for a minimum of two different I<sup>2</sup>C addresses. The I<sup>2</sup>C interface on the AD7994-0/AD7993-0 supports Standard and Fast I<sup>2</sup>C Interface Modes. The I<sup>2</sup>C interface on the AD7994-1/AD7993-1 supports Standard, Fast and two High-Speed I<sup>2</sup>C Interface Modes.

The AD7994/AD7993 normally remain in a shutdown state while not converting, powering up only for conversions. The conversion process can be controlled using the CONVST pin, an Automatic Conversion Cycle selected through software control, or a mode where conversions occur across Write operations. There are no pipeline delays associated with the part.

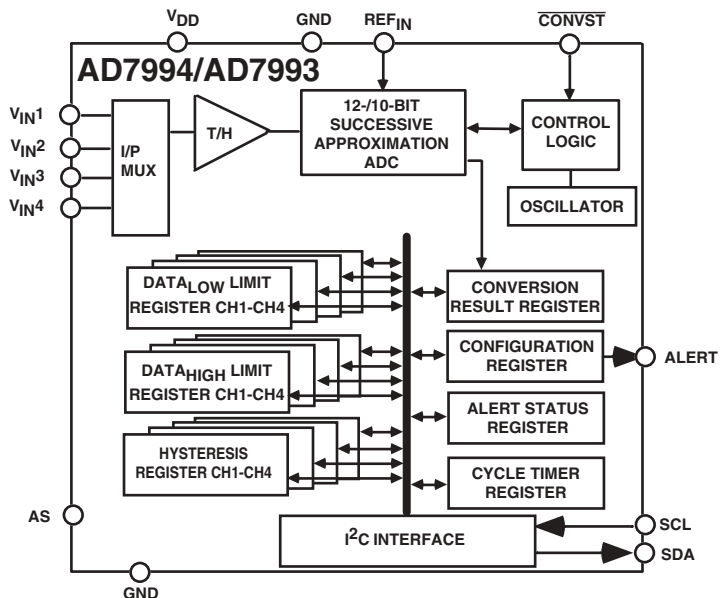
The reference for the part is applied externally to the REF<sub>IN</sub> pin and can be in the range of 1.2V to  $V_{DD}$ . This allows the widest dynamic input range to the ADC.

SMBus is a trademark and I<sup>2</sup>C is a registered trademark of Philips Corporation

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### FUNCTIONAL BLOCK DIAGRAM



On-chip registers can be programmed with high and low limits for the conversion result, and an open drain Out of Range Indicator output (ALERT), becomes active when the programmed high or low limits are violated by the conversion result. This output can be used as an interrupt.

### PRODUCT HIGHLIGHTS

- 2  $\mu$ s Conversion time with low power consumption.
- I<sup>2</sup>C Compatible Serial Interface with pin selectable addresses. Two AD7994/AD7993 versions allow five AD7994/AD7993 devices to be connected to the same serial bus.
- The parts feature automatic shutdown while not converting to maximize power efficiency. Current consumption is 1 $\mu$ A max when in shutdown.
- Reference can be driven up to the power supply.
- Out of Range Indicator which can be software disabled/enabled.
- Oneshot and automatic conversion rates.
- No Pipeline Delay  
The part features a standard successive-approximation ADC.

PRELIMINARY TECHNICAL DATA

**AD7994—SPECIFICATIONS<sup>1</sup>** ( $V_{DD} = +2.7\text{ V to }+5.5\text{ V}$ , unless otherwise noted ;  $REF_{IN} = 2.5\text{ V}$ ;  $f_{SCL} = 3.4\text{ MHz}$  unless otherwise noted;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

Parameter	B Version <sup>1</sup>	Units	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE</b>			
Signal to Noise + Distortion (SINAD) <sup>2</sup>	70	dB min	$F_{IN} = 10\text{kHz}$ Sine Wave
Signal to Noise Ratio (SNR) <sup>2</sup>	71	dB min	
Total Harmonic Distortion (THD) <sup>2</sup>	-78	dB typ	
Peak Harmonic or Spurious Noise (SFDR) <sup>2</sup>	-80	dB typ	
Intermodulation Distortion (IMD) <sup>2</sup>			$f_a = \text{TBD kHz}$ , $f_b = \text{TBD kHz}$
Second Order Terms	-78	dB typ	
Third Order Terms	-78	dB typ	
Aperture Delay	10	ns max	
Aperture Jitter	10	ps typ	
Channel-to-Channel Isolation	TBD	dB typ	$F_{IN} = \text{TBD kHz}$
Full Power Bandwidth	TBD	kHz typ	@ 3 dB
	TBD	kHz typ	@ 0.1 dB
<b>DC ACCURACY</b>			
Resolution	12	Bits	
Integral Nonlinearity <sup>2</sup>	$\pm 1$	LSB max	
	$\pm 0.6$	LSB typ	
Differential Nonlinearity <sup>2</sup>	+1.5/-0.9	LSB max	Guaranteed No Missed Codes to 12 Bits.
	$\pm 0.75$	LSB typ	
Offset Error <sup>2</sup>	$\pm 1.5$	LSB max	
Offset Error Match <sup>2</sup>	$\pm 0.5$	LSB max	
Gain Error <sup>2</sup>	$\pm 1.5$	LSB max	
Gain Error Match <sup>2</sup>	$\pm 0.5$	LSB max	
<b>ANALOG INPUT</b>			
Input Voltage Ranges	0 to $REF_{IN}$	Volts	
DC Leakage Current	$\pm 1$	$\mu\text{A}$ max	
Input Capacitance	30	pF typ	
<b>REFERENCE INPUT</b>			
$REF_{IN}$ Input Voltage Range	1.2 to $V_{DD}$	V min/Vmax	
DC Leakage Current	$\pm 1$	$\mu\text{A}$ max	
Input Capacitance	TBD	pF max	
Input Impedance	TBD	k $\Omega$ typ	
<b>LOGIC INPUTS (SDA, SCL)</b>			
Input High Voltage, $V_{INH}$	0.7( $V_{DD}$ )	V min	
Input Low Voltage, $V_{INL}$	0.3( $V_{DD}$ )	V max	
Input Leakage Current, $I_{IN}$	$\pm 1$	$\mu\text{A}$ max	$V_{IN} = 0\text{ V or }V_{DD}$
Input Capacitance, $C_{IN}^{2,3}$	10	pF max	
Input Hysteresis, $V_{HYST}$	TBD	V min	
<b>LOGIC INPUT (<math>\overline{CONVST}</math>)</b>			
Input High Voltage, $V_{INH}$	2.4	V min	$V_{DD} = 5\text{V}$
	2.0	V min	$V_{DD} = 3\text{V}$
Input Low Voltage, $V_{INL}$	0.8	V max	$V_{DD} = 5\text{V}$
	0.4	V max	$V_{DD} = 3\text{V}$
Input Leakage Current, $I_{IN}$	$\pm 1$	$\mu\text{A}$ max	$V_{IN} = 0\text{ V or }V_{DD}$
Input Capacitance, $C_{IN}^{2,3}$	10	pF max	
<b>LOGIC OUTPUTS (OPEN DRAIN)</b>			
Output Low Voltage, $V_{OL}$	0.4	V max	$I_{SINK} = 3\text{mA}$
	0.6	V max	$I_{SINK} = 6\text{mA}$
Floating-State Leakage Current	$\pm 1$	$\mu\text{A}$ max	
Floating-State Output Capacitance <sup>2,3</sup>	TBD	pF max	
Output Coding	Straight (Natural) Binary		

# AD7994—SPECIFICATIONS<sup>1</sup>

( $V_{DD} = +2.7\text{ V}$  to  $+5.5\text{ V}$ , unless otherwise noted ;  $REF_{IN} = 2.5\text{ V}$ ;  $f_{SCL} = 3.4\text{ MHz}$  unless otherwise noted;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

Parameter	B Version <sup>1</sup>	Units	Test Conditions/Comments
<b>CONVERSION RATE</b>			
Conversion Time	2	$\mu\text{s}$ typ	See Interface Section
Track/Hold Acquisition Time	TBD	ns max	Full-Scale step input
	TBD	ns max	Sine wave input $\leq 30\text{ KHz}$
Throughput Rate	3.4	KSPS max	Standard mode SCL = 100 kHz
	13	KSPS max	Fast Mode SCL = 400 kHz
	79	KSPS max	High-Speed Mode SCL = 3.4 MHz
<b>POWER REQUIREMENTS</b>			
$V_{DD}$	2.7/5.5 V	min/max	Digital Inputs = 0 V or $V_{DD}$
$I_{DD}$			Peak Current during conversion
Peak Current	TBD	$\mu\text{A}$ max	$V_{DD} = 3\text{ V}/5\text{ V}$ .
Power Down Mode , Interface Inactive	0.2/0.6	$\mu\text{A}$ max	$V_{DD} = 3\text{ V}/5\text{ V}$ 400 kHz SCL.
	0.05/0.2	mA max	$V_{DD} = 3\text{ V}/5\text{ V}$ 3.4 MHz SCL.
Interface Active	0.3/0.8	mA max	
Operating, Interface Inactive	0.06/0.15	mA max	$V_{DD} = 3\text{ V}/5\text{ V}$ 400 kHz SCL.
	0.3/0.6	mA max	$V_{DD} = 3\text{ V}/5\text{ V}$ 3.4 MHz SCL.
Interface Active	0.15/0.35	mA max	$V_{DD} = 3\text{ V}/5\text{ V}$ 400 kHz SCL.
	0.6/1.4	mA max	$V_{DD} = 3\text{ V}/5\text{ V}$ 3.4 MHz SCL.

## NOTES

<sup>1</sup>Temperature ranges as follows: B Version:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

<sup>2</sup>See Terminology.

<sup>3</sup>Sample tested @  $+25^{\circ}\text{C}$  to ensure compliance.

<sup>4</sup>See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

**AD7993—SPECIFICATIONS<sup>1</sup>**

( $V_{DD} = +2.7\text{ V to }+5.5\text{ V}$ , unless otherwise noted ;  $REF_{IN} = 2.5\text{ V}$ ;  $f_{SCL} = 3.4\text{ MHz}$  unless otherwise noted;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

Parameter	B Version <sup>1</sup>	Units	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE</b>			
Signal to Noise + Distortion (SINAD) <sup>2</sup>	61	dB min	$F_{IN} = 10\text{kHz Sine Wave}$
Signal to Noise Ratio (SNR) <sup>2</sup>	TBD	dB min	
Total Harmonic Distortion (THD) <sup>2</sup>	-73	dB typ	
Peak Harmonic or Spurious Noise (SFDR) <sup>2</sup>	-74	dB typ	
Intermodulation Distortion (IMD) <sup>2</sup>			$f_a = \text{TBD kHz}, f_b = \text{TBD kHz}$
Second Order Terms	-78	dB typ	
Third Order Terms	-78	dB typ	
Aperture Delay	10	ns max	
Aperture Jitter	10	ps typ	
Channel-to-Channel Isolation	TBD	dB typ	$F_{IN} = \text{TBD kHz}$
Full Power Bandwidth	TBD	kHz typ	@ 3 dB
	TBD	kHz typ	@ 0.1 dB
<b>DC ACCURACY</b>			
Resolution	10	Bits	
Integral Nonlinearity <sup>2</sup>	$\pm 1$	LSB max	
	$\pm 0.6$	LSB typ	
Differential Nonlinearity <sup>2</sup>	$\pm 0.9$	LSB max	Guaranteed No Missed Codes to 10 Bits.
Offset Error <sup>2</sup>	$\pm 1$	LSB max	
Offset Error Match <sup>2</sup>	$\pm 0.5$	LSB max	
Gain Error <sup>2</sup>	$\pm 1$	LSB max	
Gain Error Match <sup>2</sup>	$\pm 0.5$	LSB max	
Total Unadjusted Error (TUE) <sup>2</sup>	$\pm 1$	LSB max	
<b>ANALOG INPUT</b>			
Input Voltage Ranges	0 to $REF_{IN}$	Volts	
DC Leakage Current	$\pm 1$	$\mu\text{A max}$	
Input Capacitance	30	pF typ	
<b>REFERENCE INPUT</b>			
$REF_{IN}$ Input Voltage Range	TBD/TBD	V min/Vmax	
DC Leakage Current	$\pm 1$	$\mu\text{A max}$	
Input Capacitance	TBD	pF max	
Input Impedance	TBD	k $\Omega$ typ	
<b>LOGIC INPUTS (SDA, SCL, <math>\overline{CONVST}</math>)</b>			
Input High Voltage, $V_{INH}$	0.7( $V_{DD}$ )	V min	
Input Low Voltage, $V_{INL}$	0.3( $V_{DD}$ )	V max	
Input Leakage Current, $I_{IN}$	$\pm 1$	$\mu\text{A max}$	$V_{IN} = 0\text{ V or }V_{DD}$
Input Capacitance, $C_{IN}^{2,3}$	10	pF max	
Input Hysteresis, $V_{HYST}$	TBD	V min	
<b>LOGIC INPUT (<math>\overline{CONVST}</math>)</b>			
Input High Voltage, $V_{INH}$	2.4	V min	$V_{DD} = 5\text{V}$
	2.0	V min	$V_{DD} = 3\text{V}$
Input Low Voltage, $V_{INL}$	0.8	V max	$V_{DD} = 5\text{V}$
	0.4	V max	$V_{DD} = 3\text{V}$
Input Leakage Current, $I_{IN}$	$\pm 1$	$\mu\text{A max}$	$V_{IN} = 0\text{ V or }V_{DD}$
Input Capacitance, $C_{IN}^{2,3}$	10	pF max	
<b>LOGIC OUTPUTS (OPEN DRAIN)</b>			
Output Low Voltage, $V_{OL}$	0.4	V max	$I_{SINK} = 3\text{mA}$
	0.6	V max	$I_{SINK} = 6\text{mA}$
Floating-State Leakage Current	$\pm 1$	$\mu\text{A max}$	
Floating-State Output Capacitance <sup>2,3</sup>	TBD	pF max	
Output Coding	Straight (Natural) Binary		

# AD7993—SPECIFICATIONS<sup>1</sup> ( $V_{DD} = +2.7\text{ V to }+5.5\text{ V}$ , unless otherwise noted ; $REF_{IN} = 2.5\text{ V}$ ; $f_{SCL} = 3.4\text{ MHz}$ unless otherwise noted; $T_A = T_{MIN}$ to $T_{MAX}$ , unless otherwise noted.)

Parameter	B Version <sup>1</sup>	Units	Test Conditions/Comments
<b>CONVERSION RATE</b>			See Interface Section
Conversion Time	2	$\mu\text{s typ}$	
Track/Hold Acquisition Time	TBD	ns max	Full-Scale step input
	TBD	ns max	Sine wave input $\leq 30\text{ KHz}$
Throughput Rate	3.4	KSPS max	Standard mode 100 kHz
	13	KSPS max	Fast Mode 400 kHz
	79	KSPS max	High-Speed Mode 3.4 MHz
<b>POWER REQUIREMENTS</b>			
$V_{DD}$	2.7/5.5 V	min/max	Digital Inputs = 0 V or $V_{DD}$
$I_{DD}$			Peak Current during conversion
Peak Current	TBD	mA max	$V_{DD} = 3\text{ V/5 V}$ .
Power Down Mode , Interface Inactive	0.2/0.6	$\mu\text{A max}$	$V_{DD} = 3\text{ V/5 V } 400\text{ kHz SCL}$ .
Interface Active	0.05/0.2	mA max	$V_{DD} = 3\text{ V/5 V } 3.4\text{ MHz SCL}$ .
	0.3/0.8	mA max	
Operating, Interface Inactive	0.06/0.15	mA max	$V_{DD} = 3\text{ V/5 V } 400\text{ kHz SCL}$ .
	0.3/0.6	mA max	$V_{DD} = 3\text{ V/5 V } 3.4\text{ MHz SCL}$ .
Interface Active	0.15/0.35	mA max	$V_{DD} = 3\text{ V/5 V } 400\text{ kHz SCL}$ .
	0.6/1.4	mA max	$V_{DD} = 3\text{ V/5 V } 3.4\text{ MHz SCL}$ .

**NOTES**

<sup>1</sup>Temperature ranges as follows: B Version:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

<sup>2</sup>See Terminology.

<sup>3</sup>Sample tested @  $+25^{\circ}\text{C}$  to ensure compliance.

<sup>4</sup>See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

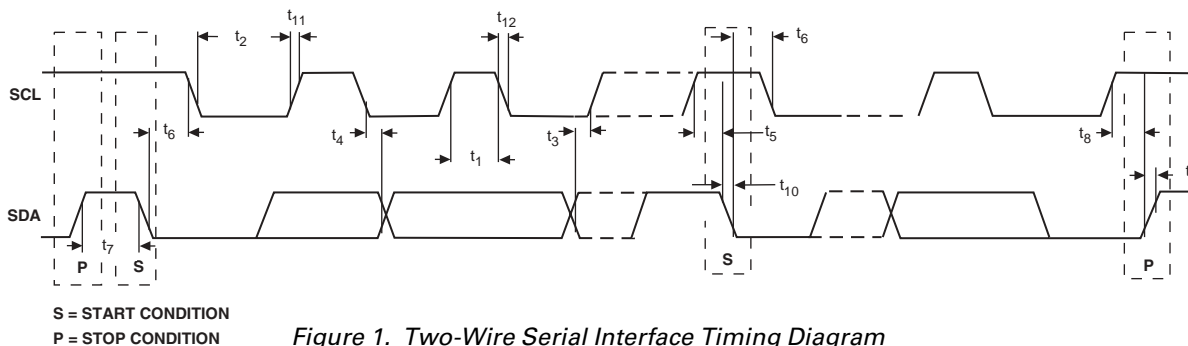


Figure 1. Two-Wire Serial Interface Timing Diagram

## I<sup>2</sup>C TIMING SPECIFICATIONS<sup>1</sup> ( $V_{DD} = +2.7\text{ V to }+5.5\text{ V}$ , unless otherwise noted ; $REF_{IN} = 2.5\text{ V}$ ; unless otherwise noted; $T_A = T_{MIN}$ to $T_{MAX}$ , unless otherwise noted..)

Parameter	Conditions	AD7994/AD7993		Unit	Description
		Limit at $T_{MIN}$ , MIN	$T_{MAX}$ MAX		
$f_{SCL}$ <sup>2</sup>	Standard Mode		100	kHz	Serial Clock Frequency
	Fast Mode		400	kHz	
	High-Speed Mode, $C_B = 100\text{pF max}$		3.4	MHz	
	High-Speed Mode, $C_B = 400\text{pF max}$		1.7	MHz	
$t_1$	Standard Mode	4		$\mu\text{s}$	$t_{HIGH}$ , SCL High Time
	Fast Mode	0.6		$\mu\text{s}$	
	High-Speed Mode, $C_B = 100\text{pF max}$	60		ns	
	High-Speed Mode, $C_B = 400\text{pF max}$	120		ns	
$t_2$	Standard Mode	4.7		$\mu\text{s}$	$t_{LOW}$ , SCL Low Time
	Fast Mode	1.3		$\mu\text{s}$	
	High-Speed Mode, $C_B = 100\text{pF max}$	160		ns	
	High-Speed Mode, $C_B = 400\text{pF max}$	320		ns	
$t_3$	Standard Mode	250	-	ns	$t_{SU;DAT}$ , Data Setup Time
	Fast Mode	100	-	ns	
	High-Speed Mode	10	-	ns	

# PRELIMINARY TECHNICAL DATA

## AD7994/AD7993

### I<sup>2</sup>C TIMING SPECIFICATIONS<sup>1</sup> (Continued.)

Parameter	Conditions	AD7994/AD7993 Limit at T <sub>MIN</sub> , T <sub>MAX</sub>		Unit	Description
		MIN	MAX		
t <sub>4</sub>	Standard Mode	0	3.45	μs	t <sub>HD;DAT</sub> , Data Hold Time
	Fast Mode	0	0.9	μs	
	High-Speed Mode, C <sub>B</sub> = 100pF max	0	70	ns	
	High-Speed Mode, C <sub>B</sub> = 400pF max	0	150	ns	
t <sub>5</sub>	Standard Mode	4.7		μs	t <sub>SU;STA</sub> , Set-up Time for a repeated START Condition
	Fast Mode	0.6		μs	
	High-Speed Mode	160		ns	
t <sub>6</sub>	Standard Mode	4		μs	t <sub>HD;STA</sub> , Hold Time (repeated) START Condition
	Fast Mode	0.6		μs	
	High-Speed Mode	160		ns	
t <sub>7</sub>	Standard Mode	4.7		μs	t <sub>BUF</sub> , Bus Free Time Between a STOP and a START Condition.
	Fast Mode	1.3		μs	
t <sub>8</sub>	Standard Mode	4		μs	t <sub>SU;STO</sub> , Set-up Time for STOP Condition
	Fast Mode	0.6		μs	
	High-Speed Mode	160		ns	
t <sub>9</sub>	Standard Mode	-	1000	ns	t <sub>RDA</sub> , Rise time of SDA signal
	Fast Mode	20 + 0.1C <sub>B</sub>	300	ns	
	High-Speed Mode, C <sub>B</sub> = 100pF max	10	80	ns	
	High-Speed Mode, C <sub>B</sub> = 400pF max	20	160	ns	
t <sub>10</sub>	Standard Mode	-	300	ns	t <sub>FDA</sub> , Fall time of SDA signal
	Fast Mode	20 + 0.1C <sub>B</sub>	300	ns	
	High-Speed Mode, C <sub>B</sub> = 100pF max	10	80	ns	
	High-Speed Mode, C <sub>B</sub> = 400pF max	20	160	ns	
t <sub>11</sub>	Standard Mode	-	1000	ns	t <sub>RCL</sub> , Rise time of SCL signal
	Fast Mode	20 + 0.1C <sub>B</sub>	300	ns	
	High-Speed Mode, C <sub>B</sub> = 100pF max	10	40	ns	
	High-Speed Mode, C <sub>B</sub> = 400pF max	20	80	ns	
t <sub>11A</sub>	Standard Mode	-	1000	ns	t <sub>RCL1</sub> , Rise time of SCL signal after a repeated START Condition and after an Acknowledge bit.
	Fast Mode	20 + 0.1C <sub>B</sub>	300	ns	
	High-Speed Mode, C <sub>B</sub> = 100pF max	10	80	ns	
	High-Speed Mode, C <sub>B</sub> = 400pF max	20	160	ns	
t <sub>12</sub>	Standard Mode	-	300	ns	t <sub>FCL</sub> , Fall Time of SCL signal
	Fast Mode	20 + 0.1C <sub>B</sub>	300	ns	
	High-Speed Mode, C <sub>B</sub> = 100pF max	10	40	ns	
	High-Speed Mode, C <sub>B</sub> = 400pF max	20	80	ns	
t <sub>SP</sub> <sup>4</sup>	Fast Mode	0	50	ns	Pulsewidth of Spike Suppressed.
	High-Speed Mode	0	10	ns	
t <sub>POWER-UP</sub>			1	μs	Power-up Time

#### NOTES

<sup>1</sup>See Figure 1. C<sub>B</sub> refers to the capacitance load on the bus line. Hs-Mode timing specifications apply to the AD7994-1/AD7993-1 only. Standard and Fast Mode timing specifications apply to both the AD7994-0/AD7993-0 and the AD7994-1/AD7993-1.

<sup>2</sup>The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.

<sup>4</sup>Input filtering on both the SCL and SDA inputs suppress noise spikes that are less than 50ns or 10ns for Fast Mode or High-Speed mode respectively.

Specifications subject to change without notice.

# PRELIMINARY TECHNICAL DATA

## AD7994/AD7993

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to GND	-0.3 V to 7 V
Analog Input Voltage to GND	-0.3 V to V <sub>DD</sub> + 0.3 V
Reference Input Voltage to GND	-0.3 V to V <sub>DD</sub> + 0.3 V
Digital Input Voltage to GND	-0.3 V to 7 V
Digital Output Voltage to GND	-0.3 V to V <sub>DD</sub> + 0.3 V
Input Current to Any Pin Except Supplies <sup>2</sup>	±10 mA
Operating Temperature Range	
Commercial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

Junction Temperature	+150°C
16-ld TSSOP Package	
θ <sub>JA</sub> Thermal Impedance	150.4°C/W (TSSOP)
θ <sub>JC</sub> Thermal Impedance	27.6°C/W (TSSOP)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infrared (15 secs)	+220°C

### NOTES

<sup>1</sup>Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Transient currents of up to 100 mA will not cause SCR latch up.

### ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Linearity Error <sup>2</sup> (max)	Package Option <sup>3</sup>
AD7994BRU-0	-40°C to +85°C	±1 LSB	RU-16
AD7994BRU-1	-40°C to +85°C	±1 LSB	RU-16
AD7993BRU-0	-40°C to +85°C	±1 LSB	RU-16
AD7993BRU-1	-40°C to +85°C	±1 LSB	RU-16

### NOTES

<sup>1</sup> The AD7994-0/AD7993-0 supports Standard and Fast I<sup>2</sup>C interface modes. The AD7994-1/AD7993-1 supports Standard, Fast and Highspeed I<sup>2</sup>C Interface Modes.

<sup>2</sup>Linearity error here refers to Integral Nonlinearity

<sup>3</sup>RU = TSSOP.

### CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7994/AD7993 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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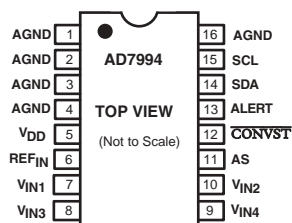
# PRELIMINARY TECHNICAL DATA

## AD7994/AD7993

### PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
AGND	Analog Ground. Ground reference point for all circuitry on the AD7994/AD7993. All analog input signals should be referred to this GND voltage.
V <sub>DD</sub>	Power Supply Input. The V <sub>DD</sub> range for the AD7994/AD7993 is from +2.7V to +5.5V.
REF <sub>IN</sub>	Voltage Reference Input. The External Reference for the AD7994/AD7993 should 0.1 μF capacitor should be placed between the REF <sub>IN</sub> pin and AGND.
V <sub>IN1</sub>	Analog Input 1. Single-ended analog input channel. The input range is 0V to REF <sub>IN</sub> .
V <sub>IN3</sub>	Analog Input 3. Single-ended analog input channel. The input range is 0V to REF <sub>IN</sub> .
V <sub>IN4</sub>	Analog Input 4. Single-ended analog input channel. The input range is 0V to REF <sub>IN</sub> .
V <sub>IN2</sub>	Analog Input 2. Single-ended analog input channel. The input range is 0V to REF <sub>IN</sub> .
AS	Logic Input. Address Select Input which selects one of three I <sup>2</sup> C addresses for the AD7994/AD7993 as shown in Table I.
$\overline{\text{CONVST}}$	Logic Input Signal. Convert Start Signal. This is an edge triggered logic input. The rising edge of this signal powers up the part. The power up time for the part is 1μs. The falling edge of $\overline{\text{CONVST}}$ places the track/hold into hold mode and initiates a conversion. A power up time of at least 1μs must be allowed for the $\overline{\text{CONVST}}$ high pulse, otherwise the conversion result will be invalid. (See Modes of Operation Section)
ALERT/BUSY	Digital Output, selectable as an ALERT or BUSY output function. When configured as an ALERT output, this pin acts as an Out of Range Indicator, and if enabled becomes active when the conversion result violates the DATA <sub>HIGH</sub> or DATA <sub>LOW</sub> values. See Limit Registers section. When configured as a BUSY output, this pin becomes active when a conversion is in progress.
SDA	Digital I/O. Serial Bus Bi-directional Data. Open-drain output. External pull-up resistor required.
SCL	Digital Input. Serial Bus Clock. External pull-up resistor required.

### AD7994/AD7993 PIN CONFIGURATION TSSOP





# PRELIMINARY TECHNICAL DATA

## AD7994/AD7993

**Table I. I<sup>2</sup>C Address Selection**

Part Number	AS Pin	I <sup>2</sup> C Address
AD7993-0	GND	010 0001
AD7993-0	V <sub>DD</sub>	010 0010
AD7993-1	GND	010 0011
AD7993-1	V <sub>DD</sub>	010 0100
AD7993-X <sup>1</sup>	Float	010 0000

Note:-

<sup>1</sup>. If the AS pin is left floating on any of the AD7993 parts the device address will be 010 0000

Part Number	AS Pin	I <sup>2</sup> C Address
AD7994-0	GND	010 0001
AD7994-0	V <sub>DD</sub>	010 0010
AD7994-1	GND	010 0011
AD7994-1	V <sub>DD</sub>	010 0100
AD7994-X <sup>1</sup>	Float	010 0000

Note :-

<sup>1</sup>. If the AS pin is left floating on any of the AD7994 parts the device address will be 010 0000

## AD7994/AD7993

## TERMINOLOGY

**Signal to (Noise + Distortion) Ratio**

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ( $f_s/2$ ), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02 N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB

**Total Harmonic Distortion**

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7994/AD7993, it is defined as:

$$\text{THD (dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where  $V_1$  is the rms amplitude of the fundamental and  $V_2$ ,  $V_3$ ,  $V_4$ ,  $V_5$  and  $V_6$  are the rms amplitudes of the second through the sixth harmonics.

**Peak Harmonic or Spurious Noise**

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to  $f_s/2$  and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

**Intermodulation Distortion**

With inputs consisting of sine waves at two frequencies,  $f_a$  and  $f_b$ , any active device with nonlinearities will create distortion products at sum and difference frequencies of  $m f_a \pm n f_b$  where  $m, n = 0, 1, 2, 3$ , etc. Intermodulation distortion terms are those for which neither  $m$  nor  $n$  are equal to zero. For example, the second order terms include  $(f_a + f_b)$  and  $(f_a - f_b)$ , while the third order terms include  $(2f_a + f_b)$ ,  $(2f_a - f_b)$ ,  $(f_a + 2f_b)$  and  $(f_a - 2f_b)$ .

The AD7994/AD7993 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

**Channel-to-Channel Isolation**

Channel-to-Channel Isolation is a measure of the level of crosstalk between channels. It is measured by applying a fullscale TBD kHz sine wave signal to the nonselected input channels and determining how much the TBD kHz signal is attenuated in the selected channel. This figure is given worse case across all channels.

**Aperture Delay**

This is the measured interval between the leading edge of the sampling clock and the point at which the ADC actually takes the sample.

**Aperture Jitter**

This is the sample-to-sample variation in the effective point in time at which the sample is taken.

**Full Power Bandwidth**

The Full Power Bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed Fundamental is reduced by 0.1 dB or 3 dB for a full-scale input

**PSRR (Power Supply Rejection)**

The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency,  $f_s$ , to the power of a 200 mV p-p sine wave applied to the ADC  $V_{DD}$  supply of frequency  $f_s$ .

$$\text{PSRR (dB)} = 10 \log (P_f/P_{fs})$$

$P_f$  is the power at frequency  $f$  in the ADC output;  $P_{fs}$  is the power at frequency  $f_s$  coupled into the ADC  $V_{DD}$  supply.

**Integral Nonlinearity**

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

**Differential Nonlinearity**

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**

This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e. AGND + 1LSB

**Offset Error Match**

This is the difference in offset error between any two channels.

**Gain Error**

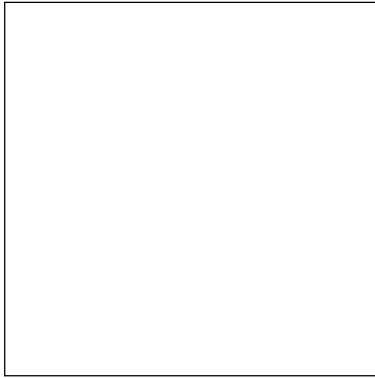
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e.,  $REF_{IN} - 1$  LSB) after the offset error has been adjusted out.

**Gain Error Match**

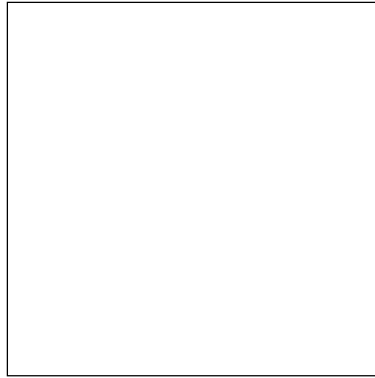
This is the difference in Gain error between any two channels.

### AD7994/AD7993 TYPICAL PERFORMANCE CURVES

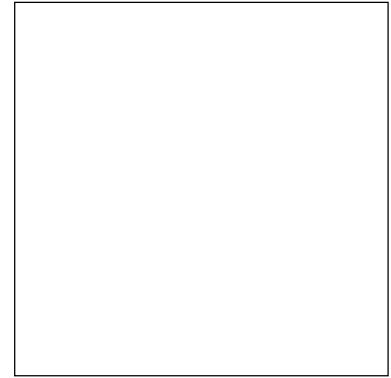
TPC 1 shows a typical FFT plot for the AD7994 at TBD kSPS sample rate and TBD kHz input frequency.



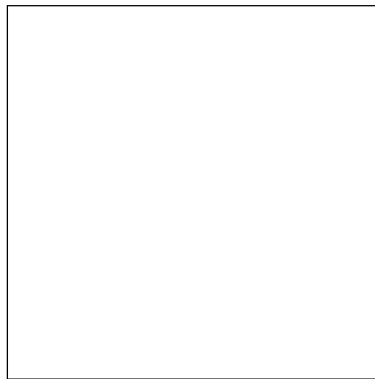
*TPC 1. AD7994 Dynamic Performance at TBD kSPS.*



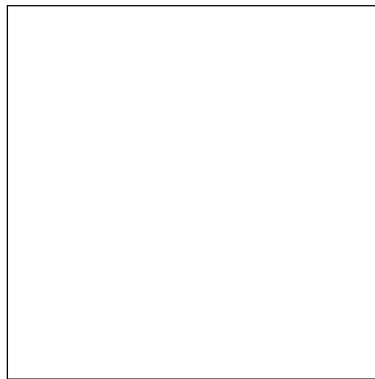
*TPC 2. AD7993 Dynamic Performance at TBD kSPS.*



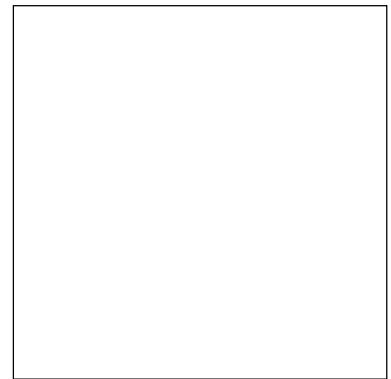
*TPC 3. PSRR vs Supply Ripple Frequency.*



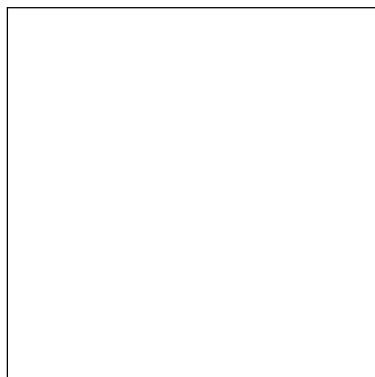
*TPC 4. AD7994 SINAD vs Analog Input Frequency for Various Supply Voltages at TBD kSPS.*



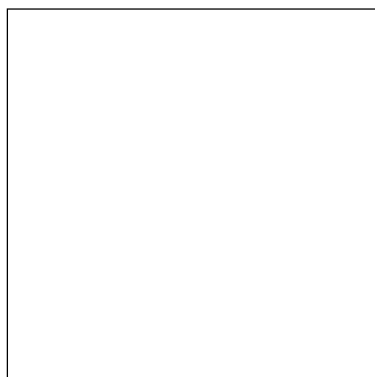
*TPC 5. AD7994 Typical INL  $V_{DD} = 5V$ .*



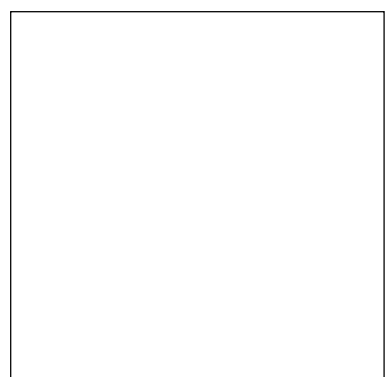
*TPC 6. AD7994 Typical DNL  $V_{DD} = 5V$ .*



*TPC 7. AD7994 Typical INL  $V_{DD} = 3V$ .*



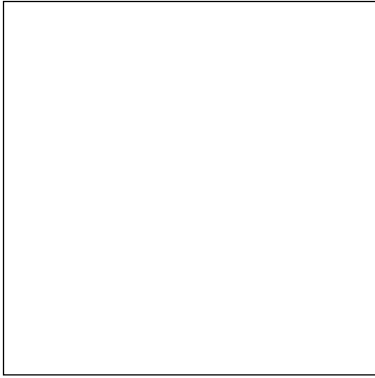
*TPC 8. AD7994 Typical DNL  $V_{DD} = 3V$ .*



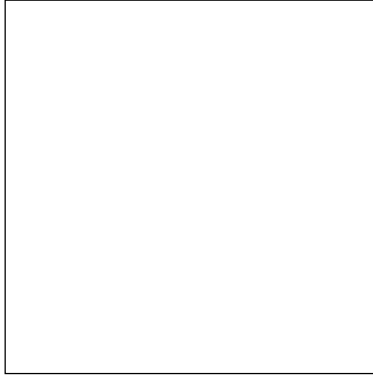
*TPC 9. AD7994 Change in INL vs Reference Voltage  $V_{DD} = 5V$ .*

# PRELIMINARY TECHNICAL DATA

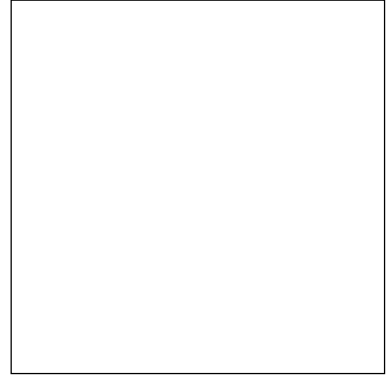
## AD7994/AD7993



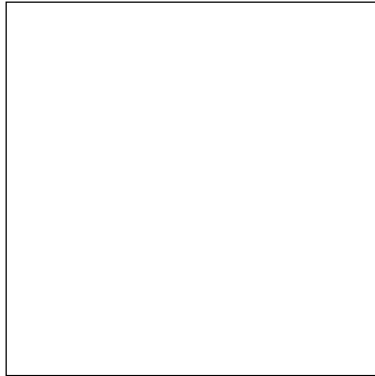
*TPC 10. AD7994 Change in DNL vs Reference Voltage.*



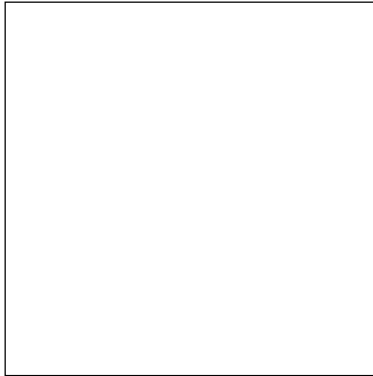
*TPC 11. AD7994 Shutdown Current vs Supply Voltage, -40 , 25 and 85 °C.*



*TPC 12. AD7994 Supply Current vs I<sup>2</sup>C Bus Rate for V<sub>DD</sub> = 3V and 5V.*



*TPC 13. AD7994 Supply Current vs Supply Voltage for Various Temperatures.*



*TPC 14. AD7994 ENOB vs Reference Voltage, V<sub>DD</sub> = 3V and V<sub>DD</sub> = 5V.*

**CIRCUIT INFORMATION**

The AD7994/AD7993 are fast, low-power, 12-/10-bit, single supply, 4 Channel A/D converters respectively. The parts can be operated from a 2.7 V to 5.5 V supply.

The AD7994/AD7993 provide the user with a 4-channel multiplexer, an on-chip track/hold, A/D converter, an on-chip oscillator, internal data registers and an I<sup>2</sup>C compatible serial interface, all housed in a 16-lead TSSOP package, which offers the user considerable space saving advantages over alternative solutions. An external reference is required by the AD7994/AD7993, and this reference can be in the range of 1.2 V to V<sub>DD</sub>.

The AD7994/AD7993 will normally remain in a power-down state while not converting. When supplies are first applied the part will come up in a shutdown state. Power-up is initiated prior to a conversion and the device returns to power-down upon completion of the conversion. Conversions can be initiated on the AD7994/AD7993 by either pulsing the  $\overline{\text{CONVST}}$  signal, using an automatic cycling mode or using a mode where wake-up and conversion occur during the write function ( see modes of Operation section). On completion of a conversion the AD7994/AD7993 will enter shutdown mode again. This automatic shutdown feature allows power saving between conversions. This means any read or write operations across the I<sup>2</sup>C interface can occur while the device is in shut-down.

**CONVERTER OPERATION**

The AD7994/AD7993 are successive approximation analog-to-digital converters based around a capacitive DAC. Figures 2 and 3 show simplified schematics of the ADC during its acquisition and conversion phase respectively. Figure 2 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition and the sampling capacitor acquires the signal on V<sub>INX</sub>.

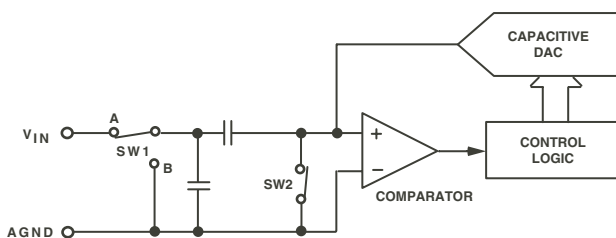


Figure 2. ADC Acquisition Phase

When the ADC starts a conversion, see Figure 3, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The input is disconnected once the conversion begins. The Control Logic and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 4 shows the ADC transfer function.

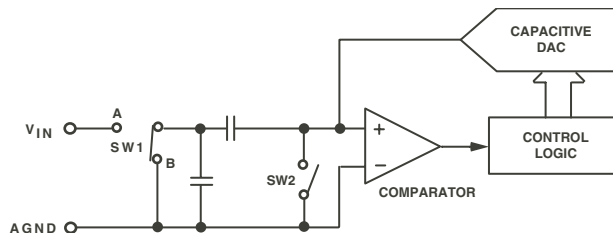


Figure 3. ADC Conversion Phase

**ADC TRANSFER FUNCTION**

The output coding of the AD7994/AD7993 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1LSB, 2LSBs, etc.). The LSB size for the AD7994 is  $= \text{REF}_{\text{IN}}/4096$  and  $\text{REF}_{\text{IN}}/256$  for the AD7993. The ideal transfer characteristic for the AD7994/AD7993 is shown in Figure 4 below.

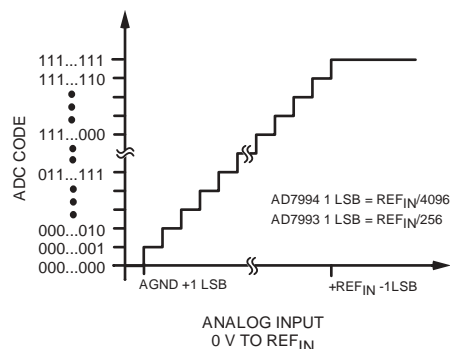


Figure 4. AD7994/AD7993 Transfer Characteristic

**TYPICAL CONNECTION DIAGRAM**

Figure 5 shows the typical connection diagram for the AD7994/AD7993. In Figure 5 the Address Select pin, AS, is tied to V<sub>DD</sub>, however AS can also be either tied to GND or left floating, allowing the user to select up to three AD7994/AD7993 devices on the same serial bus. An external reference must be applied to the AD7994/AD7993. This reference can be in the range of 1.2 V to V<sub>DD</sub>. A precision reference like the REF 19X family, ADR421, ADR03, ADR381 can be used to supply the Reference Voltage to the ADC.

SDA and SCL form the two-wire I<sup>2</sup>C/SMBus compatible interface. External Pull-up resistors should be added to the SDA and SCL bus lines.

The AD7994-0/AD7993-0 support Standard and Fast I<sup>2</sup>C Interface Modes. While the AD7994-1/AD7993-1 support Standard, Fast and High-speed I<sup>2</sup>C Interface Modes. Therefore if operating the AD7994/AD7993 in either Standard or Fast Mode, up to five AD7994/AD7993 devices (3 x AD7994-0/AD7993-0 and 2 x AD7994-1/AD7993-1 or 3 x AD7994-1/AD7993-1 and 2 x AD7994-0/AD7993-0) can be connected to the bus. When operating in Hs-Mode then up to three AD7994-1/AD7993-1 devices can be connected to the bus.

Wake-up from power-down prior to a conversion is approximately 1 $\mu$ s while conversion time is approximately 2 $\mu$ s. The AD7994/AD7993 enters power-down mode again after each conversion, this will be useful in applications where power consumption is of concern.

AD7994/AD7993

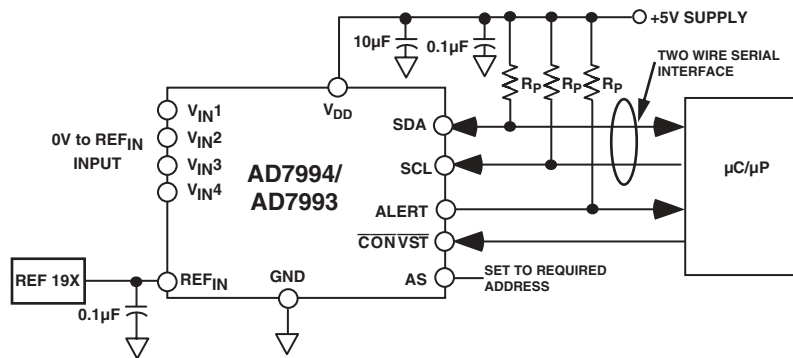


Figure 5 AD7994/AD7993 Typical Connection Diagram

Analog Input

Figure 6 shows an equivalent circuit of the analog input structure of the AD7994/AD7993. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 10 mA is the maximum current these diodes can conduct without causing irreversible damage to the part.

The capacitor C1 in Figure 6 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance ( $R_{ON}$ ) of a switch(track and hold switch) and also includes the  $R_{ON}$  of the input multiplexer. The total resistance is typically about 400Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 30 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The

maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 7 shows a graph of the Total Harmonic Distortion vs. analog input signal frequency for different source impedances when using a supply voltage of  $3V \pm 10\%$  and  $5V \pm 10\%$  and sampling at a rate of  $xkSPS$ . Figure 8 shows a graph of the total harmonic distortion versus analog input signal frequency for various supply voltages while sampling at  $xkSPS$ .

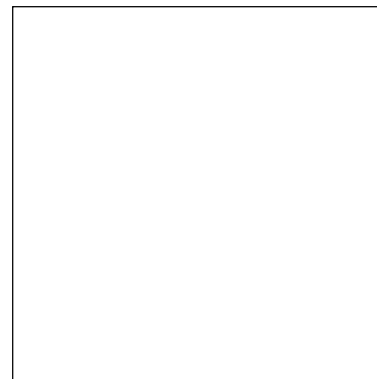


Figure 7. THD vs. Analog Input Frequency for Various Source Impedance for  $V_{DD} = 3V$  and  $5V$

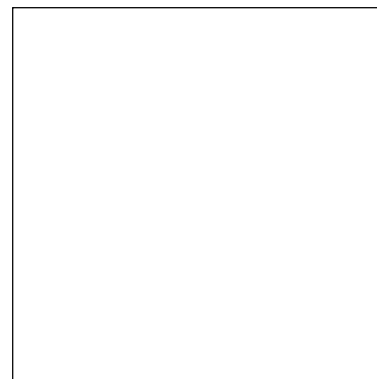


Figure 8. THD vs. Analog Input Frequency,  $F_s = xkSPS$

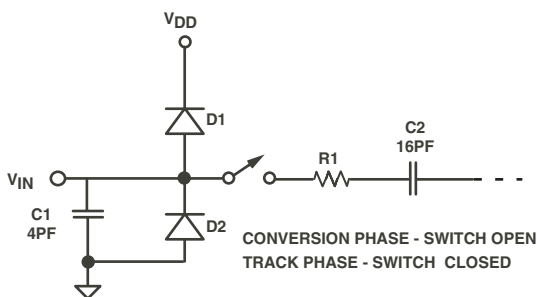


Figure 6. Equivalent Analog Input Circuit

**INTERNAL REGISTER STRUCTURE**

The AD7994/AD7993 contains seventeen internal registers, as shown in Figure 9, that are used to store conversion results, high and low conversion limits, and to configure and control the device. Sixteen are data registers and one is an address pointer register.

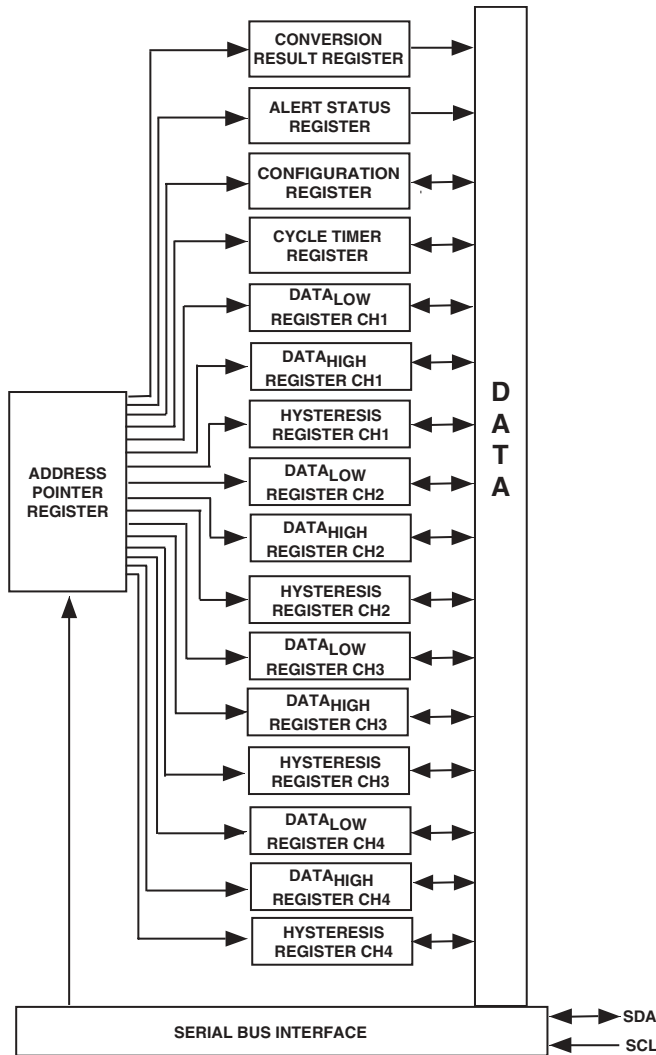


Figure 9. AD7994/AD7993 Register Structure

Each data register has an address which is pointed to by the Address Pointer register when communicating with it. The Conversion Result Register is the only data register that is read only.

**ADDRESS POINTER REGISTER**

The Address Pointer register itself does not have, nor does it require, an address, as it is the register to which the first data byte of every Write operation is written automatically. The Address Pointer Register is an 8-bit register in which the four LSBs are used as pointer bits to store an address that points to one of the data registers of the AD7994/AD7993, while the four MSBs are used as command bits when operating in Mode 2 (see Modes of Operation section). The first byte following each write address is the address of one of the data registers, which is stored in the Address Pointer Register, and selects the data register to which subsequent data bytes are written. Only the four LSBs of this register are used to select a data register. On Power up the Address Point register contains all 0's, pointing to the Conversion Result Register.

Table II. Address Pointer Register

C4	C3	C2	C1	P3	P2	P1	P0
0	0	0	0	Register Select			

Table III. AD7994/AD7993 Register Addresses

P3	P2	P1	P0	Registers
0	0	0	0	Conversion Result Register (Read)
0	0	0	1	Alert Status Register (Read/Write)
0	0	1	0	Configuration Register (Read/Write)
0	0	1	1	Cycle Timer Register (Read/Write)
0	1	0	0	DATA <sub>LOW</sub> Reg CH1 (Read/Write)
0	1	0	1	DATA <sub>HIGH</sub> Reg CH1 (Read/Write)
0	1	1	0	Hysteresis Reg CH1 (Read/Write)
0	1	1	1	DATA <sub>LOW</sub> Reg CH2 (Read/Write)
1	0	0	0	DATA <sub>HIGH</sub> Reg CH2 (Read/Write)
1	0	0	1	Hysteresis Reg CH2 (Read/Write)
1	0	1	0	DATA <sub>LOW</sub> Reg CH3 (Read/Write)
1	0	1	1	DATA <sub>HIGH</sub> Reg CH3 (Read/Write)
1	1	0	0	Hysteresis Reg CH3 (Read/Write)
1	1	0	1	DATA <sub>LOW</sub> Reg CH4 (Read/Write)
1	1	1	0	DATA <sub>HIGH</sub> Reg CH4 (Read/Write)
1	1	1	1	Hysteresis Reg CH4 (Read/Write)

# PRELIMINARY TECHNICAL DATA

## AD7994/AD7993

### CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register that is used to set the operating modes of the AD7994/AD7993. The bit functions of all 8 bits of the Configuration Register are outlined in Table IV.

**Table IV. Configuration Register Bit Function Description**

D7	D6	D5	D4	D3	D2	D1	D0
CH4	CH3	CH2	CH1	FLTR	ALERT EN	BUSY/ALERT	ALERT/BUSY POLARITY
0*	0*	0*	0*	1*	0*	0*	0*

\*Default settings at Power-up

Bit	Mnemonic	Comment
D7-D4	CH4-CH1	These four channel address bits select the analog input channel(s) to be converted on. A 1 in any of bits D7 to D4 selects a channel for conversion. If more than one channel bit is set to 1 then the AD7994/AD7993 will sequence through the selected channels, starting with the lowest channel. All unused channels should be set to zero. Table V shows how these four channel address bits are decoded. <b><i>Prior to initiating a conversion a channel(s) must be selected in the Configuration Register.</i></b>
D3	FLTR	The value written to this bit of the Control Register determines whether the filtering on SDA and SCL is enabled or to be bypassed. If this bit is a 1 then the filtering is enabled, if it is a 0, then the filtering is bypassed.
D2	ALERT EN	The hardware ALERT function is enabled if this bit is set to 1 and disabled if set to 0. This bit is used in conjunction with the BUSY/ALERT bit to determine if the ALERT/BUSY pin will act as an ALERT or a BUSY output. (See Table VI.)
D1	BUSY/ALERT	This bit is used in conjunction with the ALERT EN bit to determine if the ALERT/BUSY output, pin 13, will act as an ALERT or BUSY output (see TABLE V1), or if pin 13 is configured as an ALERT output pin, if it is to be reset. When reading the Configuration register D1 will always be a 0 when D2 is a 1.
D0	BUSY/ALERT POLARITY	This bit determines the active polarity of the ALERT/BUSY pin regardless of whether it is configured as an ALERT or BUSY output. It is active low if this bit is set to 0, and it is active high if set to 1.



Table V. Channel Selection

D7	D6	D5	D4	Analog Input Channel
0	0	0	0	No channel selected, see Address Pointer Byte, Mode 2
0	0	0	1	Convert on $V_{IN1}$
0	0	1	0	Convert on $V_{IN2}$
0	0	1	1	Sequence between $V_{IN1}$ and $V_{IN2}$
0	1	0	0	Convert on $V_{IN3}$
0	1	0	1	Sequence between $V_{IN1}$ and $V_{IN3}$
0	1	1	0	Sequence between $V_{IN2}$ and $V_{IN3}$
0	1	1	1	Sequence between $V_{IN1}$ , $V_{IN2}$ and $V_{IN3}$
1	0	0	0	Convert on $V_{IN4}$
1	0	0	1	Sequence between $V_{IN1}$ and $V_{IN4}$
1	0	1	0	Sequence between $V_{IN2}$ and $V_{IN4}$
1	0	1	1	Sequence between $V_{IN1}$ , $V_{IN2}$ and $V_{IN4}$
1	1	0	0	Sequence between $V_{IN3}$ and $V_{IN4}$
1	1	0	1	Sequence between $V_{IN1}$ , $V_{IN3}$ and $V_{IN4}$
1	1	1	0	Sequence between $V_{IN2}$ , $V_{IN3}$ and $V_{IN4}$
1	1	1	1	Sequence between $V_{IN1}$ , $V_{IN2}$ , $V_{IN3}$ and $V_{IN4}$

**Note 1:-** The AD7994/AD7993 converts on the selected channel in the Sequence in ascending order, starting with the lowest channel in the sequence.

Table VI. ALERT/BUSY Function

D2	D1	ALERT/BUSY Pin Configuration
0	0	Pin does not provide any interrupt signal.
0	1	Pin configured as a BUSY output.
1	0	Pin configured as an ALERT output.
1	1	Resets ALERT output pin, Alert_Flag bit in Conversion Result Reg, and entire Alert Status Reg ( if any active).

If 1/1 is written to bits D2/D1 in the configuration Register to reset the ALERT pin, the Alert Flag bit and the Alert Status Register; the contents of the Configuration Register will read 1/0 for D2/D1 respectively if read back.

**CONVERSION RESULT REGISTER**

The Conversion Result Register is a 16-bit read-only register which stores the conversion result from the ADC in Straight Binary format. A Two Byte read is necessary to read data from this register. Table VIIa shows the contents of the first byte to be read while Table VIIb show the contents of the second byte to be read from AD7994/AD7993.

Table VIIa. Conversion Value Register (First Read)

D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	Zero	CH_ID1	CH_ID0	MSB	B10	B9	B8

Table VIIb. Conversion Value Register (Second Read)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1/0	B0/0

The AD7994/AD7993 conversion result consists of an Alert\_Flag bit, a leading zero, two Channel Identifier bits and the 12-/10- bit data result. For the AD7993 the two LSBs (D1 and D0) of the second read will contain two zeros.

The Alert\_Flag bit indicates whether the conversion result being read or any other channel result has violated the limit registers associated with it. The Master may wish to read the ALERT Status register to obtain more information on where the ALERT occurred if this Alert\_Flag bit is set.

This is followed by a leading zero and the two Channel Identifier bits indicating which channel the conversion result corresponds to. The 12-/10-bit conversion result then follows MSB first.

Alert_Flag <sup>1</sup>	Zero	CH_ID1	CH_ID0	Channel# Result
0/1	0	0	0	Channel 1( $V_{IN1}$ )
0/1	0	0	1	Channel 2( $V_{IN2}$ )
0/1	0	1	0	Channel 3( $V_{IN3}$ )
0/1	0	1	1	Channel 4( $V_{IN4}$ )

# AD7994/AD7993

## LIMIT REGISTERS

The AD7994/AD7993 has four pairs of limit registers, each to store high and low conversion limits for each analog input channel. Each pair of limit registers has one associated hysteresis register. All twelve registers are 16-bits wide, only the 12 LSBs of the Registers are used for the AD7994/AD7993, However on the AD7993 the 2 LSBs, D1 and D0, should contain 0s. On power-up, the contents of the DATA<sub>HIGH</sub> Register for each channel will be fullscale, while the contents of the DATA<sub>LOW</sub> registers will be zeroscale by default. The Limit Registers can be used to monitor the conversion results on each on the Analog input channels. The AD7994/AD7993 will signal an Alert ( in either hardware or software or both depending on configuration) if the result moves outside the upper or lower limit set by the limit registers.

### DATA<sub>HIGH</sub> REGISTER CH1/CH2/CH3/CH4

The DATA<sub>HIGH</sub> Register for each channel is a 16-bit read/write register, only the 12 LSBs of the Register are used. The Registers store the upper limit that will activate the ALERT output and/or the Alert\_Flag bit in the Conversion Result Register. Therefore, if the value in the Conversion Result Register is greater than the value in the DATA<sub>HIGH</sub> Register, then the Alert\_Flag bit is set to 1 and the ALERT pin is activated (the latter is true if ALERT is enabled in the Configuration Register). When the conversion result returns to a value at least N LSBs below the DATA<sub>HIGH</sub> Register value the ALERT output pin and Alert\_Flag bit will be reset. The value of N is taken from the 12-bit Hysteresis register associated with that channel. The ALERT pin can also be reset by writing to bits D2, D1 in the Configuration Register. For the AD7993, D1 and D0 of the DATA<sub>HIGH</sub> register should contain 0's.

**Table VIIIa. DATA<sub>HIGH</sub> Register (First Read/Write)**

D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

**Table VIIIb. DATA<sub>HIGH</sub> Register (Second Read/Write)**

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

### DATA<sub>LOW</sub> REGISTER CH1/CH2/CH3/CH4

The DATA<sub>LOW</sub> Register for each channel is a 16-bit read/write register, of which only the 12 LSBs are used. The Register stores the lower limit that will activate the ALERT output and/or the Alert\_Flag bit in the conversion result register. Therefore, if the value in the Conversion Result Register is less than the value in the DATA<sub>LOW</sub> Register, then the Alert\_Flag bit is set to 1 and the ALERT pin is activated (the latter is true if ALERT is enabled in the Configuration Register). When the Conversion result returns to a value at least N LSBs above the DATA<sub>LOW</sub> Register value the ALERT output pin and Alert\_Flag bit will be reset. The value of N is taken from

the 12-bit Hysteresis register associated with that channel. The ALERT pin can also be reset by writing to bit D2, D1 in the Configuration Register. For the AD7993 D1 and D0 of the DATA<sub>LOW</sub> register should contain 0's.

**Table IXa. DATA<sub>LOW</sub> Register (First Read/Write)**

D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

**Table IXb. DATA<sub>LOW</sub> Register (Second Read/Write)**

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

### HYSTERESIS REGISTER (CH1/CH2/CH3/CH4)

Each Hysteresis Register is a 16-bit read/write register, only the 12 LSBs of the register are used. The Registers store the hysteresis value, N when using the limit registers. Each pair of Limit registers has a dedicated hysteresis register. The hysteresis value determines the reset point for the ALERT pin/Alert\_Flag if a violation of the limits has occurred. If a hysteresis value of say 8 LSBs is required on the upper and lower limits of channel 1 then the 12 bit word, 0000 0000 0000 1000, should be written to the Hysteresis Register CH1, the address of which is shown in Table III. On power up, the Hysteresis Registers will contain a value of 8 LSBs for the AD7994 and 2 LSBs for the AD7993. If a different hysteresis value is required then that value must be written to the Hysteresis Register for the channel in question. For the AD7993 D1 and D0 of the Hysteresis Register should contain 0's.

**Table Xa. Hysteresis Register (First Read/Write)**

D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

**Table Xb. Hysteresis Register (Second Read/Write)**

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

### Using the Limit Registers to Store Min/Max Conversion Results

If fullscale, i.e. all 1s, is written to the Hysteresis register for a particular channel then the DATA<sub>HIGH</sub> and DATA<sub>LOW</sub> Registers for that channel will no longer act as Limit registers as previously described, but instead they will act as storage registers for the maximum and minimum conversion results returned from conversions on a channel over any given period of time. This function is useful in applications where the widest span of actual conversion results is required rather than using the ALERT to signal an intervention is necessary, e.g. monitoring temperature extremes during refrigerated goods transportation. When using the limit registers to store the min and

max conversion results, the Alert\_Flag bit, D15, can be used to indicate that an alert has happened on another one of the Input channels.

It must be noted that on power-up, the contents of the DATA<sub>HIGH</sub> register for each channel will be fullscale, while the contents of the DATA<sub>LOW</sub> registers will be zeroscale, by default minimum and maximum conversion values being stored in this way will be lost if power is removed or cycled.

When using the limit registers to store the min and max conversion results, the Alert\_Flag bit, D15, is used to indicate that an alert has happened on another one of the Input channels. If the Alert\_Flag bit is set to 1, it will be reset when the Conversion result returns to a value at least N LSBs above the DATA<sub>LOW</sub> Register value or below the DATA<sub>LOW</sub> Register value or if bits D2 and D1 of the Configuration Register are set to 1. The Alert\_Flag bit in the limit registers is useful if the user is not reading from the conversion result register when reading the min and max conversion results from the limit registers.

**ALERT STATUS REGISTER**

The Alert Status Register is a 8-bit read/write register, which provides information on an Alert event. If a conversion results in activating the ALERT pin or the Alert\_Flag bit in the Conversion Result Register, as described in the Limit Registers section, then the Alert Status Register may be read to gain further information. It contains 2 status bits per channel, one corresponding to the DATA<sub>HIGH</sub> limit and the other to the DATA<sub>LOW</sub> limit. Whichever bit has a status of 1 will show where the violation occurred, i.e. on which channel and whether on upper or lower limit. If a second alert event occurs on the other channel between receiving the first alert and interrogating the Alert Status register then the corresponding bit for that Alert event will be set also.

The entire contents of the Alert Status register may be cleared by writing 1,1, to bits D2 and D1 in the Configuration register as shown in Table VI. This may also be achieved by ‘writing’ all 1’s to the Alert Status Register itself. This means that if the Alert Status Register is addressed for a write operation which is all 1’s, then the contents of the Alert Status Register will then be cleared or reset to all 0’s. Alternatively, an individual active Alert bit(s) may be reset within the Alert Status Register by performing a write of ‘1’ to that bit alone. The advantage of this is that once an Alert event has been serviced, that particular bit can be reset, e.g. CH1<sub>LO</sub>, without clearing the entire contents of the Alert Status Register, thus preserving the status of any additional Alert, e.g. CH2<sub>HI</sub>, which may have occurred while servicing the first. If it is not necessary to clear an Alert directly after servicing then obviously the Alert Status register may be read again immediately to look for any new Alerts, bearing in mind that the one just serviced will still be active.

**Table XIb. Alert Status Register Bit Function Description**

Bit	Mnemonic	Comment
D0	CH1 <sub>LO</sub>	Violation of DATA <sub>LOW</sub> limit on Channel 1 if this bit set to 1, no violation if 0.
D1	CH1 <sub>HI</sub>	Violation of DATA <sub>HIGH</sub> limit on Channel 1 if this bit set to 1, no violation if 0.
D2	CH2 <sub>LO</sub>	Violation of DATA <sub>LOW</sub> limit on Channel 2 if this bit set to 1, no violation if 0.
D3	CH2 <sub>HI</sub>	Violation of DATA <sub>HIGH</sub> limit on Channel 2 if this bit set to 1, no violation if 0.
D4	CH3 <sub>LO</sub>	Violation of DATA <sub>LOW</sub> limit on Channel 3 if this bit set to 1, no violation if 0.
D5	CH3 <sub>HI</sub>	Violation of DATA <sub>HIGH</sub> limit on Channel 3 if this bit set to 1, no violation if 0.
D6	CH4 <sub>LO</sub>	Violation of DATA <sub>LOW</sub> limit on Channel 4 if this bit set to 1, no violation if 0.
D7	CH4 <sub>HI</sub>	Violation of DATA <sub>HIGH</sub> limit on Channel 4 if this bit set to 1, no violation if 0.

**Table XIa. Alert Status Register**

D7	D6	D5	D4	D3	D2	D1	D0
CH4 <sub>HI</sub>	CH4 <sub>LO</sub>	CH3 <sub>HI</sub>	CH3 <sub>LO</sub>	CH2 <sub>HI</sub>	CH2 <sub>LO</sub>	CH1 <sub>HI</sub>	CH1 <sub>LO</sub>

## AD7994/AD7993

**CYCLE TIMER REGISTER**

The Cycle Timer Register is a 8-bit read/write register, which stores the conversion interval value for the Automatic Cycle mode of the AD7994/AD7993, see Modes of Operation section. The five MSBs of the Cycle Timer Register are unused and should contain 0's at all times. On power up, the Cycle Timer Register will contain all 0s, thus disabling the Automatic Cycle operation of the AD7994/AD7993. To enable the Automatic Cycle Mode the user must write to the Cycle Timer Register, selecting the required conversion interval. Table XIIa shows the structure of the Cycle Timer register while Table XIIb shows how the bits in this register are decoded to provide various automatic sampling intervals.

**Table XIIa. Cycle Timer Register**

D7	D6	D5	D4	D3	D2	D1	D0
Sample Dealy	Bit Trial Delay	0	0	0	Cyc Bit2	Cyc Bit1	Cyc Bit0
0*	0*	0*	0*	0*	0*	0*	0*

\* Default settings on Power-up

**Table XIIb. Cycle Timer Intervals**

D2	D1	D0	Conversion Interval (typ)
0	0	0	Mode not selected
0	0	1	$T_{\text{CONVERT}} \times 32$
0	1	0	$T_{\text{CONVERT}} \times 64$
0	1	1	$T_{\text{CONVERT}} \times 128$
1	0	0	$T_{\text{CONVERT}} \times 256$
1	0	1	$T_{\text{CONVERT}} \times 512$
1	1	0	$T_{\text{CONVERT}} \times 1024$
1	1	1	$T_{\text{CONVERT}} \times 2048$

$T_{\text{CONVERT}}$  is equivalent to the conversion time of the ADC.

**SERIAL INTERFACE**

Control of the AD7994/AD7993 is carried out via the I<sup>2</sup>C-compatible serial bus. The AD7994/AD7993 is connected to this bus as a slave device, under the control of a master device, e.g. the processor.

**SERIAL BUS ADDRESS**

Like all I<sup>2</sup>C-compatible devices, the AD7994/AD7993 has a 7-bit serial address. The three MSBs of this address for the AD7994/AD7993 are set to 010. The AD7994/AD7993 comes in two versions, the AD7994-0/AD7993-0 and AD7994-1/AD7993-1. The two versions have three different I<sup>2</sup>C addresses available which are selected by either tying the Address Select pin, AS, to GND, to V<sub>DD</sub> or letting the pin float (see Table I). By giving different addresses for the two versions, up to five AD7994/AD7993 devices can be connected to a single serial bus, or the addresses can be set to avoid conflicts with other devices on the bus. See I<sup>2</sup>C Address Selection table.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line, SCL, remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/W bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device.

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/W bit is a 0 then the master will write to the slave device. If the R/W bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to

high transition when the clock is high may be interpreted as a STOP signal.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will pull the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

**WRITING TO THE AD7994/AD7993**

Depending on the register being written to, there are two different writes for the AD7994/AD7993.

**Writing to the Address Pointer Register for a Subsequent Read**

In order to read from a particular register, the Address Pointer register must first contain the address of that register. If it does not, the correct address must be written to the Address pointer register by performing a single-byte write operation, as shown in Figure 10. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation may be subsequently performed to read the register of interest.

**Writing a Single Byte of Data to the Alert Status Register or Cycle Register**

The Configuration Register and Cycle Register are both 8-bit registers, so only one byte of data can be written to each. Writing a single byte of data to one of these registers consists of the serial bus write address, the chosen data register address written to the Address Pointer Register, followed by the data byte written to the selected data register. This is illustrated in Figure 11.

**Writing two Bytes of Data to a Limit Register, Hysteresis Register or Configuration register.**

Each of the four Limit Registers are 12-bit registers, so two bytes of data are required to write a value to any one of them. Writing two bytes of data to one of these registers consists of the serial bus write address, the chosen Limit Register address written to the Address Pointer Register, followed by two data bytes written to the selected data register. This is illustrated in Figure 12.

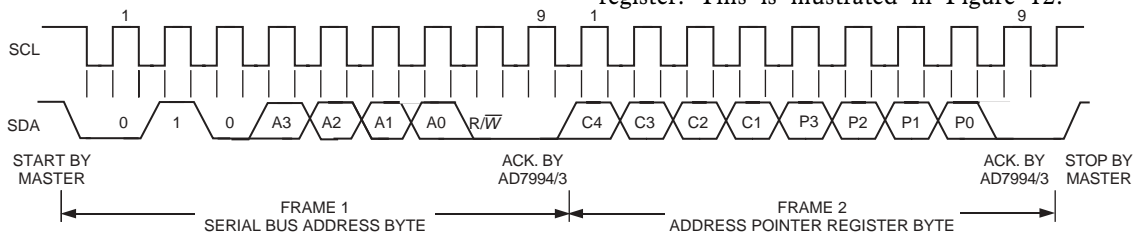


Figure 10. Writing to the Address Pointer Register to select a register for a subsequent Read operation

AD7994/AD7993

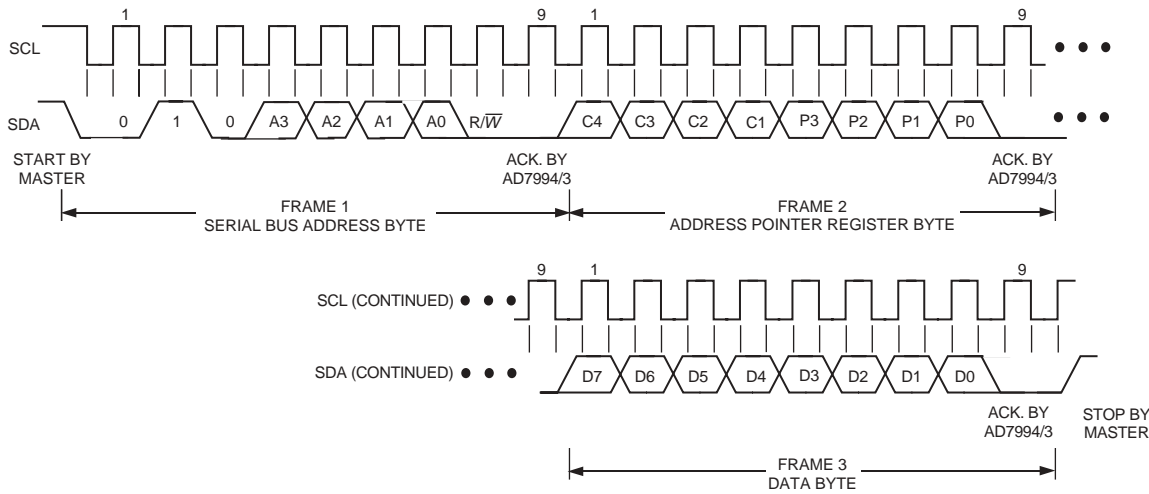


Figure 11. Single Byte Write Sequence

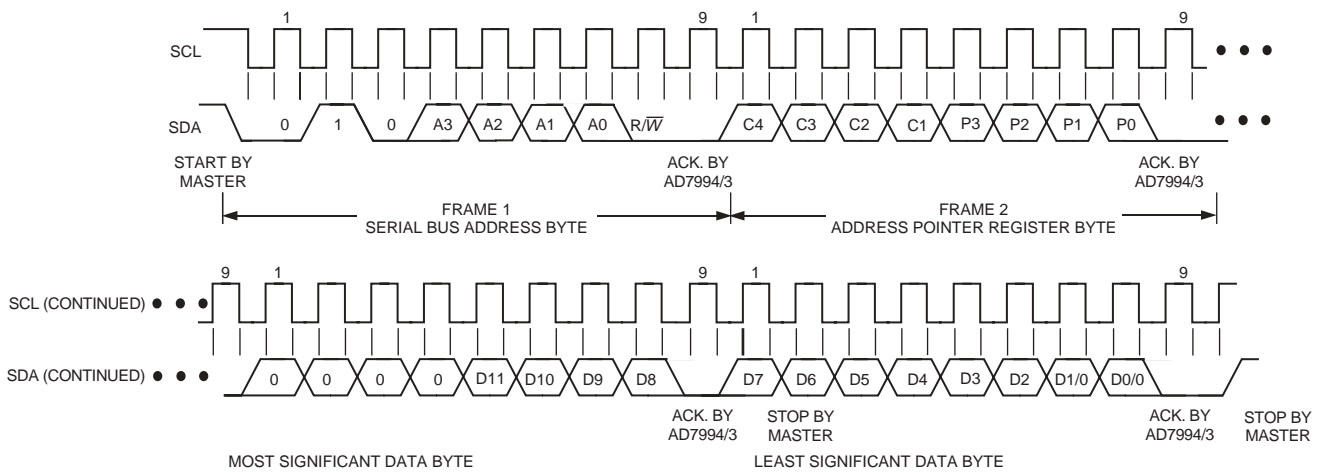


Figure 12. Two Byte Write Sequence

If the master is write addressing the AD7994/AD7993 and wishes to write to more than one register, then after the first write operation has completed for the first data register in the next byte they can simply write to the address pointer byte to select the next data register for a write operation. This eliminates the need to re-address the device in order to write to another data register.

**READING DATA FROM THE AD7994/AD7993**

Reading data from the AD7994/AD7993 is a one or two byte operation. Reading back the contents of the Configuration Register, Alert Status Register or the Cycle Timer Register is a single byte read operation as shown in Figure 13. This assumes the particular register address has previously been set up by a single byte write operation to the Address Pointer Register, Figure 10. Once the register

address has been set up, any number of reads can subsequently be performed from that particular register without having to write to the Address Pointer Register again. If a read from a different register is required, then the relevant register address will have to be written to the Address Pointer Register and again any number of reads from this register may then be performed.

Reading data from the Conversion Result Register, DATA<sub>HIGH</sub> Registers, DATA<sub>LOW</sub> Registers or Hysteresis Registers is a two byte operation as shown in Figure 14. The same rules apply for a two byte read as a single byte read.

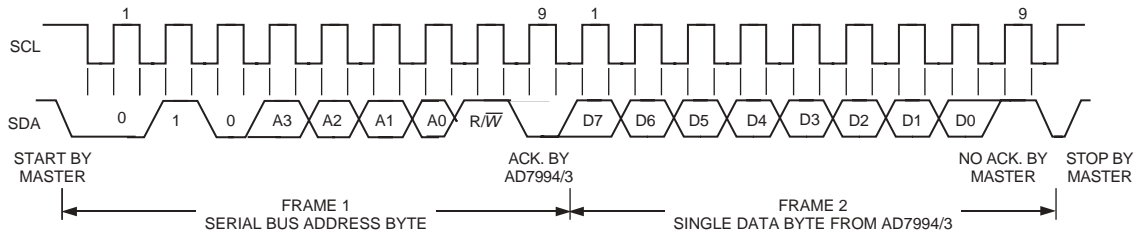


Figure 13. Reading a single byte of data from a selected register

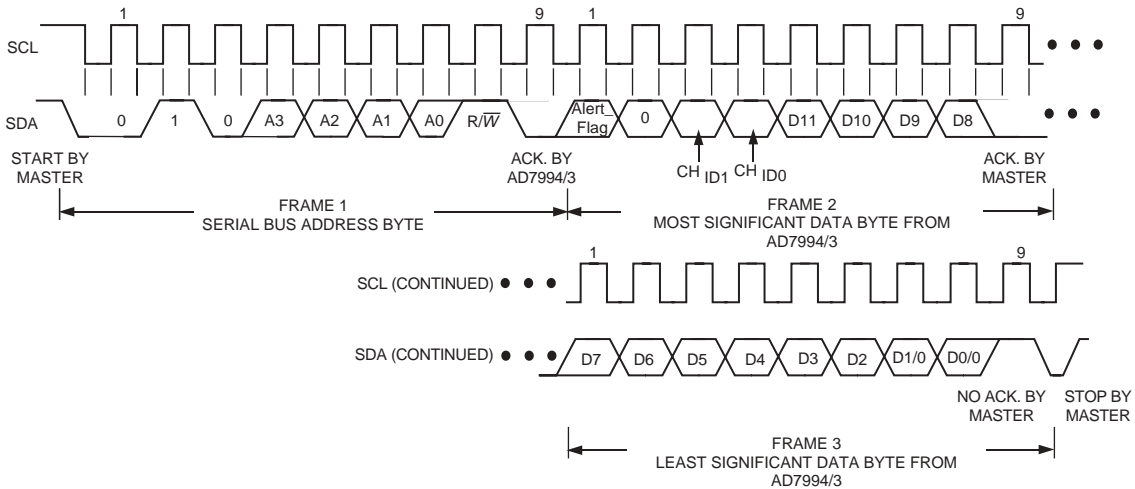


Figure 14. Reading two bytes of data from the Conversion Result Register

**ALERT/BUSY PIN**

The ALERT/BUSY may be configured as an Alert or Busy output as shown in Table VI.

**SMBus ALERT**

The AD7994/AD7993 ALERT output is an SMBus interrupt line for devices that want to trade their ability to master for an extra pin. The AD7994/AD7993 is a slave only device and uses the SMBus ALERT to signal the host device that it wants to talk. The SMBus ALERT on the AD7994/AD7993 is used as an out of conversion range indicator (a limit violation indicator).

The ALERT pin has an open-drain configuration which allows the ALERT outputs of several AD7994/AD7993 devices to be wired-AND together when the ALERT pin is active low. D0 of the Configuration Register is used to set the active polarity of the ALERT output. The power-up default is active low. The ALERT function can be disabled or enabled by setting D2 of the Configuration Register to 1 or 0 respectively.

The host device can process the ALERT interrupt and simultaneously access all SMBus ALERT devices through the alert response address. Only the device which pulled the ALERT low will acknowledge the ARA (Alert Response Address). If more than one device pulls the ALERT pin low, the highest priority (lowest address)

device will win communication rights via standard I<sup>2</sup>C arbitration during the slave address transfer.

The ALERT output becomes active when the value in the Conversion Result Register exceeds the value in the DATA<sub>HIGH</sub> Register or falls below the value in the DATA<sub>LOW</sub> Register. It is reset when a write operation to the Configuration register sets D1 to a 1, or when the conversion result returns N LSBs below or above the value stored in the DATA<sub>HIGH</sub> Register or DATA<sub>LOW</sub> Register respectively. N is the value in the Hysteresis register. (See Limit Registers section)

The ALERT output requires an external pull-up resistor. This can be connected to a voltage different from V<sub>DD</sub> provided the maximum voltage rating of the ALERT output pin is not exceeded. The value of the pull-up resistor depends on the application, but should be as large as possible to avoid excessive sink currents at the ALERT output.

AD7994/AD7993

**Placing the AD7994-1/AD7993-1 into High-speed Mode.**

Hs-Mode communication commences after the master addresses all devices connected to the bus with the Master code, 00001XXX, to indicate that a High-Speed Mode transfer is to begin. No device connected to the bus is allowed to Acknowledge the High-Speed Master code, therefore the code is followed by a not-Acknowledge, Figure 15. The master must then issue a repeated start followed by the device Address with a R/W bit. The selected device will then acknowledge its address.

All devices continue to operate in Hs-Mode until such a time as the master issues a STOP condition. When the STOP condition is issued the devices all return to F/S Mode.

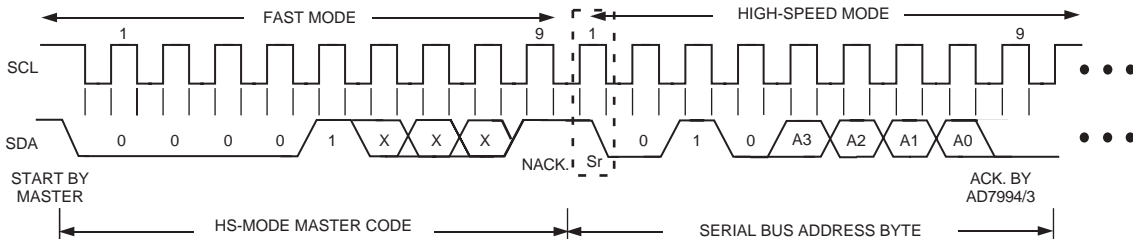


Figure 15. Placing the part into Hs Mode

**MODES OF OPERATION**

When supplies are first applied to the AD7994/AD7993, the ADC powers up in shutdown mode and will normally remain in this shutdown state while not converting. There are three different methods of initiating a conversion on the AD7994/AD7993.

**Mode 1 - Using CONVST Pin.**

A conversion can be initiated on the AD7994/AD7993 by pulsing the CONVST signal. The conversion clock for the part is internally generated so no external clock is required, except when reading from, or writing to the serial port. On the rising edge of CONVST the AD7994/AD7993 will begin to power up, see point A on Figure 16. The power up time from shutdown mode for the AD7994/AD7993 is approximately 1 us, the CONVST signal must remain high for 1 us for the part to power up fully. Then CONVST can be brought low after this time. The falling edge of the CONVST signal places the track and hold into hold mode and a conversion is also initiated at this point, see point B Figure 16. When the conversion

is complete, approximately 2 us later, the part will return to shutdown (see point C Figure 16) and remain so until the next rising edge of CONVST. The master can then read address the ADC to obtain the conversion result. The address pointer register must be pointing to the conversion result register in order to read back the conversion result.

If the CONVST pulse does not remain high for more than 1 us, then the falling edge of CONVST will still initiate a conversion but the result will be invalid as the AD7994/AD7993 will not be fully powered up when the conversion takes place. The CONVST pin should not be pulsed when reading from or writing to the serial port.

The Cycle Timer Register and bits C4 - C1 in the Address Pointer Register should contain all 0's to operate the AD7994/AD7993 in this mode. The CONVST pin should be tied low for all other Modes of operation. To select an Analog Input Channel for conversion in this mode, the user must write to the Configuration Register and select the corresponding channel for conversion. To set up a sequence of channels to be converted on with each CONVST pulse, set the corresponding channel bits in the Configuration register, see Table V.

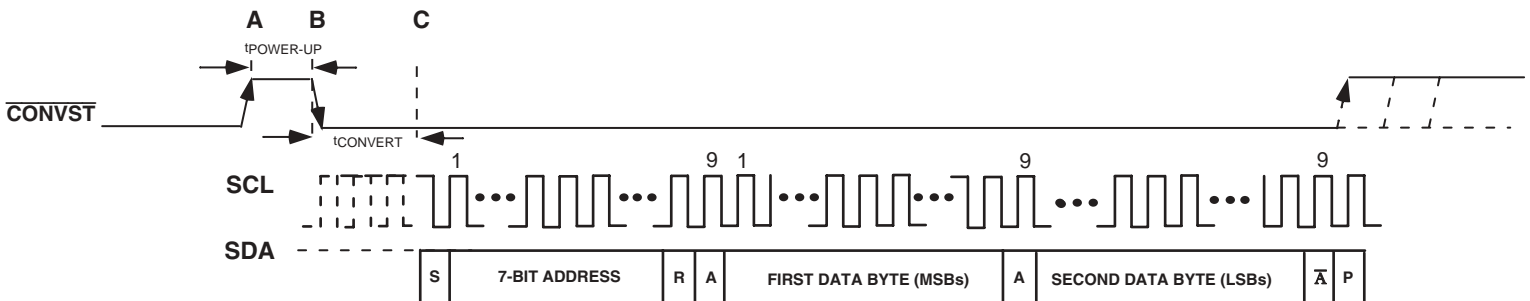


Figure 16. Mode 1 Operation



**Mode 2 -**

This mode allows a conversion to be automatically initiated anytime a read operation occurs. In order to use this mode the command bits C4 - C1 in the Address Pointer Byte shown in Table II must be programmed.

To select a particular Analog input for conversion in this mode, then the user must set the corresponding channel command bit to 1 in the Address Pointer Byte, see Table XIII. When all four command bits are 0 then this mode is not in use. A sequence can also be set up for this mode, if more than one of the command bit in the Address Pointer Byte are set. The ADC will start converting on the lowest channel in the sequence and then the next lowest until all the channels in the sequence have been converted on.

Figure 13 illustrates a two byte read operation from the Conversion Result Register. This operation would normally be preceded by a write to the Address Pointer Register so that the following read will access the desired register, in this case the Conversion Result Register Figure 10. When the contents of the Address Pointer Register are being loaded, if the command bits C4 to C1 are set then the AD7994/AD7993 will begin to power up and convert upon the selected channel(s), power-up will begin on the fifth SCL falling edge of the Address Point Byte,

see point A Figure 17. Table XIII shows the channel selection in this mode via the command bits, C4 to C1 in the Address Pointer Register. The wake-up and conversion time together should take approximately 3µs. Following this, the AD7994/AD7993 must be addressed again to tell it that a read operation is required. The read then takes place from the Conversion Result register. This read will access the result from the conversion selected via the command bits. If the Command bits C2, C1 were set to 1,1, then a four byte read would be necessary. The first read accesses the data from the conversion on V<sub>IN1</sub>. While this read takes place, a conversion occurs on V<sub>IN2</sub>. The second read will access this data from V<sub>IN2</sub>. Figure 18 illustrates how this mode operates.

When operating the AD7994-1/AD7993-1 in Mode2 with Hs-Mode, 3.4 MHz SCL, the conversion may not be complete before the master tries to read the conversion result, if this is the case the AD7994-1/AD7993-1 will hold the SCL line low after the read address during the ACK clock, until the conversion is complete. When the conversion is complete the AD7994-1/AD7993-1 will release the SCL line and the master can then read the conversion result.

**Table XIII Address Pointer Byte**

C4	C3	C2	C1	P3	P2	P1	P0	Analog Input Channel
0	0	0	0	0	0	0	0	Mode 2 not selected
0	0	0	1	0	0	0	0	Mode 2 Convert on V <sub>IN1</sub>
0	0	1	0	0	0	0	0	Mode 2 Convert on V <sub>IN2</sub>
0	0	1	1	0	0	0	0	Mode 2 Sequence between V <sub>IN1</sub> and V <sub>IN2</sub>
0	1	0	0	0	0	0	0	Mode 2 Convert on V <sub>IN3</sub>
0	1	0	1	0	0	0	0	Mode 2 Sequence between V <sub>IN1</sub> and V <sub>IN3</sub>
0	1	1	0	0	0	0	0	Mode 2 Sequence between V <sub>IN2</sub> and V <sub>IN3</sub>
0	1	1	1	0	0	0	0	Mode 2 Sequence between V <sub>IN1</sub> , V <sub>IN2</sub> and V <sub>IN3</sub>
1	0	0	0	0	0	0	0	Mode 2 Convert on V <sub>IN4</sub>
1	0	0	1	0	0	0	0	Mode 2 Sequence between V <sub>IN1</sub> and V <sub>IN4</sub>
1	0	1	0	0	0	0	0	Mode 2 Sequence between V <sub>IN2</sub> and V <sub>IN4</sub>
1	0	1	1	0	0	0	0	Mode 2 Sequence between V <sub>IN1</sub> , V <sub>IN2</sub> and V <sub>IN4</sub>
1	1	0	0	0	0	0	0	Mode 2 Sequence between V <sub>IN3</sub> and V <sub>IN4</sub>
1	1	0	1	0	0	0	0	Mode 2 Sequence between V <sub>IN1</sub> , V <sub>IN3</sub> and V <sub>IN4</sub>
1	1	1	0	0	0	0	0	Mode 2 Sequence between V <sub>IN2</sub> , V <sub>IN3</sub> and V <sub>IN4</sub>
1	1	1	1	0	0	0	0	Mode 2 Sequence between V <sub>IN1</sub> , V <sub>IN2</sub> , V <sub>IN3</sub> and V <sub>IN4</sub>

With the pointer bits set to all 0's then the next read will access the results of the conversion Result Register.

AD7994/AD7993

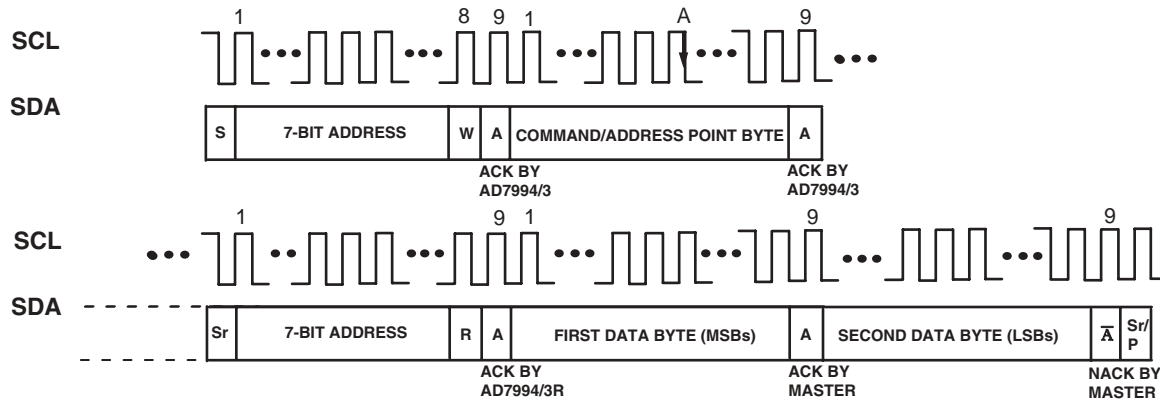


Figure 17. Mode 2 Operation

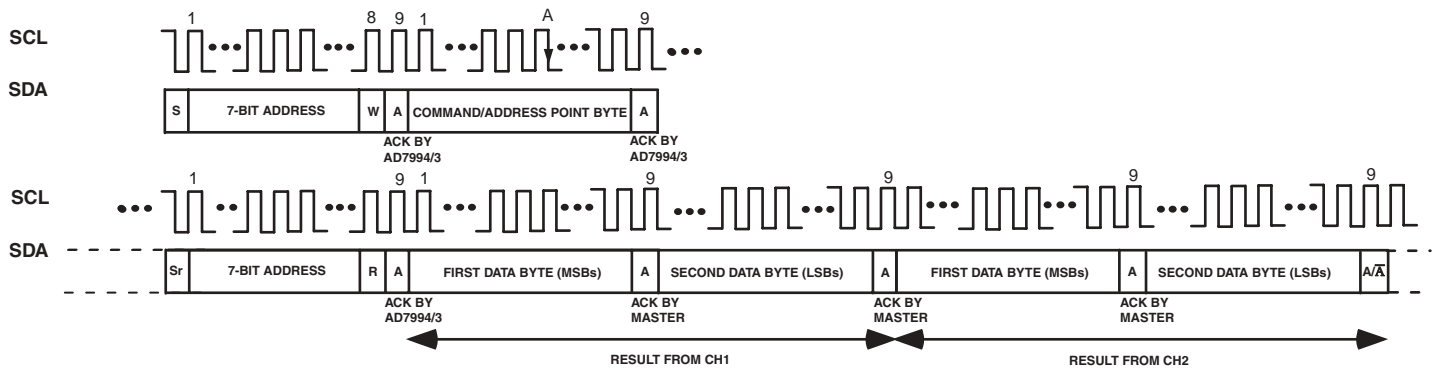


Figure 18. Mode 2 Sequence Operation

**Mode 3 - Automatic Cycle Mode**

An automatic conversion cycle can be selected and enabled by writing a value to the Cycle Timer Register. A conversion cycle interval can be set up on the AD7994/AD7993 by programming the relevant bits in the 3-bit Cycle Timer Register as decoded in Table XIIb. When the Cycle Timer register is programmed with any configuration other than all 0's, a conversion will take place every X ms, depending on the configuration of these bits in the Cycle Timer Register. There are 7 different cycle time intervals to choose from as shown in Table XIIb. Once the conversion has taken place the part powers down again until the next conversion occurs. To exit this mode of operation the user must program the Cycle Timer Register to contain all 0's. For cycle interval options see Table XIIb Cycle Timer Intervals. To select a channel(s) for operation in

the cycle mode set the corresponding channel bit(s), D7 to D4, of the Configuration Register. If more than one channel bit is set in the Configuration register the ADC will automatically cycle through the Channel sequence, starting with the lowest channel and working its way up through the sequence. Once the sequence is complete the ADC will start converting on the lowest channel again, continuing to loop through the sequence until the Cycle timer register contents are set to all 0's. This mode is useful for monitoring signals, e.g. battery voltage, temperature etc, interrupting only when the limits are violated.

It is recommended that no I<sup>2</sup>C Bus activity occurs when a conversion is taking place. However if this is not possible, e.g. when operating in Mode 2 or Mode 3, then in order to maintain the performance of the ADC, Bits D7 and D6 in the Cycle Timer Register are used to delay critical sample intervals and bit trials from occurring while there is activity on the I<sup>2</sup>C Bus. This will result in a quiet period for each bit decision. In certain cases where there is excessive activity on the interface lines this may have the effect of increasing the overall Conversion time. However if bit trial delays extend longer than 1 μs the conversion will terminate.

When bits D7 and D6 are both 0, the bit trial and sample interval delaying mechanism will be implemented. The default setting of D7 and D6 is 0. To turn off both set D7 and D6 to 1.

**Cycle Timer Register**

D7	D6	D5	D4	D3	D2	D1	D0
Sample Dealy	Bit Trial Delay	0	0	0	Cyc Bit2	Cyc Bit1	Cyc Bit0
0*	0*	0*	0*	0*	0*	0*	0*

\*Default settings at Power-up

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**16-Lead TSSOP (RU-16)**

