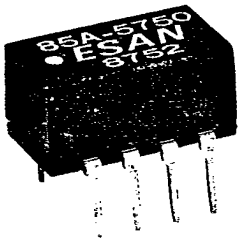
Active Delay Line (TTL Interface)

85A Series

- **5 Tap Output**
- **8 Pin Dil Package**
- **Auto-Insertable**



Specifications:

- Delay tolerance : ±5% or 2ns whichever is greater
- Rise time : 4ns max.
- Temp. coefficient : 100 ppm/°C
- Operating Temp. Range : −0°C to 70°C
- Minimum Pulse Width : 40% of total delay
- Supply Voltage : 5VDC ±5%
- Logic 1 Input current : 50 UA max.
- Logic 0 Input current : −2 mA max.
- Logic 1 Output : 2.75V min.
- Logic 0 Output : 0.4V max.
- Logic 1 Fan out : 20/TAP max.
- Logic 0 Fan out : 10/TAP max.
- Power Dissipation : 375 mW max.

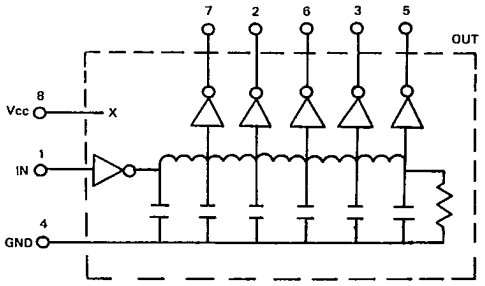
Test Conditions:

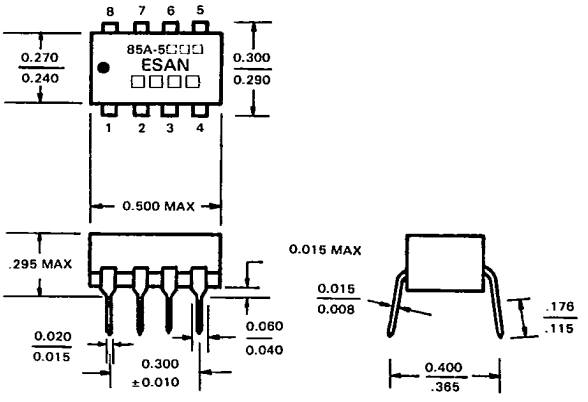
- Input pulse voltage : 3.2V
- Input pulse width : 1.2 * total delay
- Input pulse spacing : 2 * total delay
- Input pulse rise time: : 2 ns
- Rise time : 0.75V to 2.4V
- Time delay measured : @1.5V level
- All measurement : @Vcc = 5.0V, TA = 25°C

Features:

- Schottky TTL interface
- Low power schottky available named "85AL-5xxx" series
- Both Leading and Trailing edge available under request named "85B-5xxx" series

PART NO.	TOTAL DELAY (ns)	TAP TO TAP (ns)
85A-5250	25	5
85A-5500	50	10
85A-5750	75	15
85A-5101	100	20
85A-5125	125	25
85A-5151	150	30
85A-5201	200	40
85A-5251	250	50
85A-5301	300	60
85A-5401	400	80
85A-5501	500	100





Unit: Inch