R8610
Brief Sheet
32 BIT RISC MICRO CONTROLLER

1. Features

n Embedded RISC Controller

- Full 32 bit RISC architecture
- Supports diverse operation systems, including MS-Windows, Linux and most of the popular 32 bit RTOS
- 6-stage pipeline
- Operation frequency: 133 MHz
- Supports MMU function which includes 32 TLB entries

n MAC Controller

- Supports two-port 10/100 Fast Ethernet MAC
- IEEE 802.3u MII interface
- IEEE 802.3x flow control in full-duplex mode
- Descriptor architecture for packet TX/RX

n Interrupt Controller

- Provides two 8259 compatible interrupt controllers which are cascaded internally
- Independent programmable level/edge-triggered interrupt channels
- Serial IRQ supported

n DMA Controller

- Provides two 8237 DMA compatible controllers which are cascaded internally
- 4 channels for 8-bit DMA transfer and 3 channels for 16 bit transfer

n Two USB 2.0 Host Port Support

- Supports HS, FS and LS

n FIFO UART Port

- A high performance UART port with transmit and receive FIFOs
- Supports the programmable baud rate generator with the data rates from 50 to 115,200 bps
- The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits

n PCI Control Interface

- Supports PCI Rev 2.1 specification
- 32-bit bus interface
- Supports PCI clock at 33 MHz
- Supports PCI host
- Supports PCI master/ slave
- Up to 133 Mbytes / Sec. maximum bandwidth
- Supports up to 3 external master devices on PCI
- Provides four PCI interrupt channels

n LPC (Low Pin Count) Bus Interface

- LPC revision 1.0 compliant
- Supports LPC/FWH (Firmware Hub) compliant interfaces
- Provides the interface to connect an LPC/FWH Flash ROM or Super I/O chip
- Supports LPC DMA
- Supports serial IRQ
- Supports 8/16/32-bit transfer size
- Supports bus master request in DMA channel 4

n X-Bus Interface

- Provides the interface to boot ROM BIOS & DOC (Disk On Chip).
- Supports 8/16 bit data width
- Provides ROMCS_n for booting from X-bus Flash ROM
- Supports from 64K byte to max 16M byte ROM space addressing
- Supports two independent and programmable CSs (Chip Selects)

n SDRAM Control Interface

- PC100/ PC133 compliant
- Supports 16-bit data bus width
- Supports speeds up to 133 MHz and above
- Supports maximum 128 MB memory space

n On-Chip L1 16KB Cache

- Unified instructions and data cache
- Supports write through for cache write policy
- Snooping mechanism support for data coherence between main memory and cache
- Direct map

n General Programmable I / O

- Supports 58 programmable I/ O pins

- Each GPIO pin can be individually configured to be an input/output pin

n Counter / Timers

- 8254 compatible timers
- Provides three independent programmable timers / counters
- Supports a watchdog timer (WDT)
- Supports a speaker output

n Real Time Clock (External)

- Provides a direct interface to external RTC chips

n Operating Voltage Range

- Core voltage : 1.8 V ± 5%
- I / O voltage : 3.3 V ± 10%

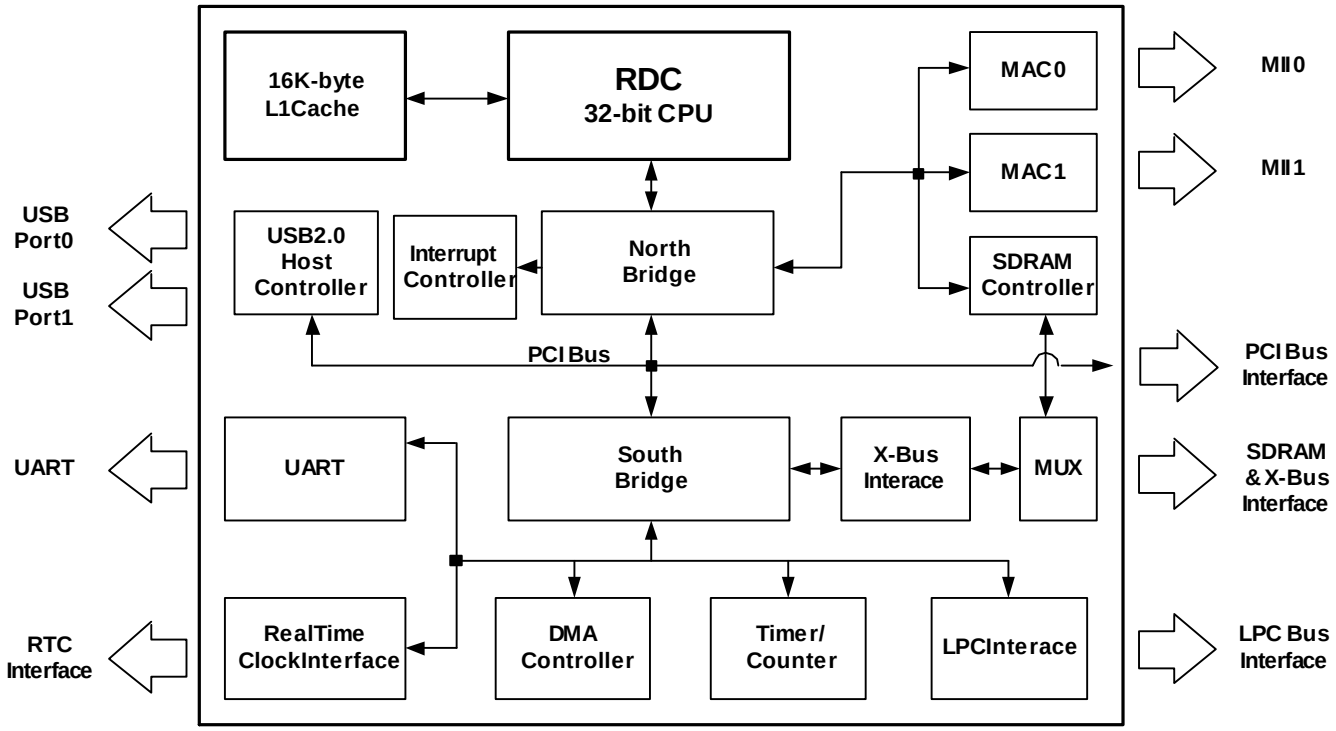
n Operating Temperature: 0 ~ +70°C

n Package Type

- 24mm x 24mm, 216- pin LQFP
- 13mm x 13mm, 225 -pin LFBGA

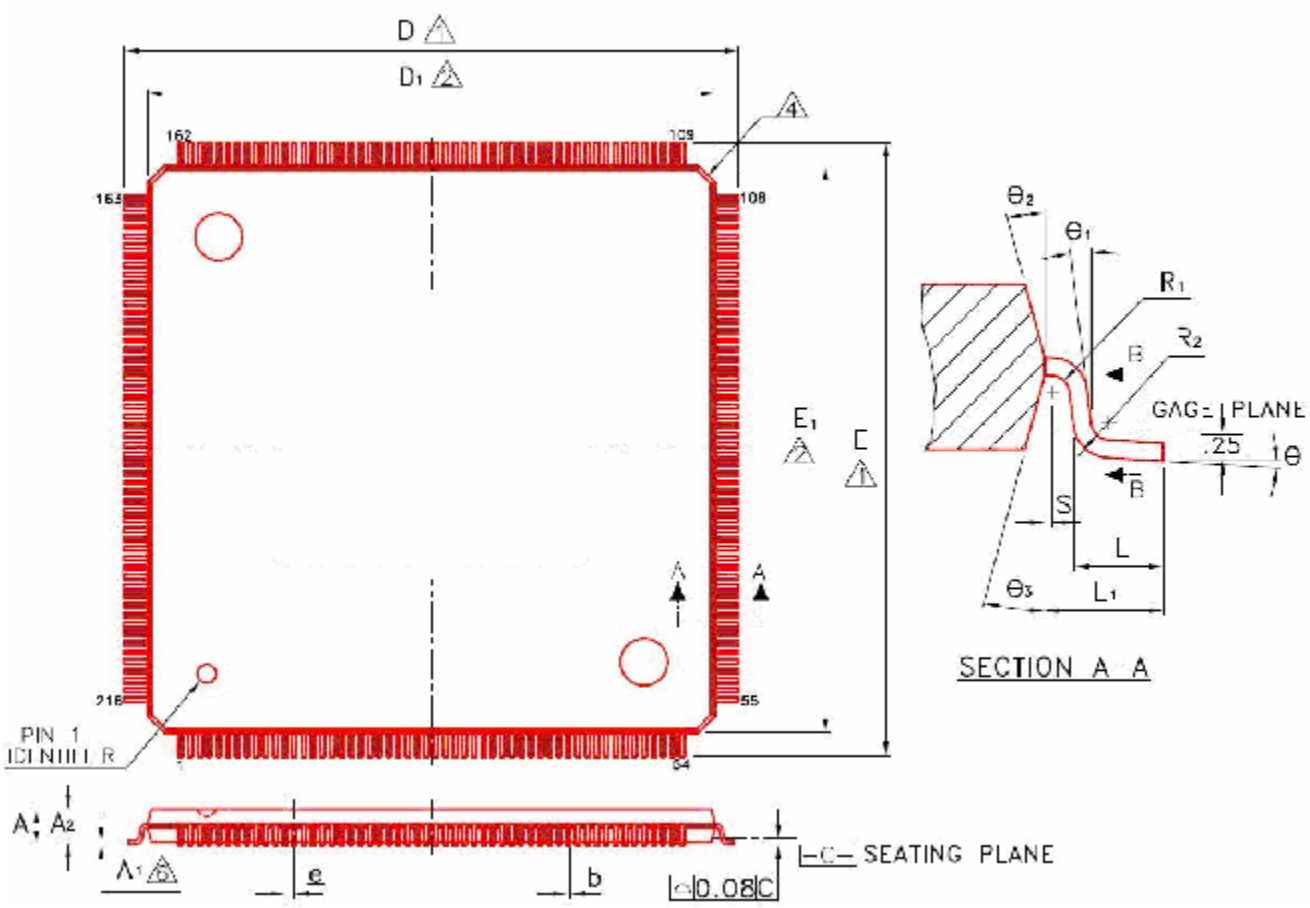
n RoHS Compliant

2. Block Diagram



4. Package Information

LQFP: 216 pins



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	--	--	1.60
A_1	0.05	--	0.15
A_2	1.35	1.40	1.45
b	0.13	0.18	0.23
D	25.85	26.00	26.15
D_1	23.90	24.00	24.10
E	25.85	26.00	26.15
E_1	23.90	24.00	24.10
e	0.40 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	--	--
R_2	0.08	--	--
S	0.20	--	--
Θ	0°	3.5°	7°
$Θ_1$	0°	--	--
$Θ_2$	11°	12°	13°
$Θ_3$	11°	12°	13°

LFBGA 225 balls