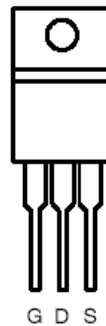


N-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

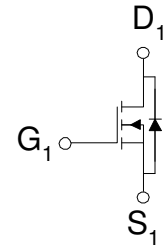
- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TO-220 saves board space
- Fast switching speed
- High performance trench technology

TO-220AB



Top View

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
100	16 @ $V_{GS} = 10V$	90 ^a
	19 @ $V_{GS} = 4.5V$	



N-Channel MOSFET

DRAIN connected to TAB

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25^\circ\text{C}$	I_D	90	A
Pulsed Drain Current ^b		I_{DM}	240	
Continuous Source Current (Diode Conduction) ^a		I_S	90	A
Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	300	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	0.5	$^\circ\text{C/W}$

Notes

- Package Limited
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	uA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55°C			25	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	120			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 2 A			16	mΩ
		V _{GS} = 4.5 V, I _D = 2 A			19	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 2 A		30		S
Diode Forward Voltage	V _{SD}	I _S = 2 A, V _{GS} = 0 V		1.1		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 90 A		49		nC
Gate-Source Charge	Q _{gs}			9		
Gate-Drain Charge	Q _{gd}			10		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, R _L = 25 Ω , I _D = 34 A, V _{GEN} = 10 V		16		nS
Rise Time	t _r			10		
Turn-Off Delay Time	t _{d(off)}			50		
Fall-Time	t _f			23		

Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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