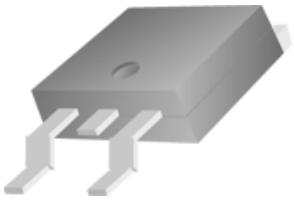
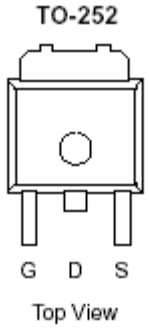
N-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
100	130 @ V_{GS} = 10V	17
	160 @ V_{GS} = 4.5V	15

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Limit**	**Units**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_C=25°C	I_D	17	A
Pulsed Drain Current[b]		I_{DM}	36	
Continuous Source Current (Diode Conduction)[a]		I_S	30	A
Power Dissipation[a]	T_C=25°C	P_D	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	$R_{\theta JA}$	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

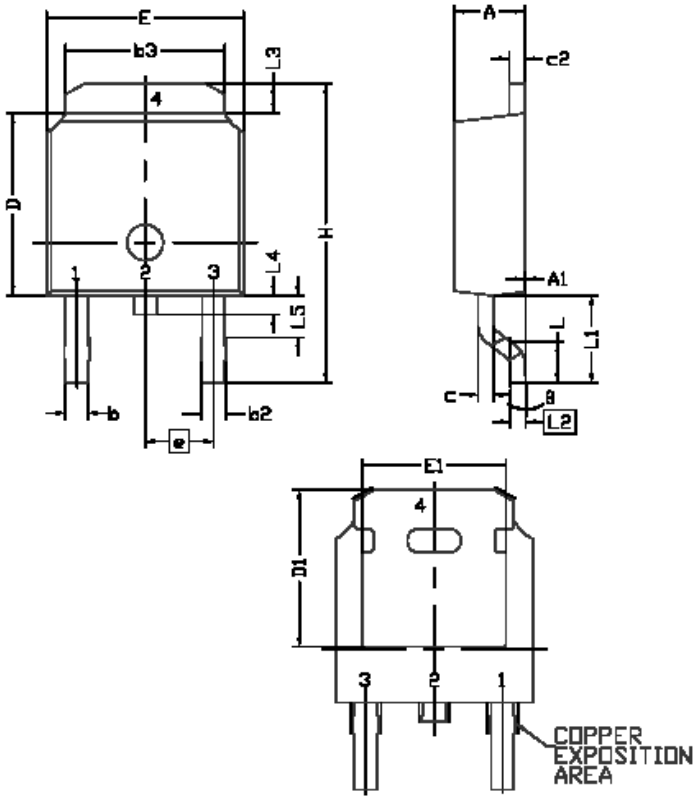
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 uA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	uA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	34			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2 A			130	mΩ
		V_{GS} = 4.5 V, I_D = 2 A			160	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 40 V, I_D = 2 A		4.4		S
Diode Forward Voltage	V_{SD}	I_S = 2 A, V_{GS} = 0 V		1.1		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 2 A		4		nC
Gate-Source Charge	Q_{gs}			1		
Gate-Drain Charge	Q_{gd}			1		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, R_L = 25 Ω , I_D = 9 A, V_{GEN} = 10 V		2		nS
Rise Time	t_r			3		
Turn-Off Delay Time	$t_{d(off)}$			11		
Fall-Time	t_f			5		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	---	1.27
L4	0.64	---	1.01
L5	---	---	---
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	---	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.30	---	---
E1	4.40	---	---
θ	0°	---	10°