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SL1466

Wideband PLL FM Demodulator

Preliminary Information

DS 3979 2.2 August 1997

The SL1466 is a wideband PLL FM demodulator, intended primarily for application in satellite tuners.

The device contains all elements necessary, with the exception of external local oscillator tank and loop filter components, to form a complete PLL system operating at 403 or 480MHz.

An AFC system is provided, whose output signals can be used to correct for any frequency drift at the head end local oscillator.

FEATURES

- Single chip PLL system for wideband FM demodulation
- Simple low component count application
- Fully balanced low radiation design
- High operating input sensitivity
- 2 stage AGC detect for control over internal and external AGC stages
- Low distortion video output drive
- Video polarity invert
- Digital AFC with window adjust
- ESD protection (Normal ESD handling procedures should be observed)

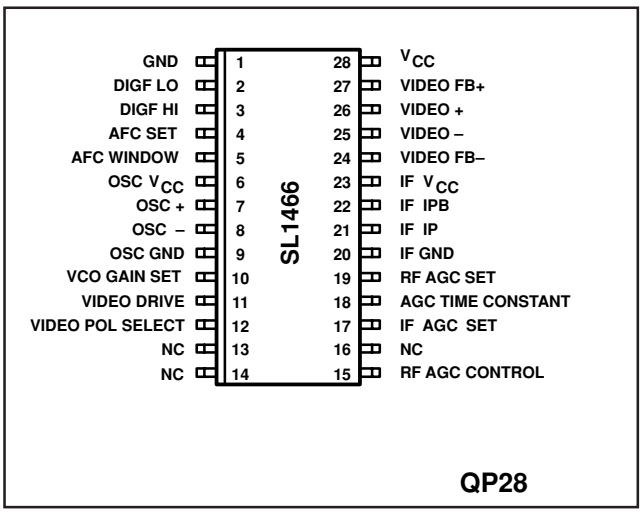


Fig.1 Pin connections - top view

APPLICATIONS

- Satellite receiver systems
- Data communications systems

ORDERING INFORMATION

SL1466/KG/QP1S

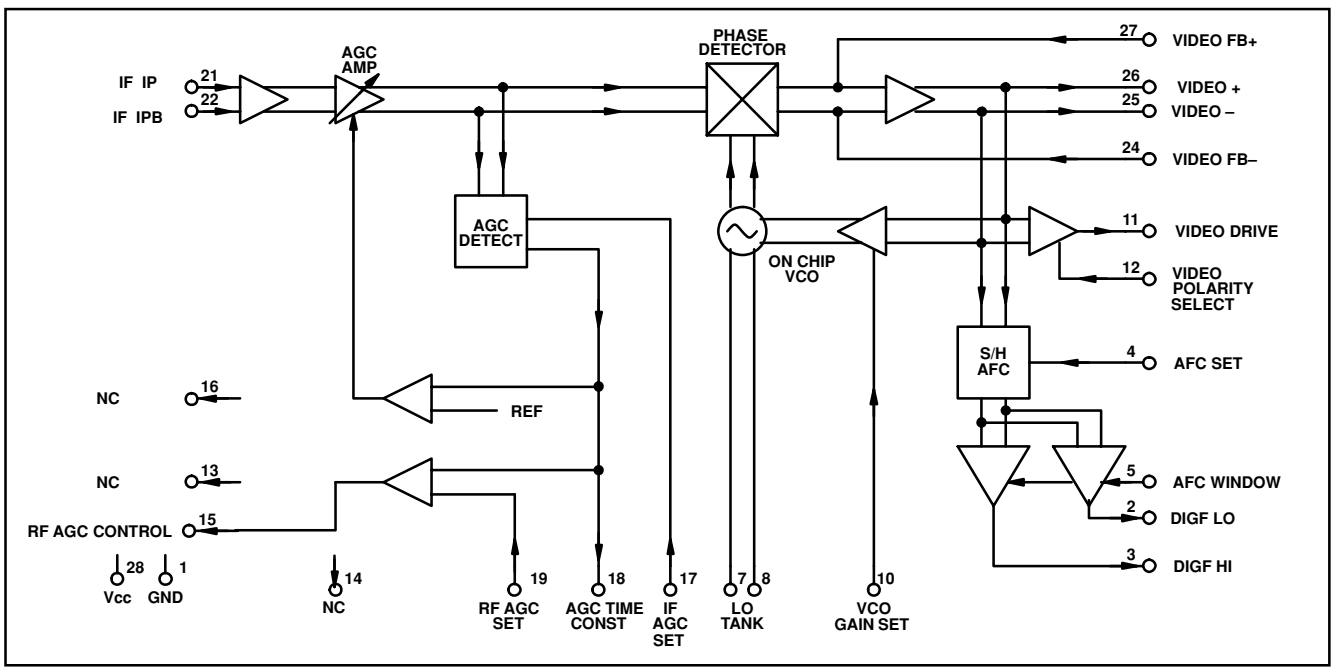


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

T_{AMB} = -20°C to +80°C, V_{CC} = +4.75 to +5.25V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current, Icc	6,23,28		65		mA	
RF Section						
Operating frequency	21, 22		480		MHz	
Input sensitivity	21, 22		-60		dBm	At 27°C
Input overload	21, 22	0	-7		dBm	
Input Impedance	21, 22		75		Ω	
Internal AGC AMP range		50			dB	
VCO Section						
VCO dF/dV (K_o)	10		54		MHz/V	
VCO supply sensitivity	6,7,8,9		1.0		MHz/V	At 27°C
VCO temperature sensitivity	7,8		0.05		MHz/°C	0-55°C, V_{CC}=5V, 750ppmNTC, 0.5pF tuning cap.
Video section						
Phase detector gain (K_d)			0.5		V/rad	Differential loop filter
Loop amplifier input impedance			570		Ω	R1 in note on loop parameters
Video drive output swing	11		0.9		Vp-p	Into 75Ω, 18MHz frequency deviation
	11		1.8		Vp-p	Into 1KΩ, 18MHz frequency deviation
Video drive output Impedance	11		100		Ω	At 27°C
Video drive luminance						
non - linearity	11		2		%	75Ω load
Differential gain	11		±2		%	75Ω load
Differential phase	11		±2		Deg	75Ω load
Tilt	11		1.0		%	75Ω load
Base line distortion	11			0.5	dB	75Ω load
Intermodulation	11		-46	-40	dB	75Ω load, see note 1
Signal/noise	11		58		dB	75Ω load, see note 2
Video polarity select input Low	12			V_{EE}	V	Negative polarity
Video polarity select input High	12	V_{CC}			V	Positive polarity
Video polarity switch leakage current	12			10	µA	V_{CC}=5.25V V_{in}=0V
Video polarity switch leakage current	12			10	µA	V_{CC}=5.25V V_{in}=5.25V
Positive to negative video gain balance	11			1	dB	
AFC section						
AFC window minimum widths			0.44		MHz	Deadband measured at 90% of AFC high voltage
AFC output high voltage	2,3	V_{CC}-0.4		V_{CC}	V	
AFC output low voltage	2,3	0		0.4	V	

NOTE:
1. Product of input modulation f_1 at 4.43MHz p-p deviation and f_2 at 6MHz, 2MHz p-p deviation, (PAL chroma and sound subcarriers).
2. Ratio of luminance bar amplitude (100% white), 13.5MHz p-p deviation, to output rms noise in 6MHz bandwidth with no input modulation.
3. The above characteristics were measured in the Application circuit shown in Fig.10, with an input power of -50dBm and f(RFIN) =480MHz, unless otherwise stated.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} at 0V

Characteristic	Min	Max	Units	Conditions
Supply voltage	-0.3	7	V	
RF input voltage		2.5	Vp-p	
Storage temperature	-55	125	°C	
Junction temperature		150	°C	
QP 28 package thermal resistant, chip to ambient		93	°C/W	
QP 28 package thermal resistance, chip to case		34	°C/W	
ESD protection	2		kV	Mil std 883B method 30115 cat 1.

PIN DESCRIPTION

PIN NO	PIN NAME	DESCRIPTION (Note units are MHz, Amps and Volts)
1	GND	Chip ground
2	DIGFLO	Flag = high when F (local oscillator) < F (IFIN) - F (WINDOW)/2
3	DIGFHI	Flag = high when F (local oscillator) >F (IFIN) + F (WINDOW)/2
4	AFCSET	Connected to V_{CC}
5	AFCWINDOW	Control input current sink sets width of AFCWINDOW F =2250 K_o x I where I is the AFCWINDOW current F is the window width and K_o is the VCO gain
6	OSC V_{CC}	Oscillator V_{CC}
7	OSC+	External tank
8	OSC-	External tank
9	OSC GND	Oscillator ground
10	VCO GAIN SET	Control voltage input to set VCO GAIN. Connect to V_{CC}
11	VIDEO DRIVE	Video output (1KΩ, 1.8V p-p)
12	VIDEO POL SELECT	Control voltage input to set Video polarity. 0 Volts = inverted, 5 Volt = normal
13	NC	
14	NC	
15	RF AGC CONTROL	Control output current to tuner AGC control port. See Fig. 4.
16	NC	
17	IF AGC SET	Connect to V_{CC} via 6k8 Ohm resistor
18	AGC TIME CONSTANT	Control input current source. Pulse at carrier frequency F(IFIN) with mark/space proportional to applied device AGC gain. Use external R-C to set time constant. 47K, 100nF

PIN DESCRIPTION

PIN NO	PIN NAME	DESCRIPTION (Note units are MHz, Amps and Volts)
19	RF AGC SET	Connect to V_{CC} via 1.8K resistor
20	IF GND	IF stage ground
21	IF IP	IF input (preferred input for single ended use)
22	IF IPB	IF input
23	IF V_{CC}	IF stage V_{CC}
24	VIDEO FB-	Loop amp negative input. Connected to VIDEO + via loop network
25	VIDEO-	Loop amp negative output
26	VIDEO+	Loop amp positive output
27	VIDEO FB+	Loop amp positive input. Connected to VIDEO- via loop network
28	V_{CC}	Chip V_{CC}

FUNCTIONAL DESCRIPTION

The SL1466 is a wideband PLL FM demodulator, optimised for application in satellite receiver systems and requiring a minimal external component count. It contains all the elements required for the construction of a phase locked loop circuit, with the exception of tuning components for the local oscillator. Also included is an AFC detector circuit for generation of error signals to correct for any frequency drift in the outdoor unit local oscillator. A block diagram is shown in Fig. 2 and a typical application in Fig. 6.

The internal pin connections are shown in Fig. 1.

In normal applications the second satellite IF of typically 403.2 or 479.5 MHz is fed to the RF preamplifier, which contains a two stage level detect circuit. This generates two AGC signals, one of which controls the gain of the internal IF amplifier stage and one which can be used for controlling the gain of an external RF preamplifier so maintaining a fixed level to the input of the phase detector for optimum threshold, performance. The typical AGC curves are shown in Fig. 4.

The output of the preamplifier is fed to the mixer section which is of a balanced design for low radiation. In this stage the IF signal is mixed with the local oscillator signal, which is generated by an on board oscillator.

The oscillator is tuned internally, requiring only an external fixed LC tank and is optimised for high linearity over the normal deviation range. Typical frequency versus video drive voltage response for the oscillator is shown in Fig. 8. This response was measured with a modulated carrier. The compensated oscillator temperature stability is typically 0.05MHz/°C.

The gain of the oscillator is nominally Ko = 54MHz/Volt.

Note: Because there is a x3 amplifier in the video output section, the overall chip gain (MHz/V) is one third of the VCO gain or18MHz/Volt. The gain may be set accurately by means of potential divider connected to Pin 10. (+4.5V)

The output of the mixer is then fed to the loop amplifier around which feedback is applied to determine loop amplifier transfer characteristics. The output of the loop amplifier is referenced so as to eliminate V_{CC} dependence of the VCO.

The loop amplifier drives a buffer amplifier, which can be connected to a 75 Ohm load or a high impedance stage to give greater linearity and approximately 6dB higher demodulated signal. The video polarity can be inverted depending on the sense of the video polarity select input; open circuit or a resistor to V_{CC} gives positive video whereas a resistor to V_{EE} gives negative video.

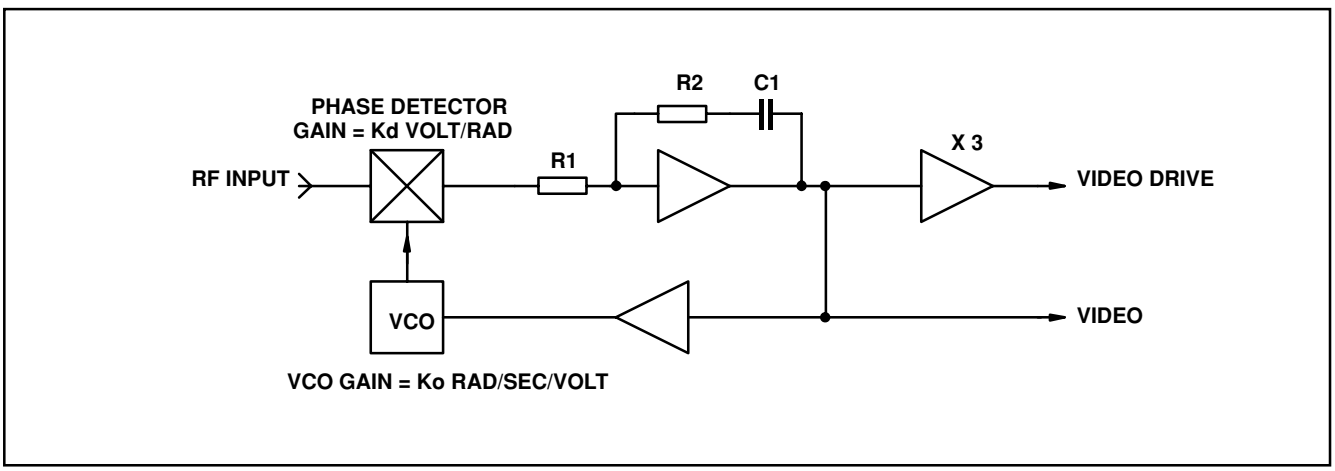


Fig. 3 Design of PLL loop parameters

The SL1466 is normally used as a type 2 second order loop and can be represented by the above diagram. for such a system the following loop parameters apply.

$T_1 = C1\ R1$
$T_2 = C1\ R2$
and
$T_1 = K_o\ K_D/\omega_n^2$
$T_2 = 2\ \xi/\omega_n$

where:

K_O is the VCO gain in radians seconds per volt
K_D is the phase detector gain in volts per radian
ω_n is the natural loop bandwidth
ξ is the loop damping factor

From these factors the loop 3dB bandwidth can be determined from the following expression;

$$\omega_{3dB}^2 = \omega_n^2(2\xi^2 + 1) + \omega_n^2 \sqrt{((2\xi^2 + 1) + 1}$$

which approximates to $\omega_{3dB} = 2\xi\omega_n$, when $\xi >> 1$

N.B. VCO gain within the PLL is three times higher than at the video drive pin due to gain in the output stage.

NOTE: R1 is the loop amplifier input resistor. R2 and C2 are the generic designators for the loop components R7-R9 and C9, C14 on the circuit diagram.

AGC FACILITY

A sophisticated two stage level detect circuit has been provided which will control both internal IF AGC and external tuner AGC amplifiers in order to maintain a fixed level to the input of the phase detector of around –20dBm for optimum threshold performance. The internal AGC amplifier provides 50dB of gain adjust and the external AGC control provides for 15dB of gain adjust, thus covering 65dB of dynamic range at the tuner input.

The RF output current RF AGC CONTROL can be converted to a positive gradient control voltage by an external resistor.

AFC FACILITY

The SL1466 contains a digital frequency error detect circuit, which generates an output consisting of two logic flags, DIGFHI and DIGFLO, dependant on whether the LO frequency is above or below the input frequency. These flags have an overlap region where both are high; this is equivalent to the deadband window.

The function of the AFC outputs is shown in Fig. 7 and the accompanying Table.

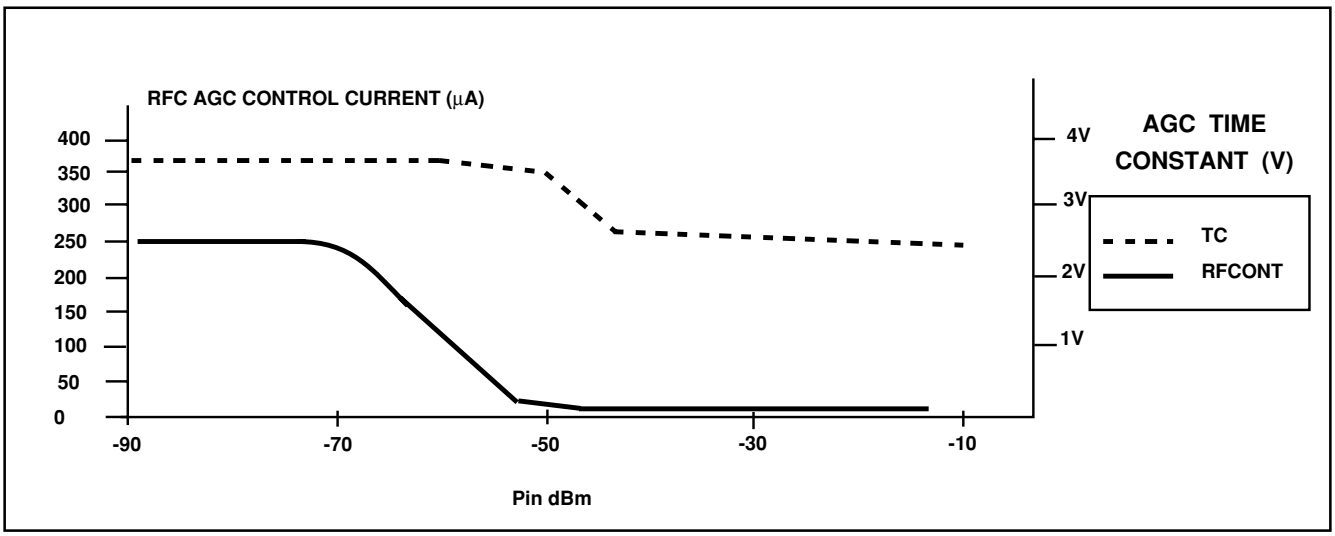


Fig. 4 RF AGC control current and AGC time cinstant voltage vs Input power

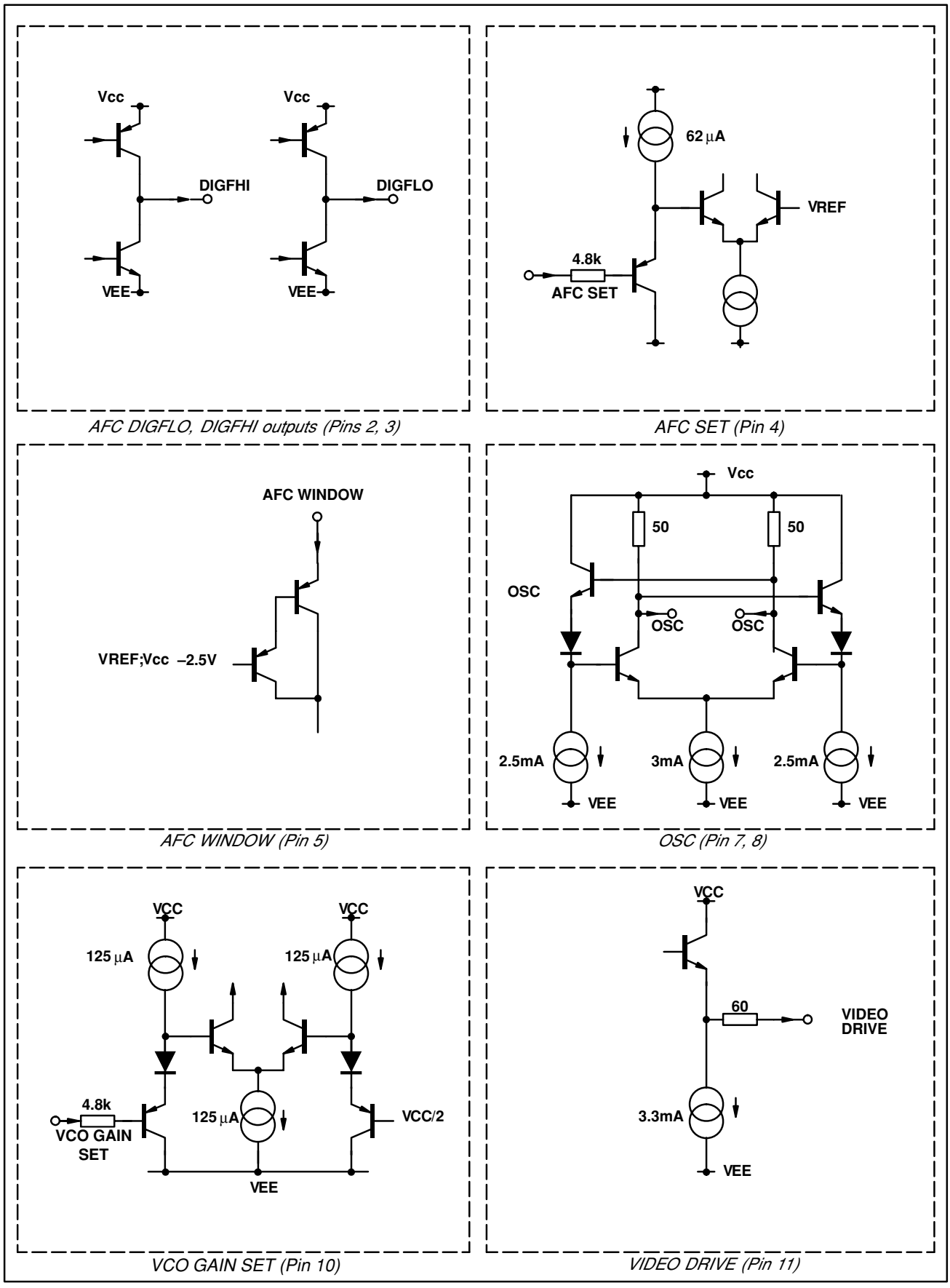


Fig. 5a SL1466 I.O.ports internal circuitry

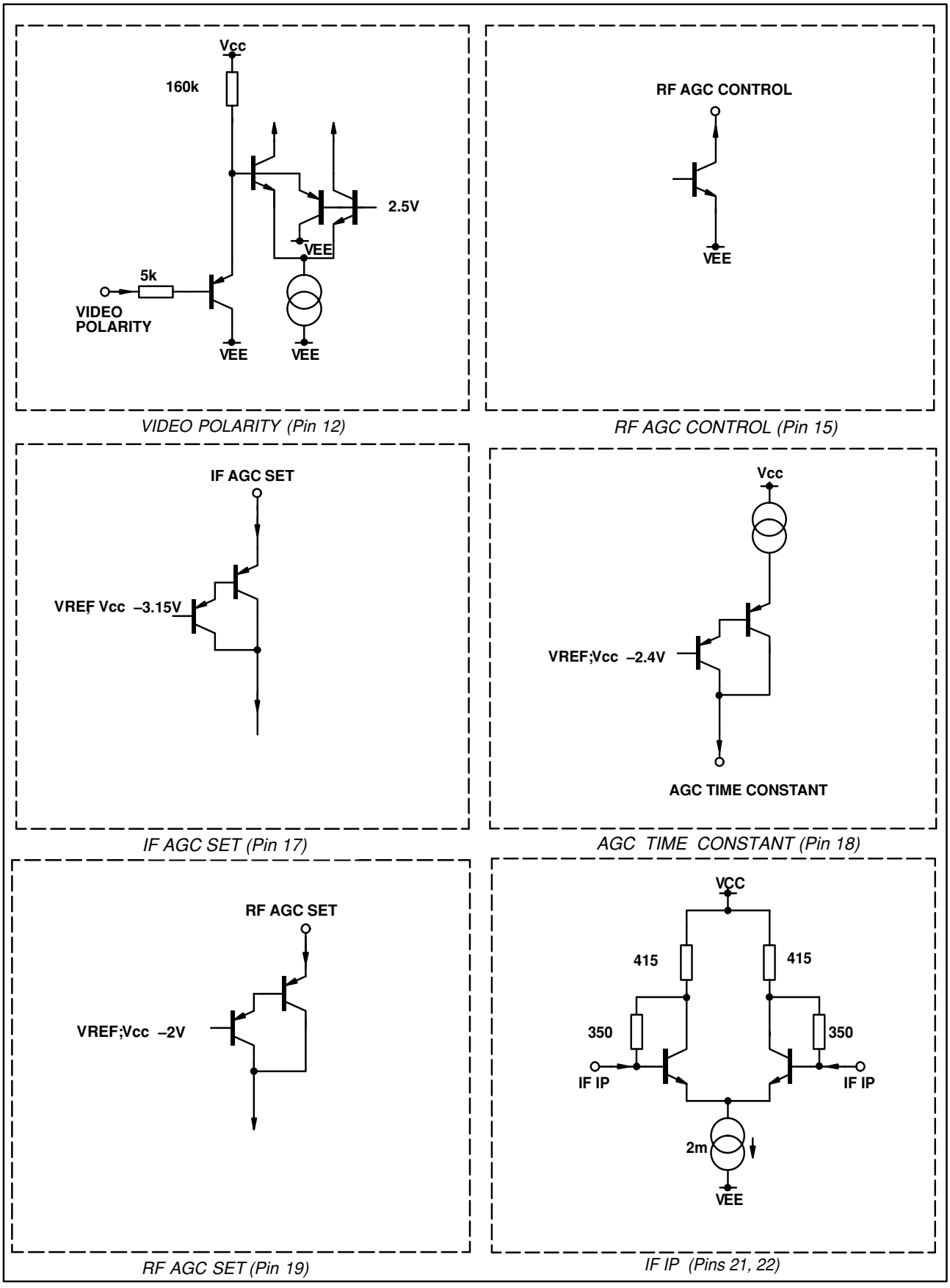


Fig. 5b SL1466 I.O ports internal circuitry

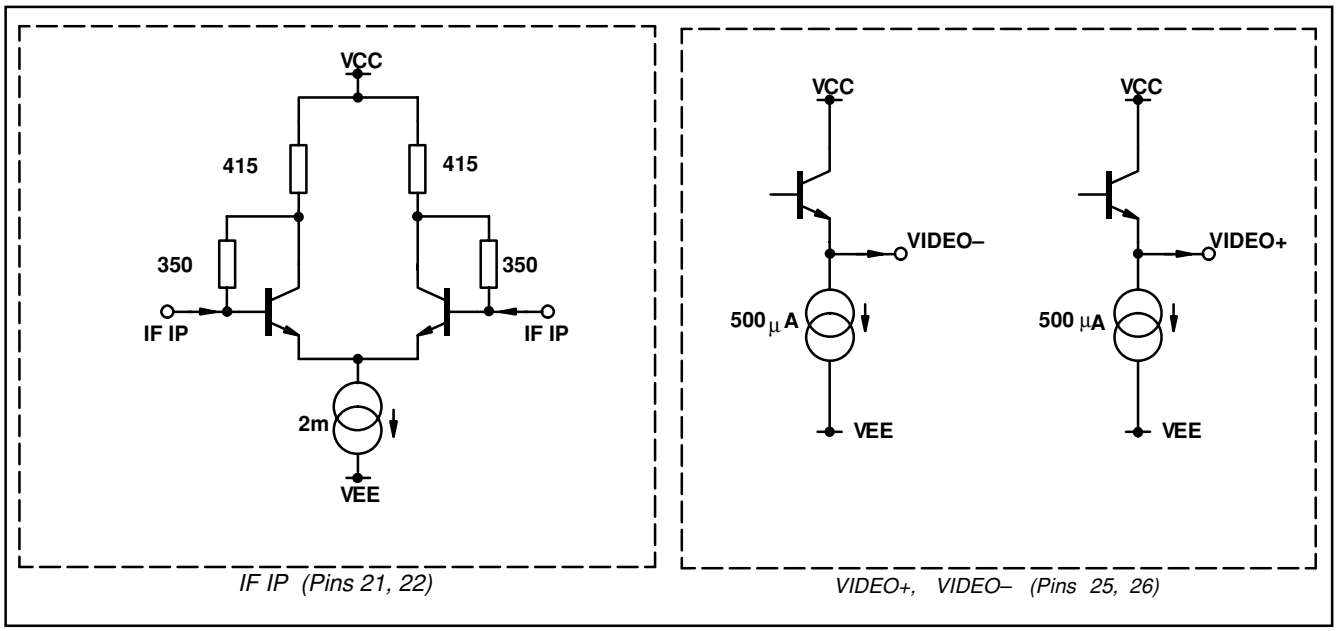


Fig. 5c SL1466 I.O ports internal circuitry

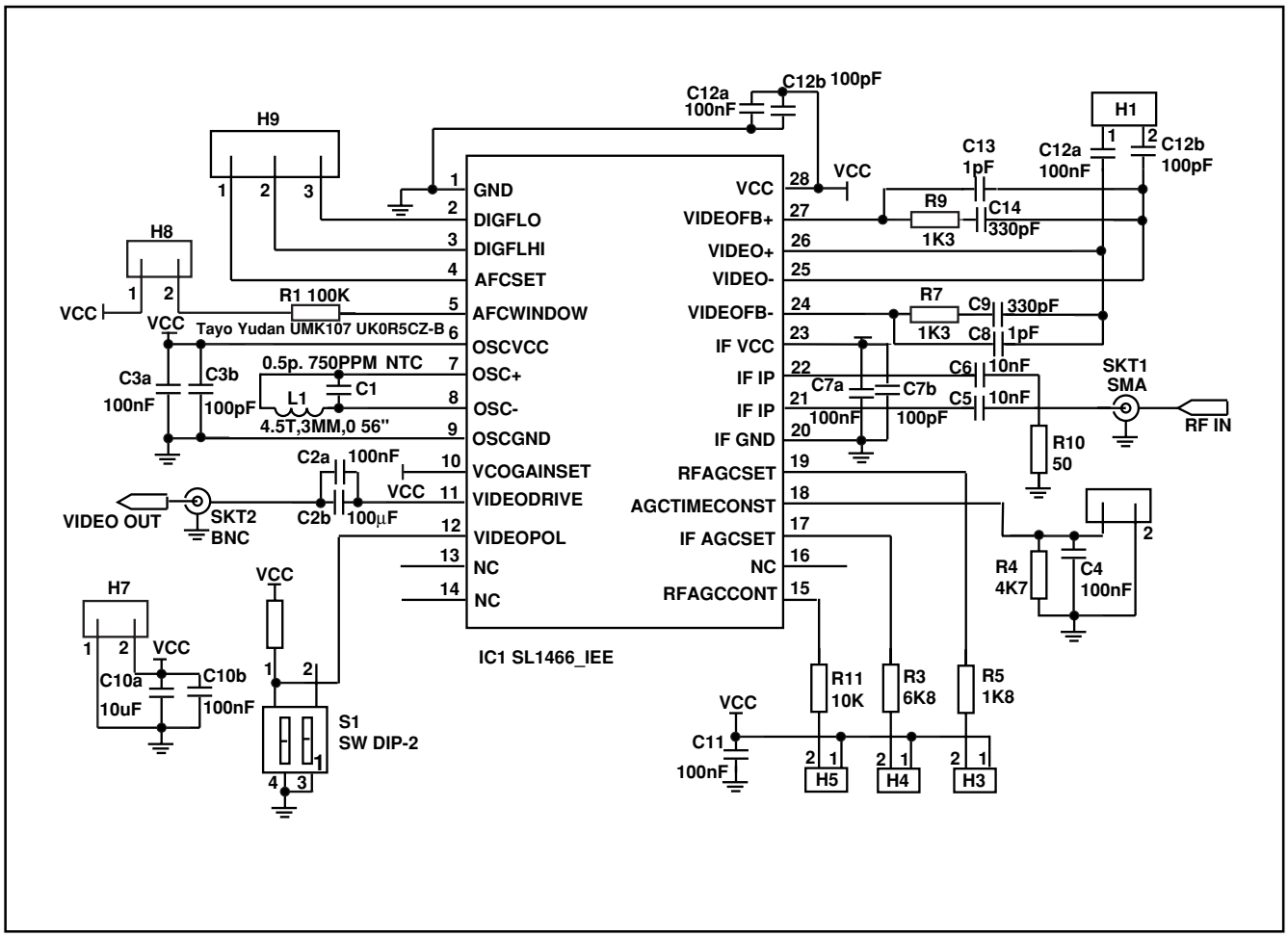


Fig. 6 Typical application circuit.

Note: Loop component values may need re-optimising on Application and VCO gain setting.

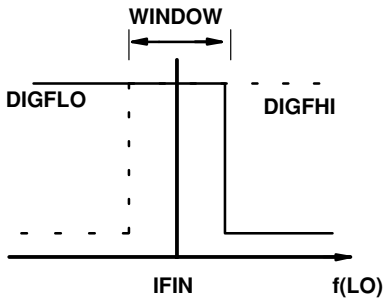


Fig. 7 SL1466 digital AFC output

FREQUENCY ERROR	DIGFLO	DIGFHI
f(LO) Below window	1	0
f(LO) Within window	1	1
f(LO) Above window	0	1

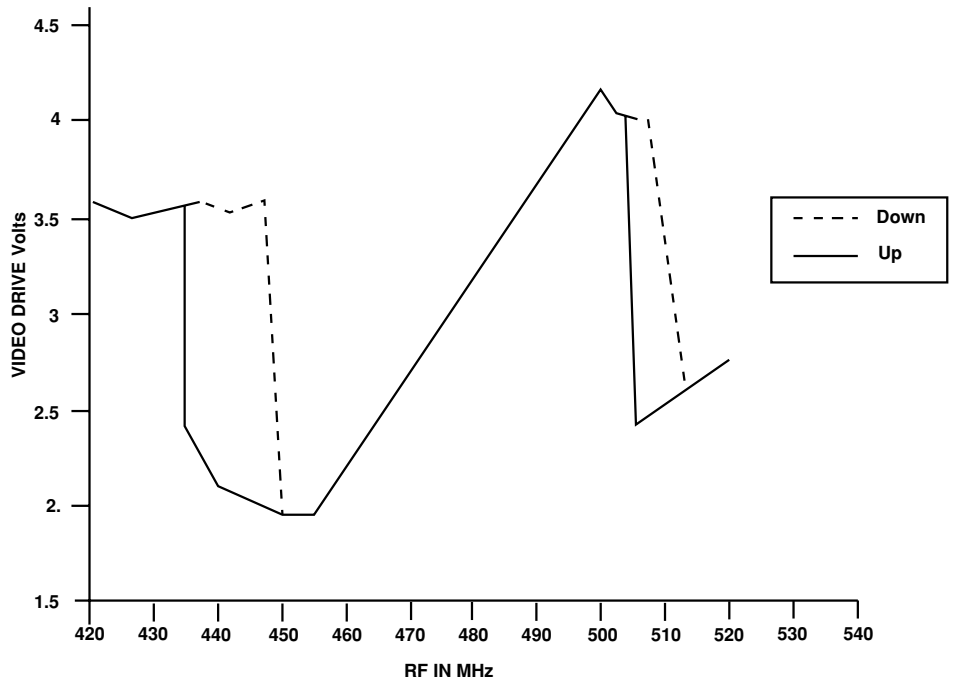


Fig.8 VCO performance (S curve characteristics)

APPLICATION NOTES

Tuning procedure

The component values shown in the applications circuit Fig. 6 are optimised for operation at an IF of 479.5MHz. The AFC circuit can be used to fine tune the external tank as follows:

With the SL1466 connected as in the test set up Fig. 11 or its equivalent using 75Ω cables. Set the video generator for 1V p-p output. Set the satellite test transmitter for a carrier frequency of 479.5MHz, frequency deviation 13.5MHz, power level -30dBm. Turn on the pre-emphasis filter.

Monitor the voltage levels on Pin 2 (DIGFLO) and Pin 3 (DIGFHI).

Adjust the tank coil by squeezing it slightly until the signal on both Pins goes high (i.e. > Vcc –0.4 Volts).

These Pins remain high provided the LO frequency is tuned to within the AFC WINDOW aperture,(± 0.22MHz).

Optimising the loop components

The network connected from Pin 26 (VIDEO+) to Pin 24 (VIDEOFB–) and from Pin 25 (VIDEO–) to Pin 27 (VIDEO FB+) forms the loop filter.

The components shown are based on a natural frequency fn of 2.46MHz ($\omega_n = 2x\,\pi\,x2.46$ Mrads/s) and damping factor ξ =2.6, and assuming Ko = 54MHz/V.

The closed loop gain of the receiver (i.e. the ratio of the output amplitude to the input carrier frequency variation versus frequency) has a low pass filter characteristic. Its roll off is determined by the natural frequency whilst its in band flatness is determined by the damping factor. Both factors will affect the 3dB bandwidth as discussed earlier. A narrow bandwidth will cause loss of high frequency resolution whilst a large bandwidth will degrade the overall signal/noise in the output waveform. Thus a selection procedure might be as follows:

■ Calculate R7 (R9) and C9 (C14) based on f n = 2.46MHz, ξ =2.6 and connect as in Fig. 5.

■ Set the video generator for 1Vp–p composite video and the test generator for a carrier frequency of 479.5MHz, frequency deviation of 13.5MHz and power level –30dBm.

■ Turn on the pre–emphasis filter. Use the 15kHz test pattern to give black/white screen.

■ Monitor the video analyser or TV set.

■ Adjust the de–emphasis filter until the bar amplitude is 1Vp–p or 0% error. Reduce transmitter power level until sparklies or streaking appear.

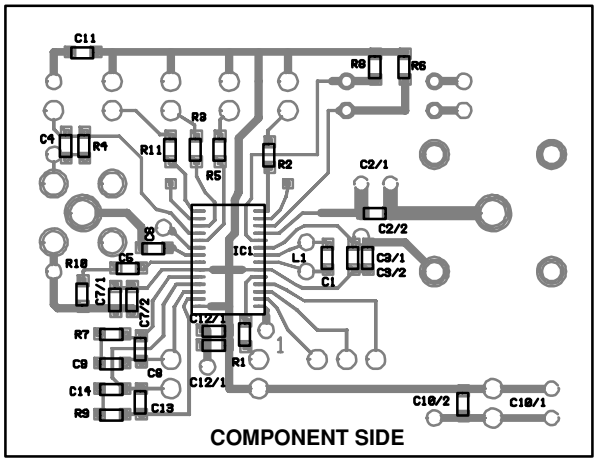
■ Adjust component values for minimum power level when streaking and sparklies occur together.

AGC settings

The signal level at the input to the limiter preceding the phase detector is maintained at an level of around –20dBm or more by an internal (device) AGC and an external (tuner) AGC circuit.

Current pulses at the carrier frequency with mark/space proportional to this input power are sourced out of pin 18 (AGC TIME CONSTANT). These are smoothed and turned into a voltage by the external components R4, C4. The time constant R4 C4 should be adjusted so that the expected signal fading rate can be tracked but its value is not critical, 5mSec typically.

Fig. 4 shows a typical external AGC control curve. Also shown is the AGCTIMECONST voltage which is an indication of the level of internal AGC gain being applied, (the control range is the flat part of the curve).



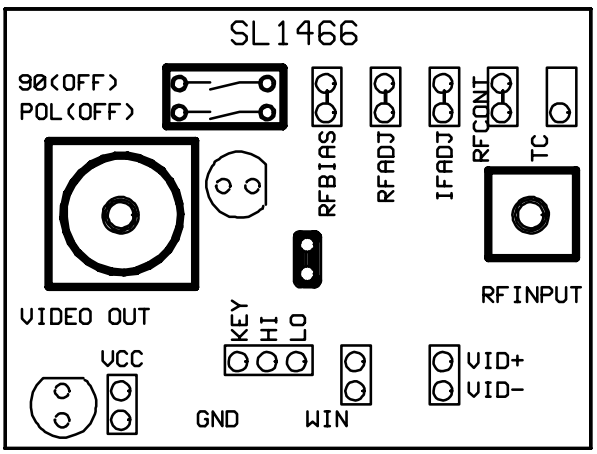


Fig. 9 Test demo PCB

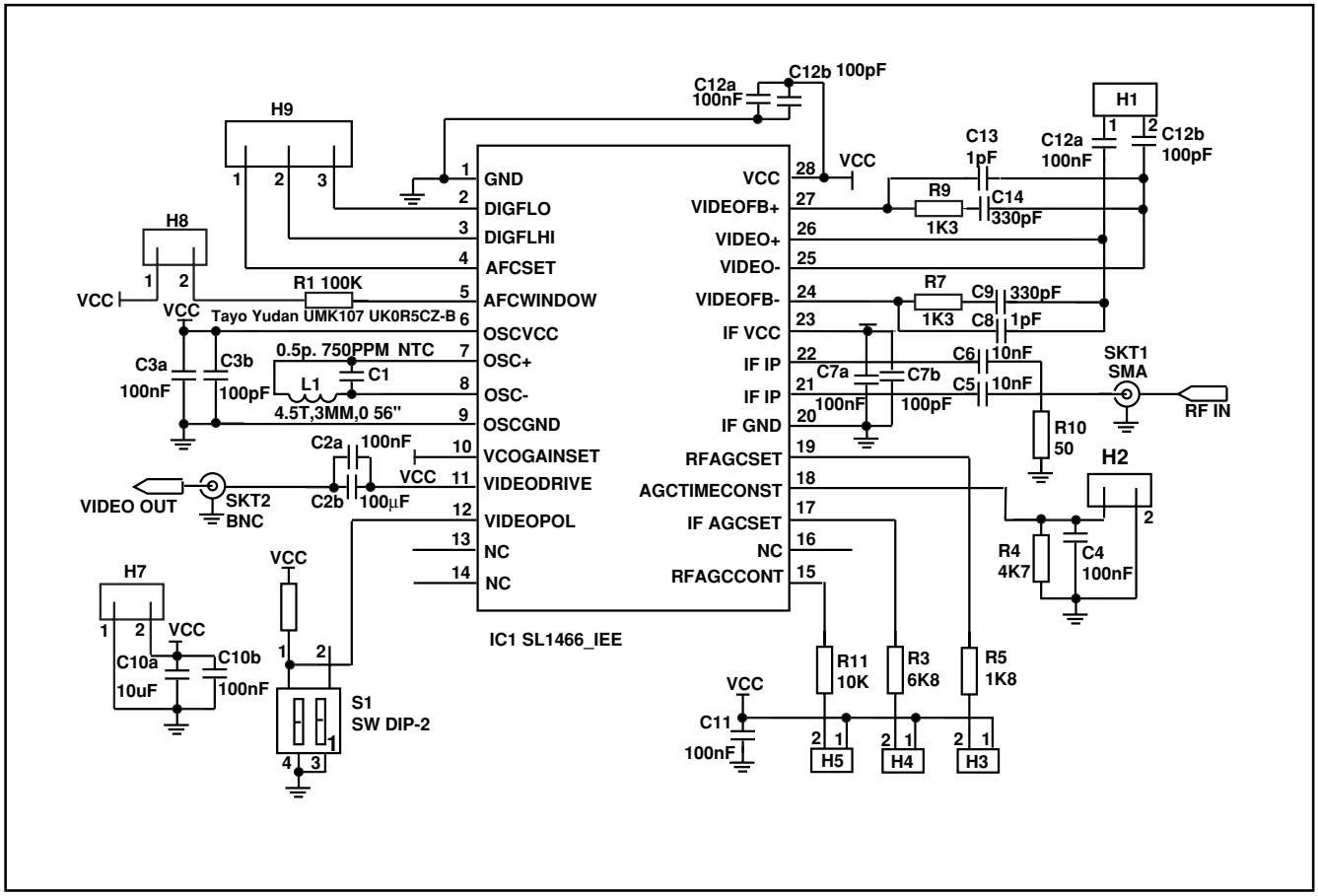


Fig. 10 Test/Demo circuit diagram

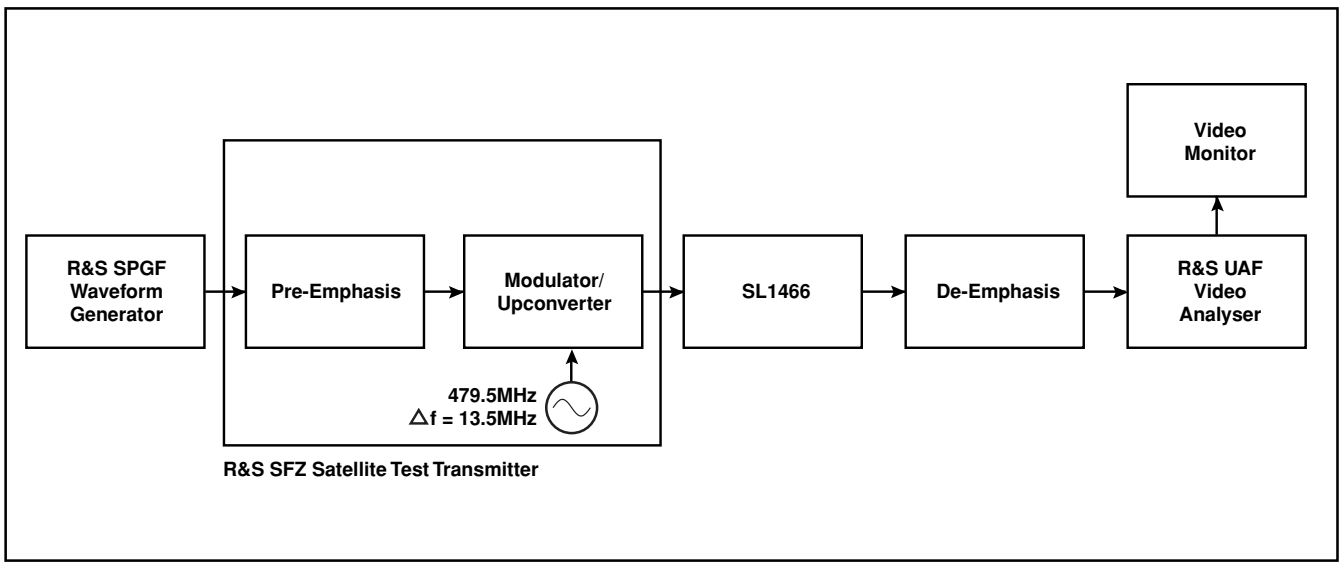
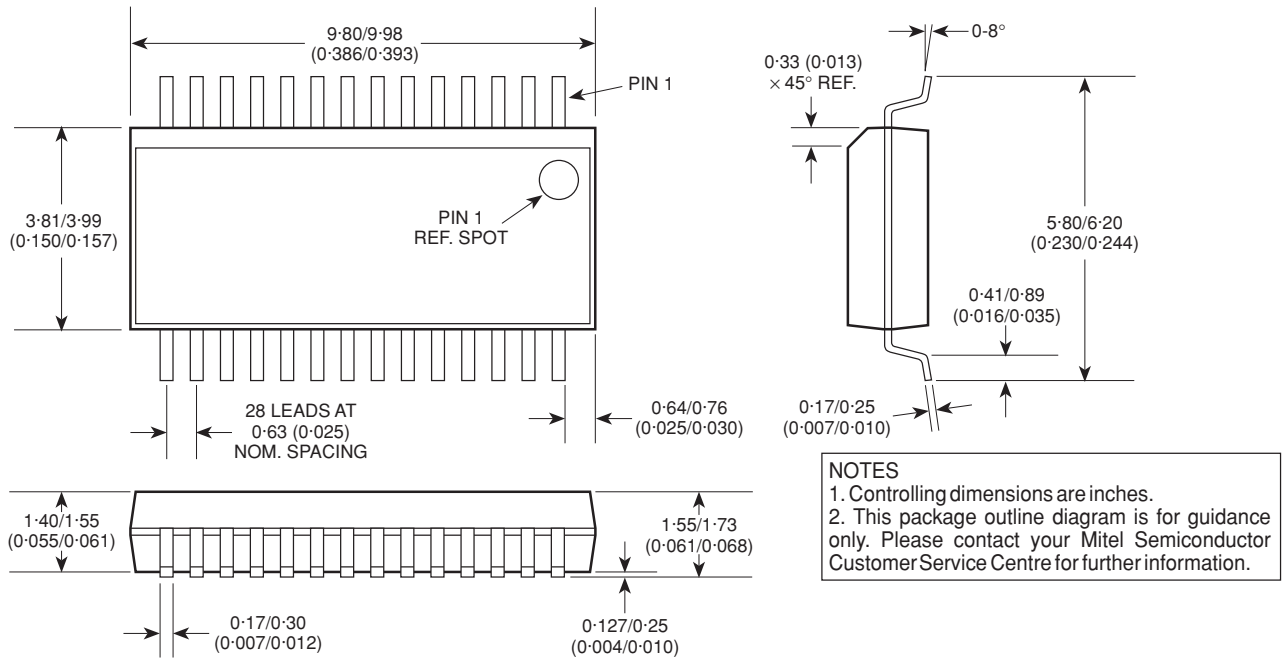


Fig. 11 Test set up

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further information.

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