

**Features**

- Temperature Ranges
  - Industrial: -40 °C to 85 °C
- Very high speed: 55 ns
  - Wide voltage range: 2.20 V – 3.60 V
- Pin-compatible with CY62148CV25, CY62148CV30 and CY62148CV33
- Ultra low active power
  - Typical active current: 1.5 mA at f = 1 MHz
  - Typical active current: 8 mA at f = f<sub>max</sub>(55-ns speed)
- Ultra low standby power
- Easy memory expansion with  $\overline{CE}$ , and  $\overline{OE}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Available in Pb-free 32-pin Small-outline integrated circuit (SOIC package)

**Functional Description<sup>[1]</sup>**

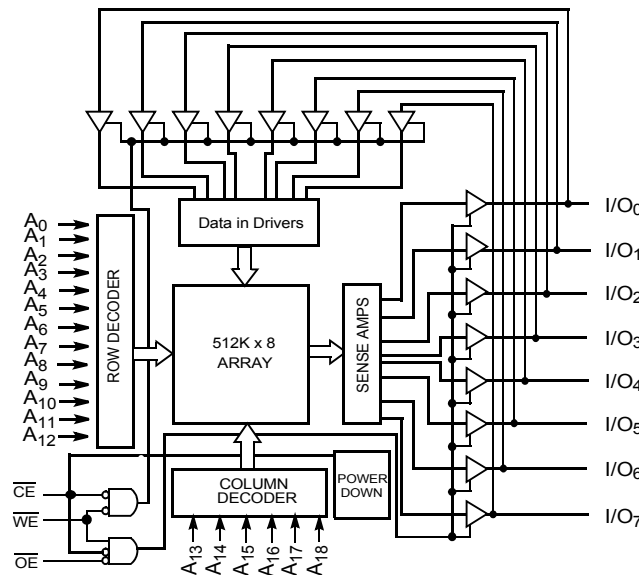
The CY62148DV30 is a high-performance CMOS static RAM organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when deselected ( $\overline{CE}$  HIGH). The eight input and output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- When the write operation is active ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW)

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Read from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

**Logic Block Diagram**



**Note**

1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

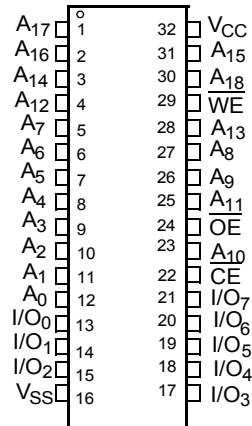
## Contents

<b>Pin Configuration</b> .....	<b>3</b>	<b>Truth Table</b> .....	<b>8</b>
<b>Product Portfolio</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>9</b>
<b>Maximum Ratings</b> .....	<b>4</b>	Ordering Code Definition .....	9
<b>Operating Range</b> .....	<b>4</b>	<b>Package Diagrams</b> .....	<b>10</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>11</b>
<b>Capacitance</b> .....	<b>5</b>	<b>Document Conventions</b> .....	<b>11</b>
<b>Thermal Resistance</b> .....	<b>5</b>	Units of Measure .....	11
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>13</b>
<b>Data Retention Characteristics</b> .....	<b>5</b>	Worldwide Sales and Design Support .....	13
<b>Data Retention Waveform</b> .....	<b>5</b>	<a href="#">Products</a> .....	<a href="#">13</a>
<b>Switching Characteristics</b> .....	<b>6</b>	<a href="#">PSoC Solutions</a> .....	<a href="#">13</a>
<b>Switching Waveforms</b> .....	<b>6</b>		

## Pin Configuration

### 32-pin SOIC Pinout

#### Top View



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		f = 1 MHz		f = f <sub>max</sub>							
		Min	Typ <sup>[2]</sup>	Max		Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62148DV30LL	Industrial	2.2	3.0	3.6	55	1.5	3	8	10	2	8

**Note**

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

(Exceeding maximum ratings may impair the useful life of the device. For user guidelines, not tested.)

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... 55 °C to +125 °C

supply voltage to ground potential ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

DC voltage applied to outputs in High Z state<sup>[3, 4]</sup> ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

DC input voltage<sup>[3, 4]</sup> ..... -0.3 V to  $V_{CC(max)}$  + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001V (per MIL-STD-883, method 3015)

Latch-up current ..... > 200 mA

## Operating Range

Product	Range	Ambient Temperature	$V_{CC}^{[5]}$
CY62148DV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ <sup>[2]</sup>	Max	
$V_{OH}$	Output HIGH voltage	$I_{OH} = -0.1$ mA	$V_{CC} = 2.20$ V	2.0	-	-	V
		$I_{OH} = -1.0$ mA	$V_{CC} = 2.70$ V	2.4	-	-	V
$V_{OL}$	Output LOW voltage	$I_{OL} = 0.1$ mA	$V_{CC} = 2.20$ V	-	-	0.4	V
		$I_{OL} = 2.1$ mA	$V_{CC} = 2.70$ V	-	-	0.4	V
$V_{IH}$	Input HIGH voltage	$V_{CC} = 2.2$ V to 2.7 V		1.8	-	$V_{CC} + 0.3V$	V
		$V_{CC} = 2.7$ V to 3.6 V		2.2	-	$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 2.2$ V to 2.7 V		-0.3	-	0.6	V
		$V_{CC} = 2.7$ V to 3.6 V		-0.3	-	0.8	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$		-1	-	+1	$\mu$ A
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , output disabled		-1	-	+1	$\mu$ A
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$ $I_{OUT} = 0$ mA CMOS levels	-	8	10	mA
		$f = 1$ MHz		-	1.5	3	mA
$I_{SB1}$	Automatic CE Power-down current — CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V) $f = f_{max}$ (address and data only), $f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), $V_{CC} = 3.60$ V		-	2	8	$\mu$ A
$I_{SB2}$	Automatic CE Power-down current — CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = 3.60$ V		-	2	8	$\mu$ A

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100  $\mu$ s ramp time from 0 to  $V_{CC(min)}$  and 200  $\mu$ s wait time after  $V_{CC}$  stabilization.

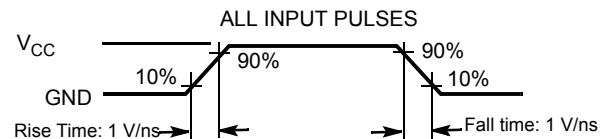
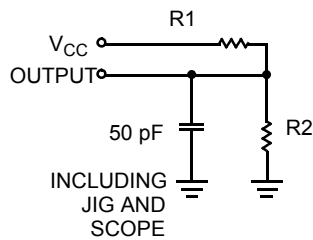
## Capacitance

Parameter <sup>[6]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

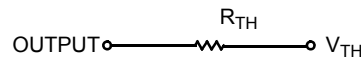
## Thermal Resistance

Parameter <sup>[6]</sup>	Description	Test Conditions	SOIC	Unit
Θ <sub>JA</sub>	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	55	°C/W
Θ <sub>JC</sub>	Thermal resistance (Junction to case)		22	°C/W

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

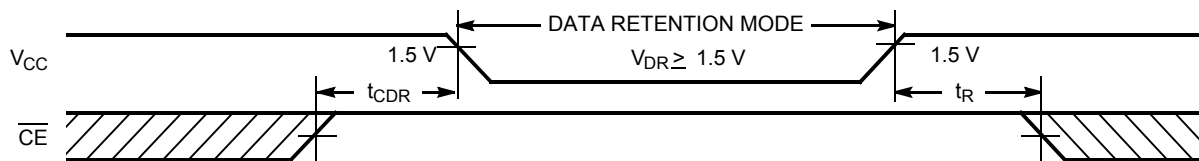


Parameters	2.5 V (2.2 V – 2.7 V)	3.0 V (2.7 V – 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ <sup>[7]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.5	–	–	V
I <sub>CCDR</sub>	Data retention current	V <sub>CC</sub> = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V	–		6	μA
t <sub>CDR</sub> <sup>[6]</sup>	Chip deselect to data retention time		0	–	–	ns
t <sub>R</sub> <sup>[8]</sup>	Operation recovery time		55	–	–	ns

## Data Retention Waveform

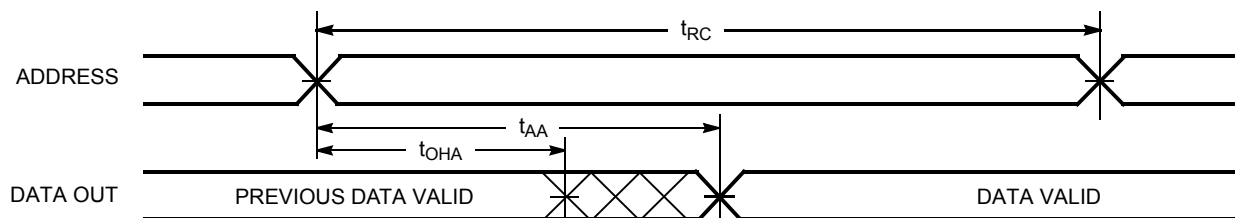


### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C
- Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

**Switching Characteristics** (Over the Operating Range)

Parameter <sup>[9]</sup>	Description	55 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	55	–	ns
$t_{AA}$	Address to data valid	–	55	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low $Z^{[10]}$	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High $Z^{[10,11]}$	–	20	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low $Z^{[10]}$	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High $Z^{[10,11]}$	–	20	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-up	–	55	ns
<b>Write Cycle<sup>[12]</sup></b>				
$t_{WC}$	Write cycle time	55	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	40	–	ns
$t_{AW}$	Address set-up to write end	40	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address set-up to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	40	–	ns
$t_{SD}$	Data set-up to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High $Z^{[10,11]}$	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low $Z^{[10]}$	10	–	ns

**Switching Waveforms**
**Figure 1. Read Cycle No. 1 (Address Transition Controlled)<sup>[13, 14]</sup>**

**Notes**

9. Test Conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the “AC Test Loads and Waveforms” on page 5.
10. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ;  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
11.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
13. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
14.  $\overline{WE}$  is HIGH for read cycle.

Switching Waveforms (continued)

Figure 2. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)<sup>[15, 16]</sup>

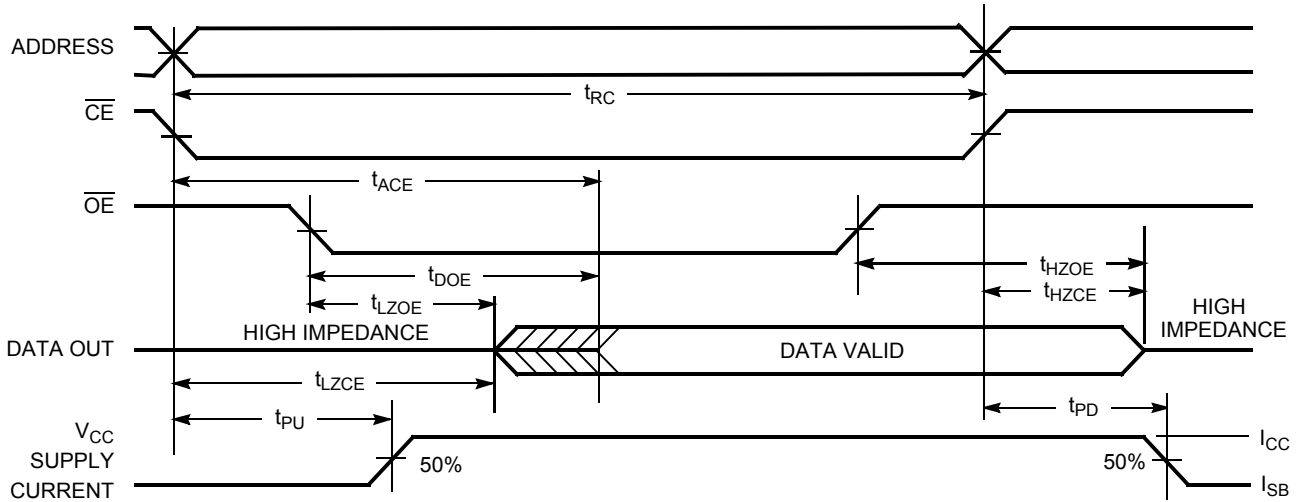
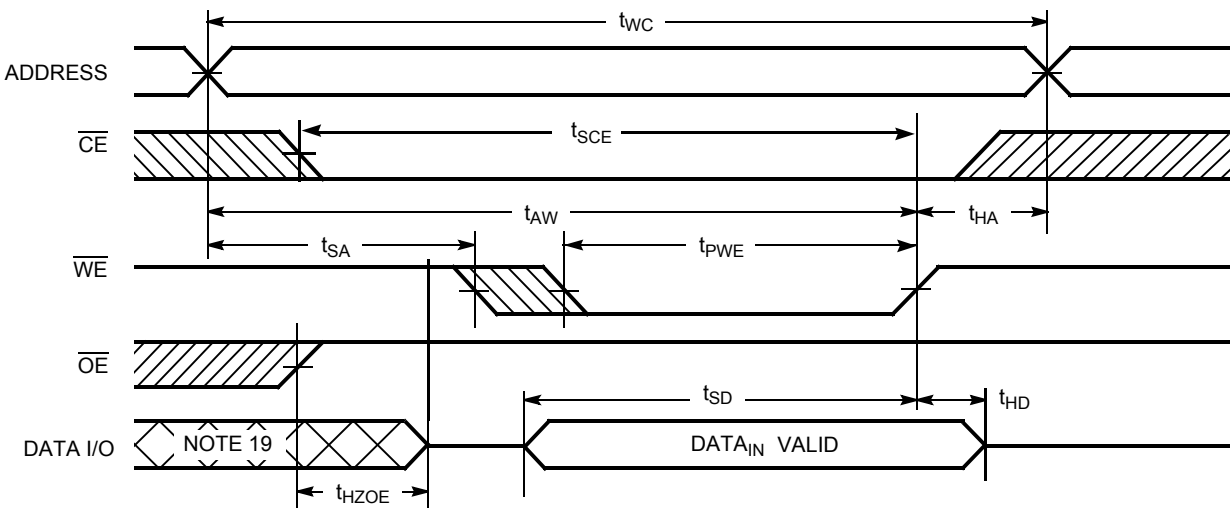


Figure 3. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)<sup>[17, 18]</sup>



Notes

- 15.  $\overline{\text{WE}}$  is HIGH for read cycle.
- 16. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.
- 17. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
- 18. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in high-impedance state.
- 19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 4. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)<sup>[20, 21]</sup>

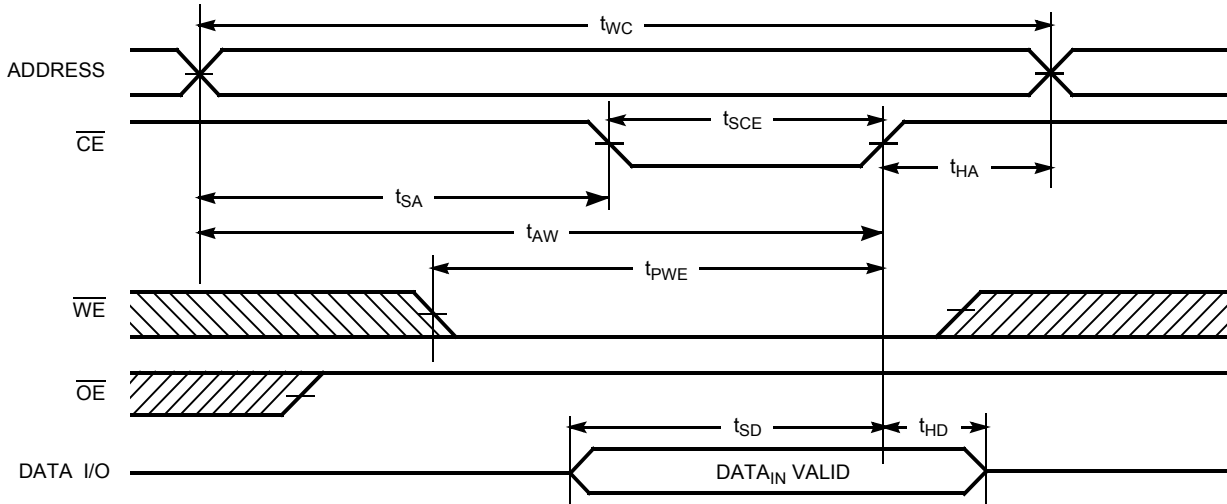
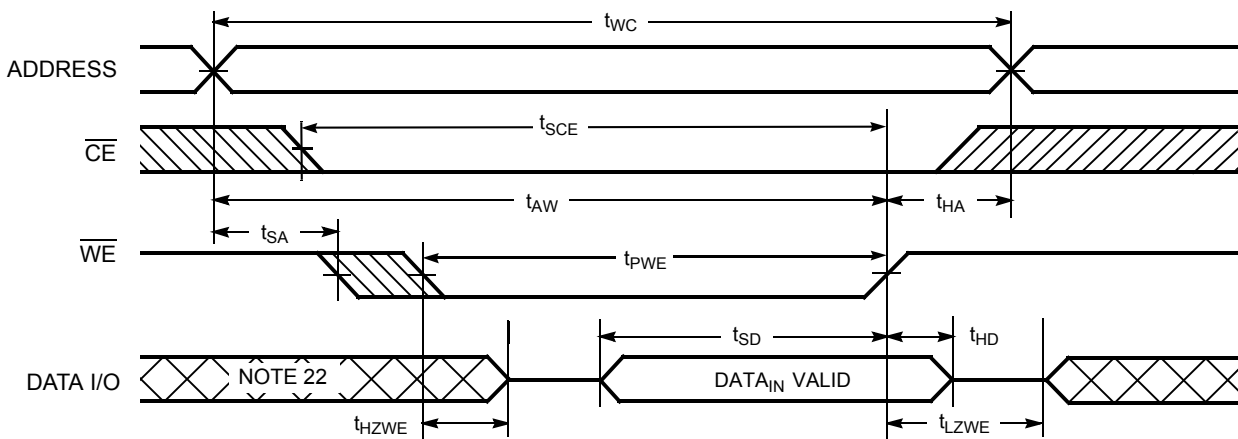


Figure 5. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[21]</sup>



Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data out ( $I/O_0$ - $I/O_7$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	H	High Z	Output disabled	Active ( $I_{\text{CC}}$ )
L	L	X	Data in ( $I/O_0$ - $I/O_7$ )	Write	Active ( $I_{\text{CC}}$ )

Notes

- 20. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
- 21. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in high-impedance state.
- 22. During this period, the I/Os are in output state and input signals should not be applied.

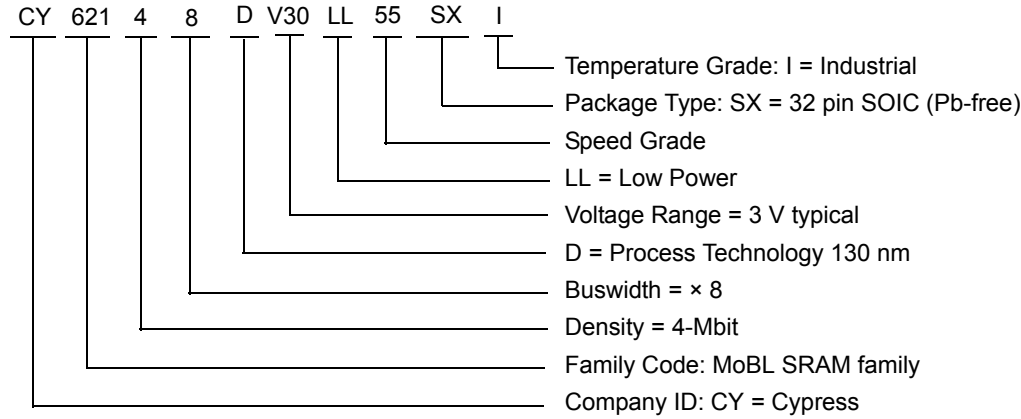


**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62148DV30LL-55SX I	51-85081	32-pin SOIC (Pb-free)	Industrial

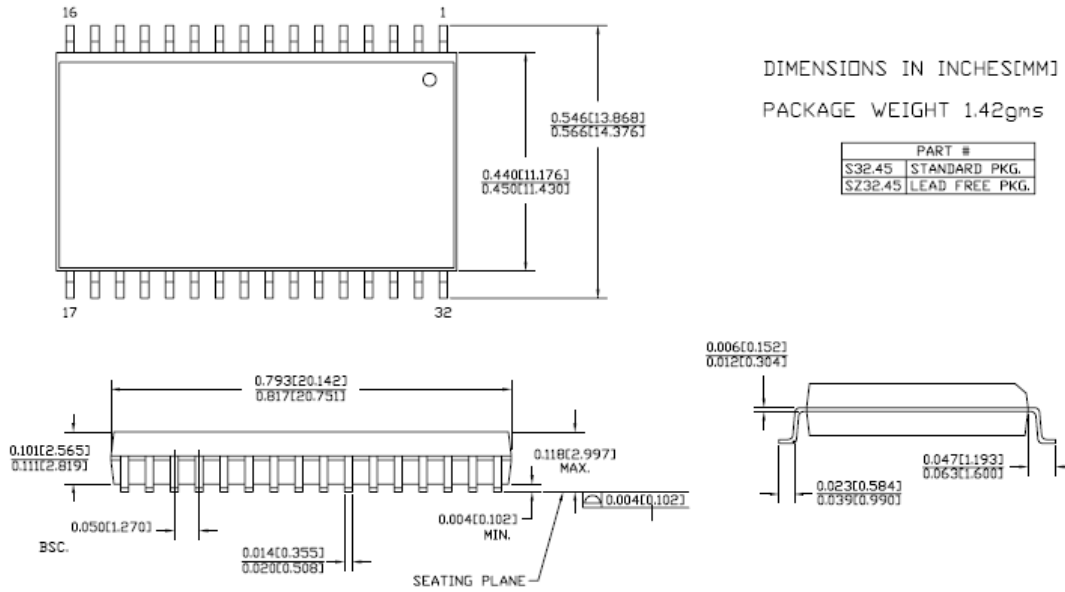
Contact your local Cypress sales representative for availability of these parts

**Ordering Code Definition**



Package Diagrams

32-pin (450 MIL) Molded SOIC, 51-85081



51-85081 °C

MoBL is a registered trademark, and More Battery Life is a trademark, of Cypress Semiconductor. All product and company names mentioned in this document may be the trademarks of their respective holders.

## Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
MoBL	more battery life
SOIC	small-outline integrated circuit
SRAM	static random access memory

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	volts
$\mu$ A	micro amperes
mA	milli amperes
pF	pico Farad
°C	degree Celsius
W	watts

Document History Page

Document Title:CY62148DV30, 4-Mbit (512K x 8) MoBL <sup>®</sup> Static RAM Document Number: 38-05341				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	127480	06/17/03	HRT	Created new data sheet
*A	131041	01/23/04	CBD	Changed from Advance to Preliminary
*B	222180	See ECN	AJU	Changed from Preliminary to Final Added 70 ns speed bin Modified footnote #6 and #12 Removed MAX value for V <sub>DR</sub> on "Data Retention Characteristics" table Modified input and output capacitance values Added Pb-free ordering information Removed 32-pin STSOP package
*C	498575	See ECN	NXR	Added Automotive-A Operating Range Removed SOIC package from Product Offering Updated Ordering Information Table
*D	729917	See ECN	VKN	Added SOIC package and its related information Updated Ordering Information Table
*E	2896036	03/19/10	AJU	Removed inactive parts from Ordering Information. Added Table of Contents. Updated Packaging Information Updated links in Sales, Solutions, and Legal Information.
*F	3166059	02/08/2011	RAME	Removed Automotive related info Removed 70 ns speed bin related info Remove TSOP and VFBGA package related info Updated as per new template Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> table Added <a href="#">Ordering Code Definition</a> details

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Automotive	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
Interface	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
Lighting & Power Control	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
Memory	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
Optical & Image Sensing	<a href="http://cypress.com/go/image">cypress.com/go/image</a>
PSoC	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
Touch Sensing	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
USB Controllers	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
Wireless/RF	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
PSoC 1 | PSoC 3 | PSoC 5

---

© Cypress Semiconductor Corporation, 2010-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.