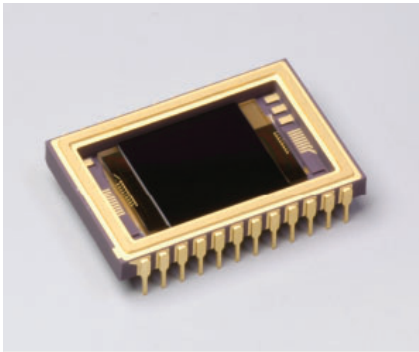


# CCD area image sensor



S10747-0909

## Enhanced near-infrared sensitivity by using fully-depleted CCD technology

The S10747-0909 is a back-illuminated CCD area image sensor that has significantly improved near-infrared sensitivity and soft X-ray detection efficiency. This has been achieved by using a thick silicon substrate that allows the depletion layer to be thickened by applying a bias voltage.

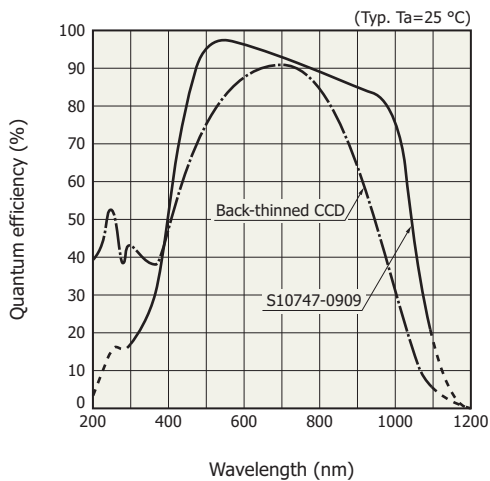
### Features

- Quantum efficiency: 70% ( $\lambda=1000$  nm,  $T_a=25$  °C)
- Pixel size: 24 × 24  $\mu\text{m}$
- 512 × 512 pixels
- Low readout noise

### Applications

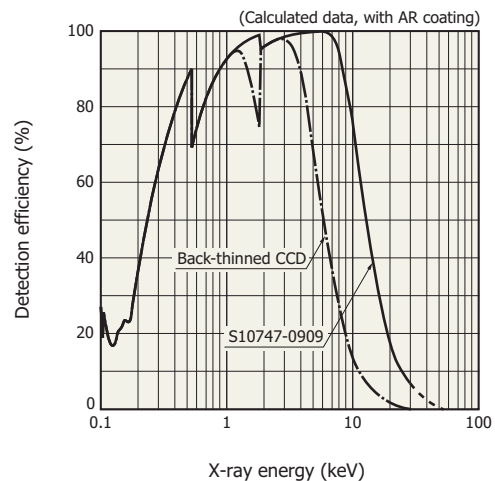
- Space telescope

### Spectral response (without window)



KMPDB0313EA

### Soft X-ray detection efficiency



KMPDB0317EA

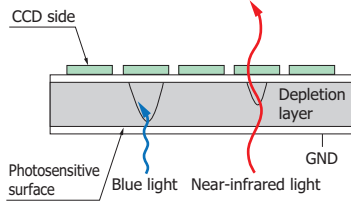
### General ratings

Parameter	Specification
Pixel size	24 (H) × 24 (V) $\mu\text{m}$
Number of pixels	532 (H) × 520 (V)
Number of active pixels	512 (H) × 512 (V)
Active area	12.288 (H) × 12.288 (V) mm
Vertical clock phase	2 phases
Horizontal clock phase	2 phases
Output circuit	One-stage MOSFET source follower
Package	24-pin ceramic DIP (refer to dimensional outline)
Window	None (temporary glass window)

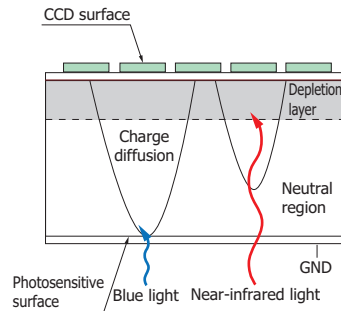
**Structure of fully-depleted back-illuminated CCD**

Back-thinned CCDs the silicon substrate is only a few dozen microns thick. This means that near-infrared light is more likely to pass through the substrate (see Figure 1), thus resulting in a loss of quantum efficiency in infrared region. Thickening the silicon substrate increases the quantum efficiency in the near-infrared region but also makes the resolution worse since the generated charges diffuse into the neutral region unless a bias voltage is applied (see Figure 2). Fully-depleted back-illuminated CCDs use a thick silicon substrate that has no neutral region when a bias voltage is applied and therefore deliver high quantum efficiency in the near-infrared region while maintaining a good resolution (see Figure 3). One drawback, however, is that the dark current becomes large so that these devices must usually be cooled to about -70 °C during use.

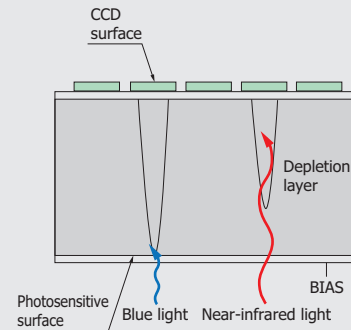
**[Figure 1] Back-thinned CCD**



**[Figure 2] When no bias voltage is applied to thick silicon**



**[Figure 3] When a bias voltage is applied to thick silicon (fully-depleted back-illuminated CCD)**



KMPDC0332EA

**▣ Absolute maximum ratings (Ta=-70 °C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-120	-	+30	°C
Storage temperature	Tstg	-200	-	+70	°C
Substrate voltage (applied bias voltage)	Vss	-0.5	-	+30	V
OD voltage	VOD	-25	-	+0.5	V
RD voltage	VRD	-18	-	+0.5	V
ISV voltage	VISV	-18	-	+0.5	V
ISH voltage	VISH	-18	-	+0.5	V
IGV voltage	VIG1V, VIG2V	-15	-	+10	V
IGH voltage	VIG1H, VIG2H	-15	-	+10	V
SG voltage	VSG	-15	-	+10	V
OG voltage	VOG	-15	-	+10	V
RG voltage	VRG	-15	-	+10	V
TG voltage	VTG	-15	-	+10	V
Vertical clock voltage	VP1V, VP2V	-15	-	+10	V
Horizontal clock voltage	VP1H, VP2H	-15	-	+10	V

▣ Operating conditions (Ta=-70 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	-22	-20	-18	V
Reset drain voltage		VRD	-13	-12	-11	V
Output gate voltage		VOG	-6	-5	-4	V
Substrate voltage		VSS	0.5	20	25	V
Test point	Vertical input source	VISV	-	VRD	-	V
	Horizontal input source	VISH	-	VRD	-	V
	Vertical input gate	VIG1V, VIG2V	-	0	3	V
	Horizontal input gate	VIG1H, VIG2H	-	0	3	V
Vertical shift register clock voltage	High	VP1VH, VP2VH	-8	-7	-6	V
	Low	VP1VL, VP2VL	2	3	4	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	-8	-7	-6	V
	Low	VP1HL, VP2HL	2	3	4	
Summing gate voltage	High	VSGH	-8	-7	-6	V
	Low	VSGL	2	3	4	
Reset gate voltage	High	VRGH	-8	-7	-6	V
	Low	VRGL	2	3	4	
Transfer gate voltage	High	VTGH	-8	-7	-6	V
	Low	VTGL	2	3	4	
External load resistance		RL	20	22	24	kΩ

▣ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	-	150	kHz
Vertical shift register capacitance		CP1V, CP2V	-	600	-	pF
Horizontal shift register capacitance		CP1H, CP2H	-	110	-	pF
Summing gate capacitance		CSG	-	20	-	pF
Reset gate capacitance		CRG	-	30	-	pF
Transfer gate capacitance		CTG	-	60	-	pF
Charge transfer efficiency*1		CTE	0.99995	0.99999	-	-
DC output level*2		Vout	-15	-13	-11	V
Output impedance*2		Zo	-	3	-	kΩ
Power consumption*2 *3		P	-	12	13	mW

- \*1: Charge transfer efficiency per pixel measured at half of the full well capacity
- \*2: The values depend on the load resistance. (VOD=-20 V, load resistance=22 kΩ)
- \*3: Power consumption of the on-chip amplifier plus load resistance

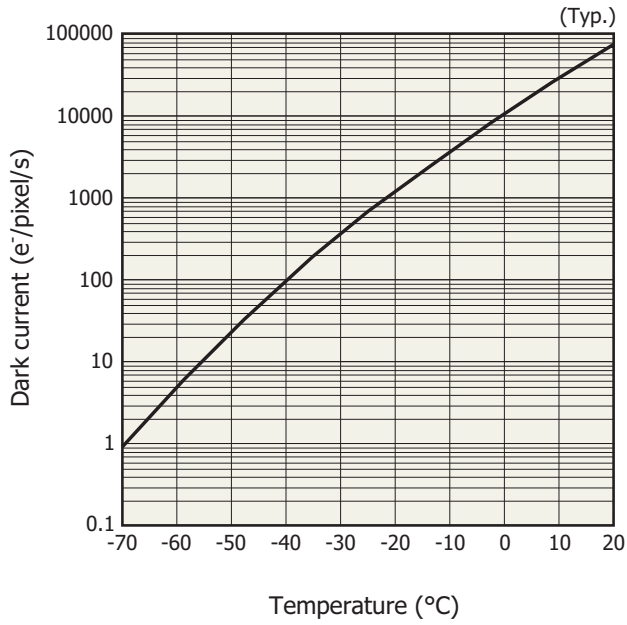
▣ Electrical and optical characteristics (Ta=-70 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	150	200	-	ke <sup>-</sup>
	Horizontal, summing gate		600	800	-	
CCD node sensitivity*4		Sv	1.4	1.7	2.0	μV/e <sup>-</sup>
Dark current*5		DS	-	1	10	e <sup>-</sup> /pixel/s
Readout noise*6		Nr	-	30	60	e <sup>-</sup> rms
Dynamic range*7	Line binning	DR	20000	26667	-	-
	Area scanning		5000	6666	-	-
Photo response non-uniformity*8		PRNU	-	±3	±10	%
Spectral response range		Ta=25 °C λ	-	300 to 1100	-	nm

- \*4: Load resistance=22 kΩ
- \*5: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
- \*6: Operating frequency=150 kHz
- \*7: Dynamic range = Full well capacity / Readout noise
- \*8: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 560 nm)

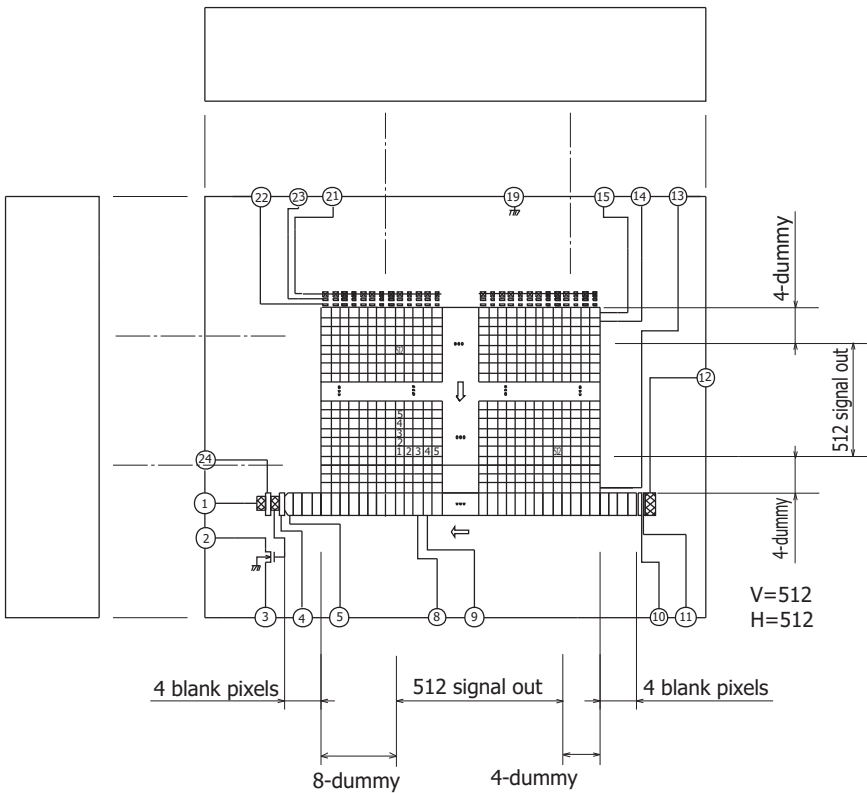
$$\text{Photo response non-uniformity (PRNU)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 \text{ [\%]}$$

**Dark current vs. temperature**



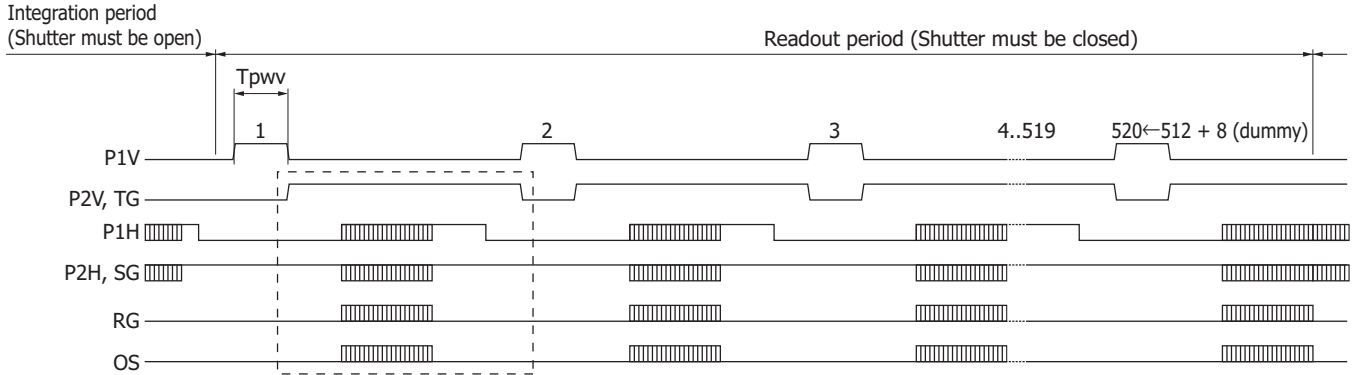
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**Device structure (conceptual drawing of top view)**

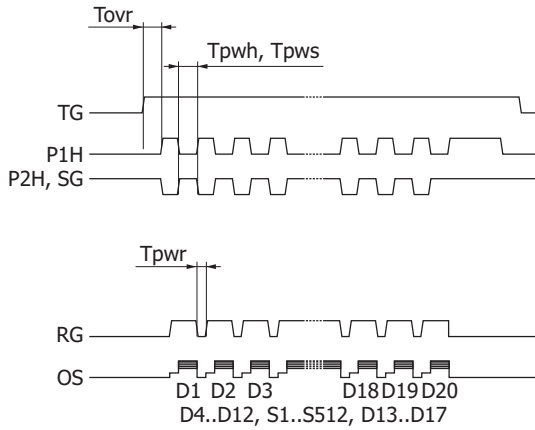


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**Timing chart**



Enlarged view

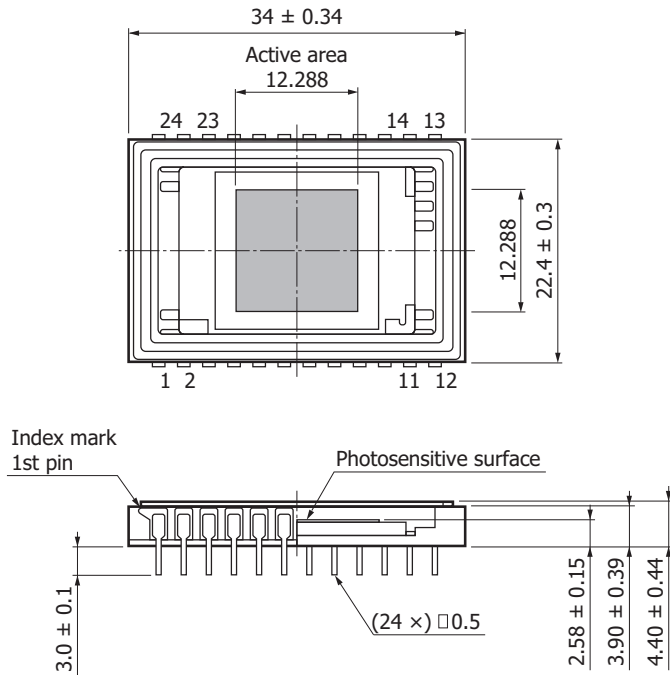


KMPDC0338EA

Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG* <sup>9</sup>	Pulse width	T <sub>pww</sub>	100	-	-	μs
	Rise and fall times	T <sub>prv</sub> , T <sub>pfv</sub>	4000	-	-	ns
P1H, P2H* <sup>9</sup>	Pulse width	T <sub>pwh</sub>	3.3	-	-	μs
	Rise and fall times	T <sub>prh</sub> , T <sub>pfh</sub>	5	-	-	ns
	Duty ratio	-	-	50	-	%
SG* <sup>9</sup>	Pulse width	T <sub>pws</sub>	3.3	-	-	μs
	Rise and fall times	T <sub>prs</sub> , T <sub>pfs</sub>	5	-	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	T <sub>pwr</sub>	60	-	-	ns
	Rise and fall times	T <sub>prr</sub> , T <sub>prf</sub>	5	-	-	ns
TG-P1H	Overlap time	T <sub>ovr</sub>	60	-	-	μs

\*9: Symmetrical pulses should be overlapped at 50% of maximum amplitude.

**Dimensional outline (unit: mm)**



KMPDA0256EA

**Pin connections**

Pin no.	Symbol	Function	Remark (standard operation)
1	RD	Reset drain	-12 V
2	OS	Output transistor source	RL=22 kΩ
3	OD	Output transistor drain	-20 V
4	OG	Output gate	-5 V
5	SG	Summing gate	
6	-		
7	-		
8	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	0 V
11	IG1H	Test point (horizontal input gate-1)	0 V
12	ISH	Test point (horizontal input source)	Connect to RD
13	TG	Transfer gate	
14	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	
16	-		
17	-		
18	-		
19	SS	Substrate voltage (applied bias voltage)	+20 V
20	-		
21	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	0 V
23	IG1V	Test point (vertical input gate-1)	0 V
24	RG	Reset gate	

**⚠ Precaution for use (Electrostatic countermeasures)**

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

**⚠ Element cooling/heating temperature incline rate**

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

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