

IRF644B/IRFS644B

250V N-Channel MOSFET

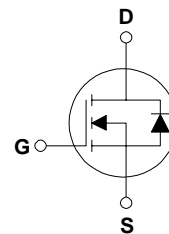
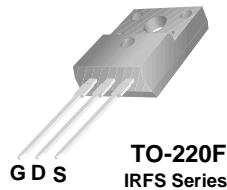
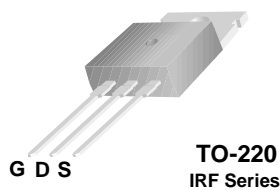
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converter and switch mode power supplies.

Features

- 14A, 250V, $R_{DS(on)} = 0.28\Omega @ V_{GS} = 10V$
- Low gate charge (typical 47 nC)
- Low C_{rss} (typical 30 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	IRF644B	IRFS644B	Units
V_{DSS}	Drain-Source Voltage	250		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	14	14 *	A
		8.9	8.9 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	56	56 *	A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	480		mJ
I_{AR}	Avalanche Current (Note 1)	14		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	13.9		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	139	43	W
		1.11	0.35	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	IRF644B	IRFS644B	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Max.	0.9	2.89	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Max.	62.5	62.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	250	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.24	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 200\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 7.0\text{ A}$	--	0.22	0.28	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 7.0\text{ A}$ (Note 4)	--	11.7	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1250	1600	pF
C_{oss}	Output Capacitance		--	150	195	pF
C_{riss}	Reverse Transfer Capacitance		--	30	40	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125\text{ V}, I_D = 14\text{ A},$ $R_G = 25\ \Omega$	--	20	50	ns
t_r	Turn-On Rise Time		--	115	240	ns
$t_{d(off)}$	Turn-Off Delay Time		--	150	310	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	--	95	200
Q_g	Total Gate Charge	$V_{DS} = 200\text{ V}, I_D = 14\text{ A},$ $V_{GS} = 10\text{ V}$	--	47	60	nC
Q_{gs}	Gate-Source Charge		--	6.2	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4, 5)	--	23	--

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	14	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	56	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 14\text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 14\text{ A},$	--	240	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	1.96	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 3.9\text{ mH}, I_{AS} = 14\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 14\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

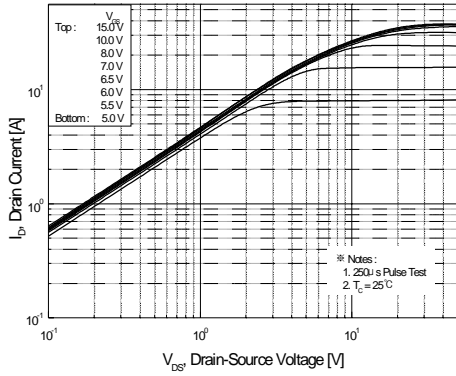


Figure 1. On-Region Characteristics

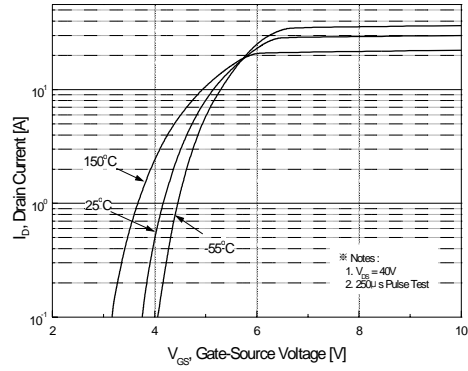


Figure 2. Transfer Characteristics

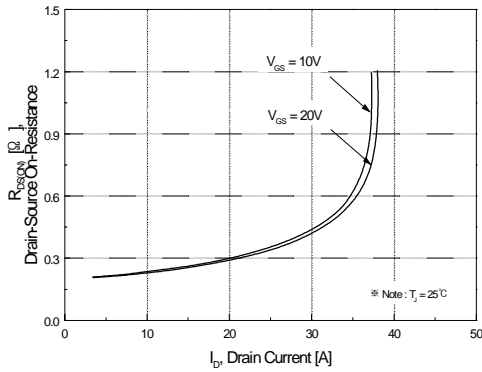


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

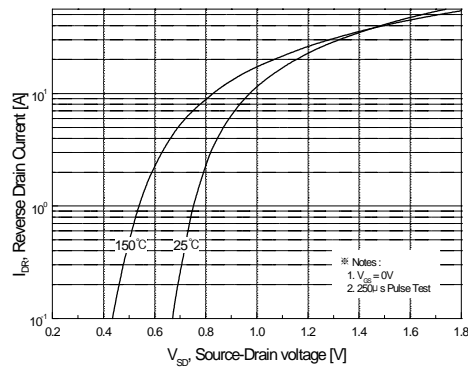


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

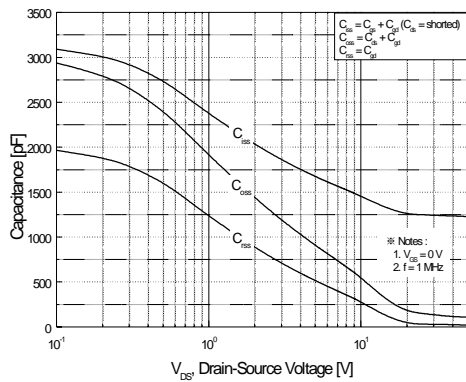


Figure 5. Capacitance Characteristics

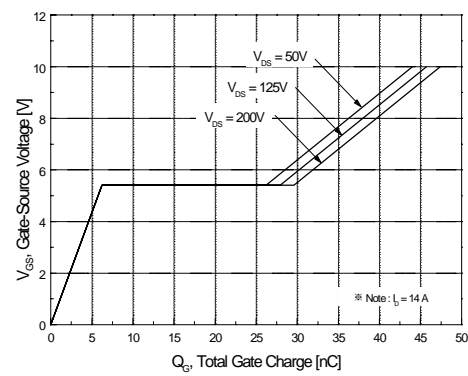


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

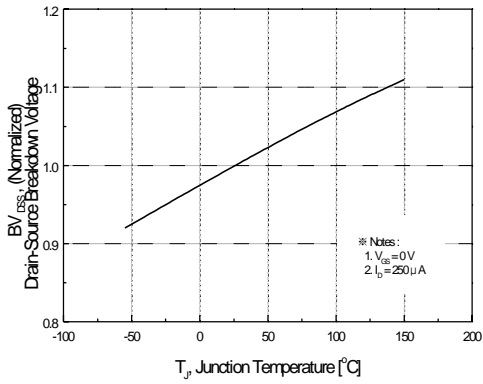


Figure 7. Breakdown Voltage Variation vs Temperature

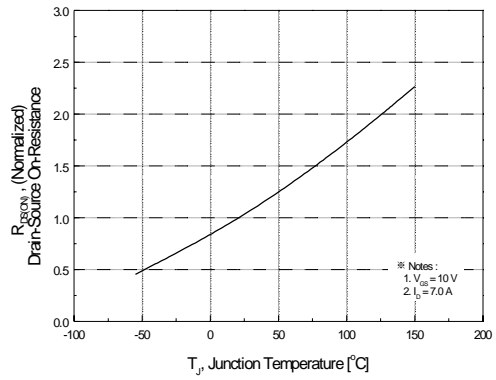


Figure 8. On-Resistance Variation vs Temperature

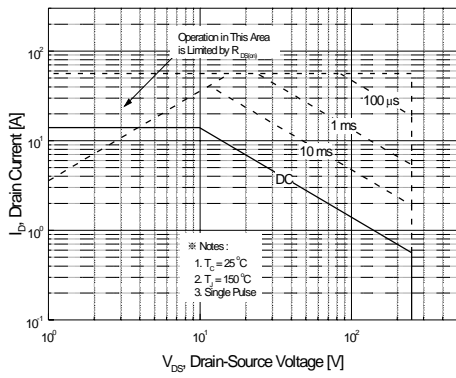


Figure 9-1. Maximum Safe Operating Area for IRF644B

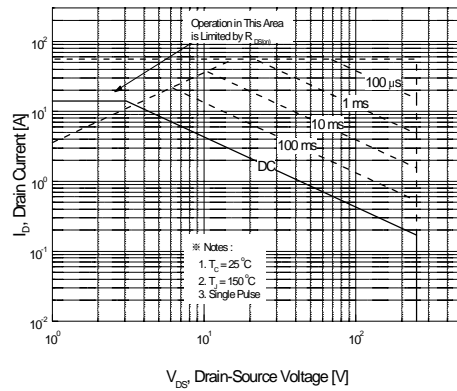


Figure 9-2. Maximum Safe Operating Area for IRFS644B

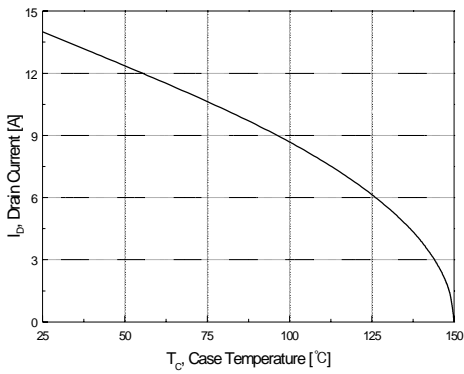


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

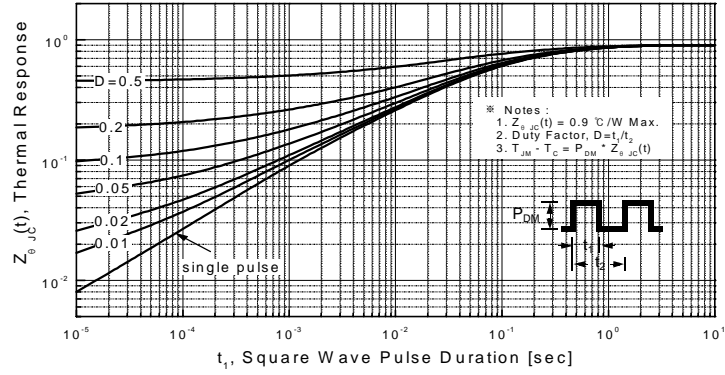


Figure 11-1. Transient Thermal Response Curve for IRF644B

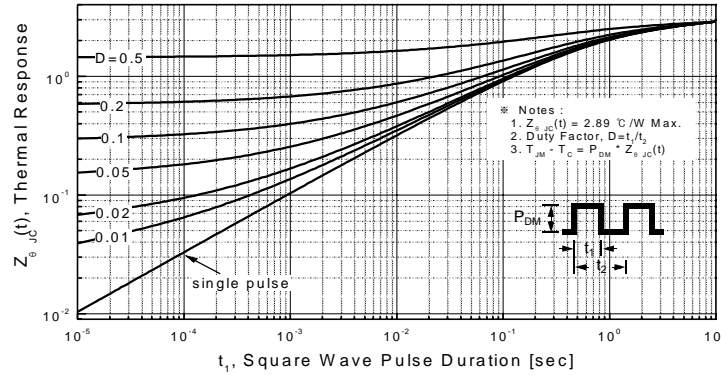


Figure 11-2. Transient Thermal Response Curve for IRFS644B

Gate Charge Test Circuit & Waveform



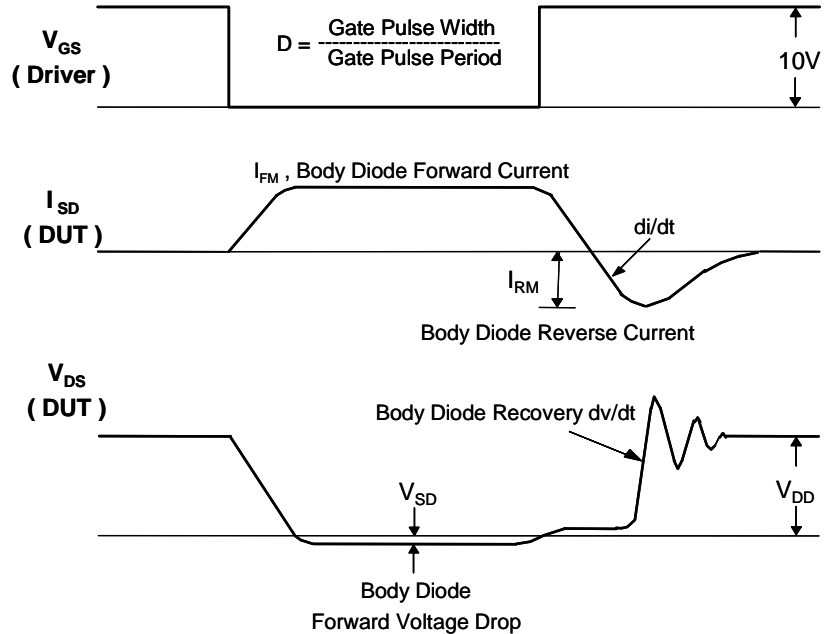
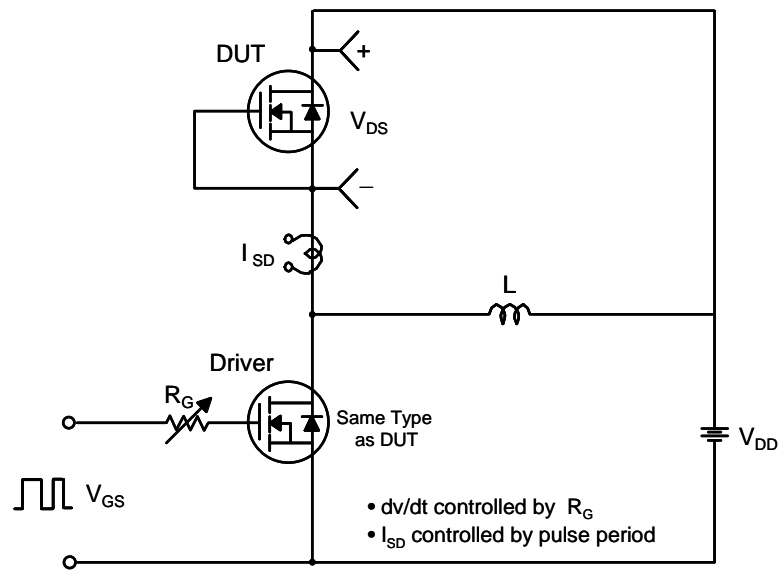
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

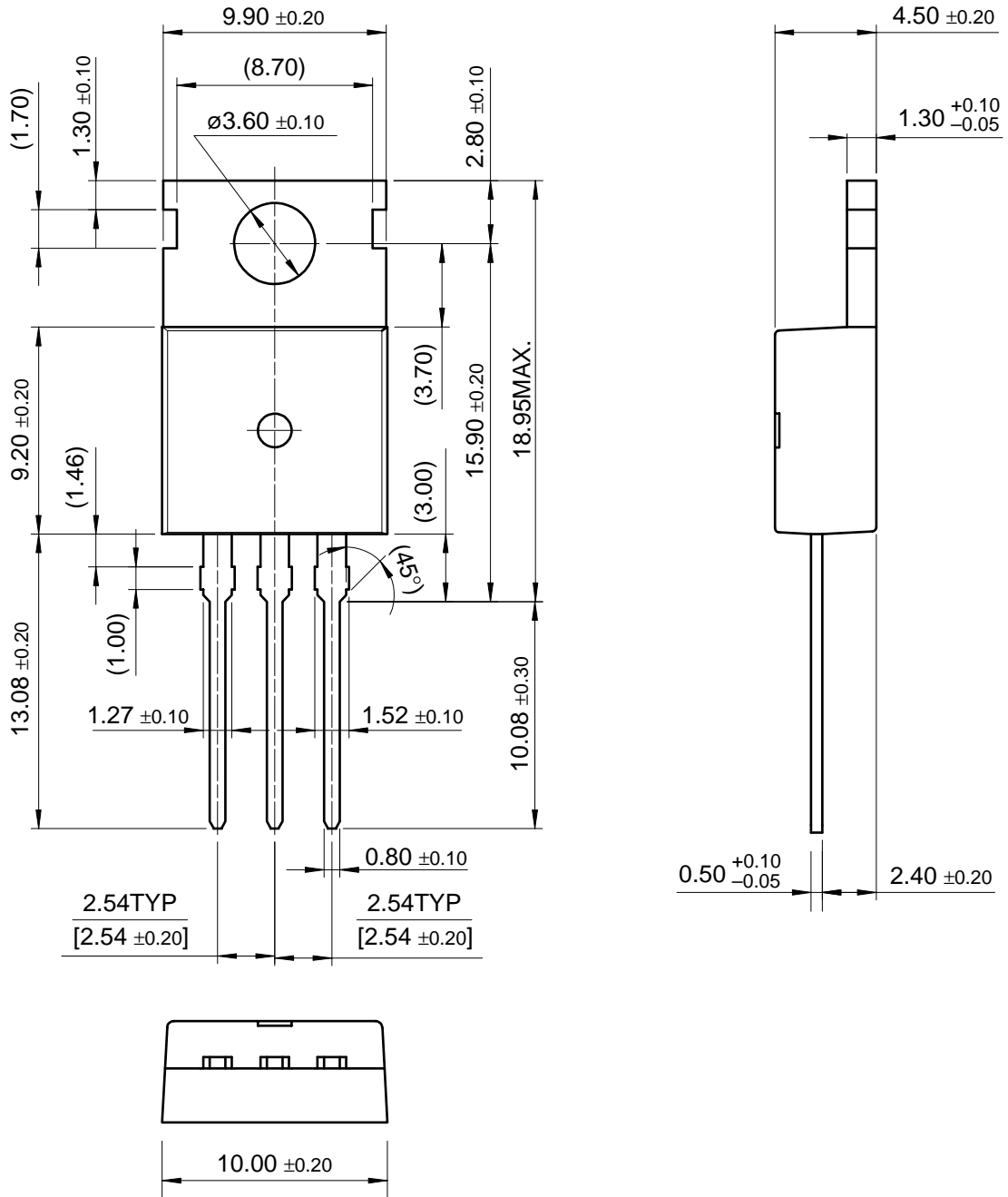


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-220



Dimensions in Millimeters

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Definition of Terms

Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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IRFS644B

250V N-Channel B-FET / Substitute of IRFS644 & IRFS644A

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General description

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Product status/pricing/packaging

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Product	Product status	Pb-free Status	Package type	Leads	Packing method	Package Marking Convention**
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IRFS644B_FP001	Not recommended for new designs		TO-220F	3	RAIL	Line 1: \$Y (Fairchild logo) &Z (Asm. Plant Code) &4 (4-Digit Date Code) Line 2: IRFS Line 3: 644B
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Indicates product with Pb-free second-level interconnect. For more information [click here](#).

Package marking information for product IRFS644B is available. [Click here for more information](#).

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Qualification Support

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Product
IRFS644B_FP001

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