Ordering number : ENA1760

SANYO Semiconductors
DATA SHEET

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LV8491CT — Bi-CMOS LSI Piezo Actuator Driver IC

Overview

The LV8491CT is a piezoelectric actuator driver IC. It internally generates drive waveforms and this makes it possible to control piezoelectric actuators with simple instructions.

Features

- Actuators using piezoelectric elements can be driven and controlled simply by I^2C communication.
- Multiple patterns of drive waveform conditions can be set for before and after performing normal operation when executing the DRVPULSE instruction.
- The piezoelectric drive waveforms are set externally by serial input signals using the I^2C interface.
  The rising and falling timings are determined with clock count.
- Startup/stop of the IC is controlled by ENIN register input through I^2C communication.
- The time for which the actuator is driven is determined with the drive frequency setting based on I^2C communication.
- BUSY output can be used to identify the operation/stop state of the actuator while output is present at the OUT pin. The BUSY signal can also be checked with the READ function controlled through I^2C communication.
- Built-in undervoltage detection and protection circuit, and register power-on reset function.

Specifications

Absolute Maximum Ratings at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		-0.5 to 5.0	V
Output current	I_O max		300	mA
Peak output current 1	I_O peak 1	t ≤ 1ms	750	mA
Peak output current 2	I_O peak 2	t ≤ 10μs	1200	mA
Input signal voltage	V_{IN} max		-0.5 to V_{CC}+0.5	V
Allowable dissipation	Pd	*Mounted on a specified board.	350	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

* Specified board : 40mm × 40mm × 1.6mm, glass epoxy board.

Allowable Operating Conditions at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.2 to 3.3	V
Input signal voltage	V_{IN}		-0.3 to V_{CC}	V
Corresponding CLK input frequency	Fclk		to 60	MHz
Maximum operating frequency	Ct max		Set STP count × 512	Times

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V, GND = 0V, unless otherwise specified.

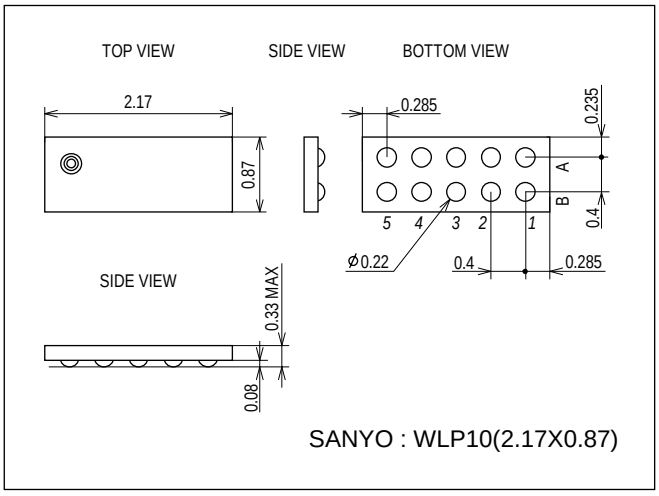
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	$I_{CC}0$	No CLK input, When SCL/SDA = L			1.0	μA
Operating mode current drain	$I_{CC}1$	CLK = 10MHz, When SCL/SDA = H		0.5	1.0	mA
High-level input voltage	V_{IH}	2.2V ≤ V_{CC} ≤ 3.3V SCL, SDA	1.4		V_{CC}+0.3	V
Low-level input voltage	V_{IL}	2.2V ≤ V_{CC} ≤ 3.3V SCL, SDA	-0.3		0.4	V
CLK pin high-level input voltage	$V_{IH}2$	CLK	0.5×V_{CC}		V_{CC}+0.3	V
CLK pin low-level input voltage	$V_{IL}2$	CLK	-0.3		0.2×V_{CC}	V
BUSY pin high-level output voltage	B_OH	With no load	V_{CC}-0.15		V_{CC}	V
BUSY pin low-level output voltage	B_OL	With no load	0		0.15	V
BUSY pin leakage current	BLK				1.0	μA
BUSY pin sink current	Blsk	BUSY pin voltage when BUSY is set low = 2.8V	1.5	2.2		mA
BUSY pin source current	Blso	BUSY pin voltage when BUSY is set high = 0V	1.5	2.2		mA
Low voltage detection voltage	Vres	V_{CC} voltage	1.8	2.0	2.2	V
Output block upper-side on resistance	RonP			0.8	1.5	Ω
Output block lower-side on resistance	RonN			0.6	1.2	Ω
Turn on time	TPLH	With no load *1			0.15	μS
Turn off time	TPHL	With no load *1			0.1	μS

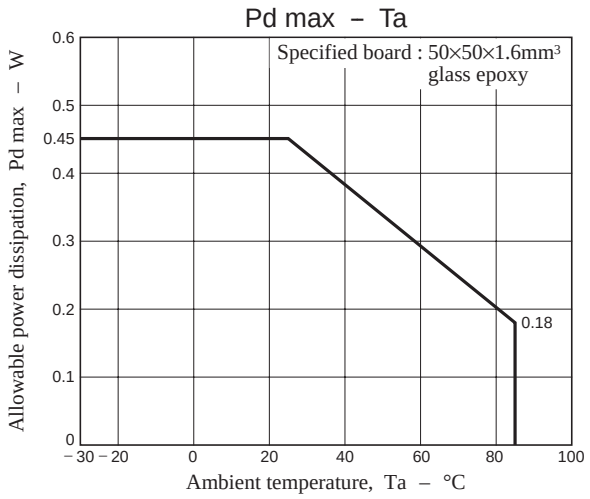
*1 : Rising time from 10 to 90% and falling time from 90 to 10% are specified with regard to the OUT pin voltage.

Package Dimensions

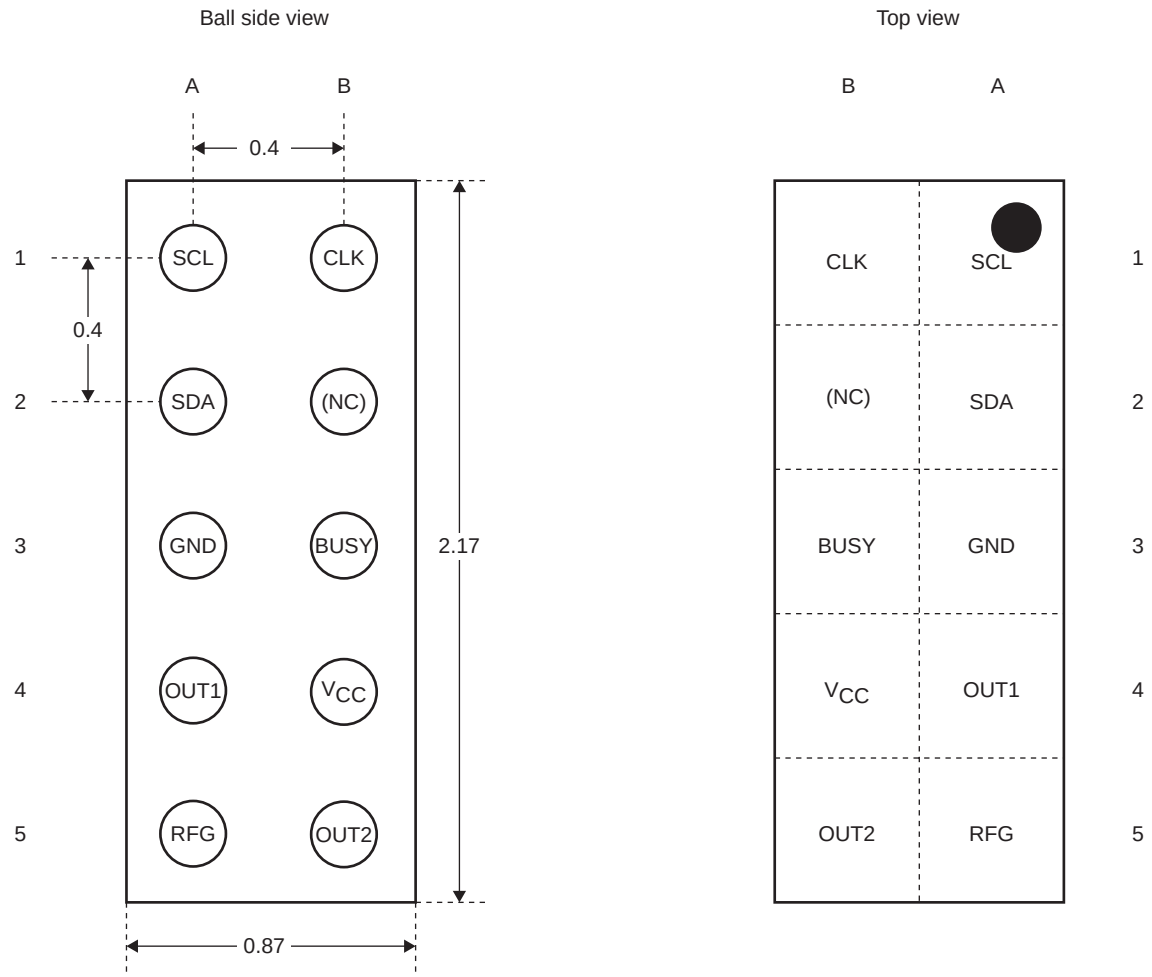
unit : mm (typ)

3399



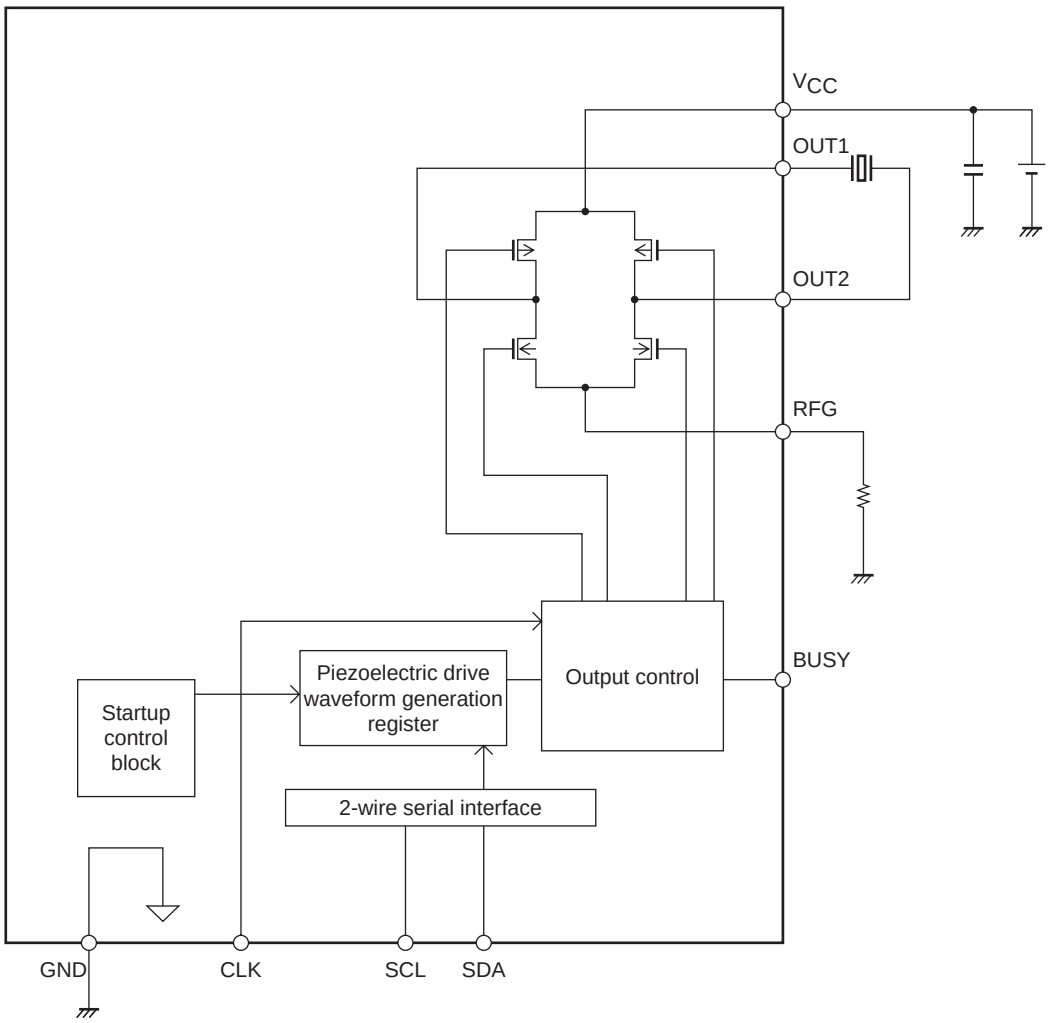


Pin Assignment



A1:SCL
A2:SDA
A3:GND
A4:OUT1
A5:RFG
B1:CLK
B2:(NC)
B3:BUSY
B4:V_{CC}
B5:OUT2

Block Diagram



Value of the resistor connected to the RFG pin

Inrush current flowing to the piezoelectric elements can be controlled in the LV8491CT by inserting a resistor between the RFG pin and GND potential.

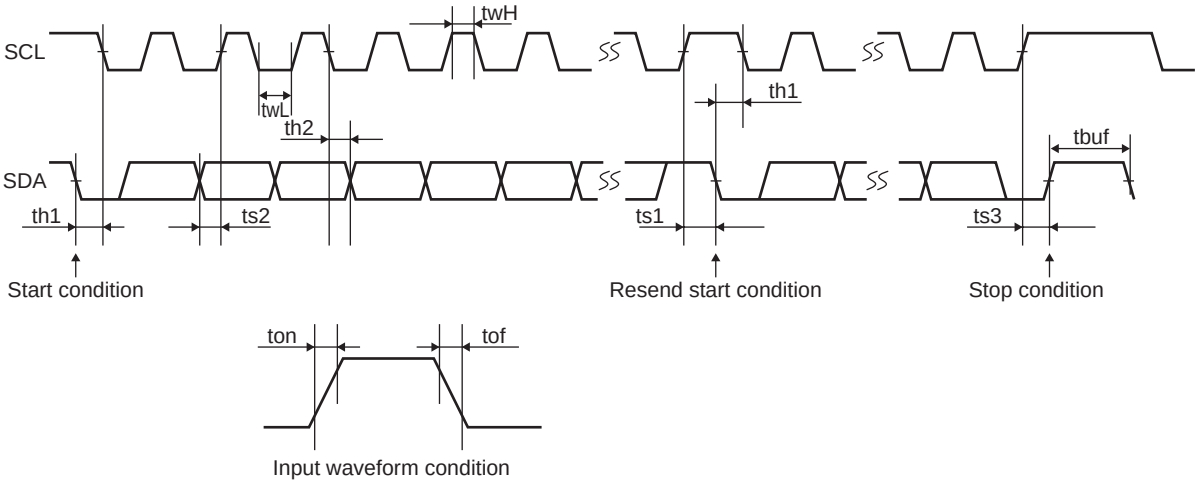
Since the resistance affects the actuator operation, the constant must be determined in a range from 0 to 3.3Ω while monitoring the operation of the actuator.

Capacitor on the V_{CC} line

Piezoelectric actuators are capacitive loads in electrical terms, and they operate units by charging and discharging the charges. Since the charge between the capacitor on the V_{CC} line and piezoelectric elements is transferred, the capacitor must be mounted near the V_{CC} pin. The capacitance of the capacitor required is determined by the capacitance of the piezoelectric element. A capacitance within a range that does not affect operation must be selected.

Serial Bus Communication Specifications

I^2C serial transfer timing conditions



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0.06			μs
Pulse width	twL	SCL low period pulse width	4.7			μs
	twH	SCL high period pulse width	4.0			μs
Input waveform conditions	ton	SCL/SDA (input) rising time			1000	ns
	tof	SCL/SDA (input) falling time			300	ns
Bus free time	tbuf	Interval between stop condition and start condition	4.7			μs

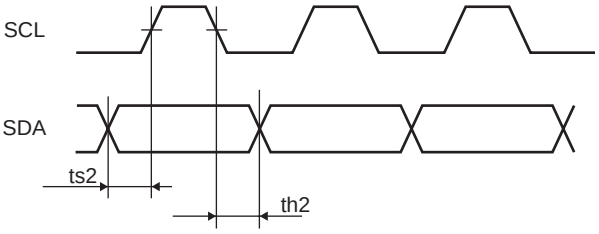
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	Clock frequency of SCL	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6			μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0.06			μs
Pulse width	twL	SCL low period pulse width	1.3			μs
	twH	SCL high period pulse width	0.6			μs
Input waveform conditions	ton	SCL/SDA (input) rise time			300	ns
	tof	SCL/SDA (input) fall time			300	ns
Bus free time	tbuf	Interval between the stop condition and the start condition	1.3			μs

I²C bus transfer method

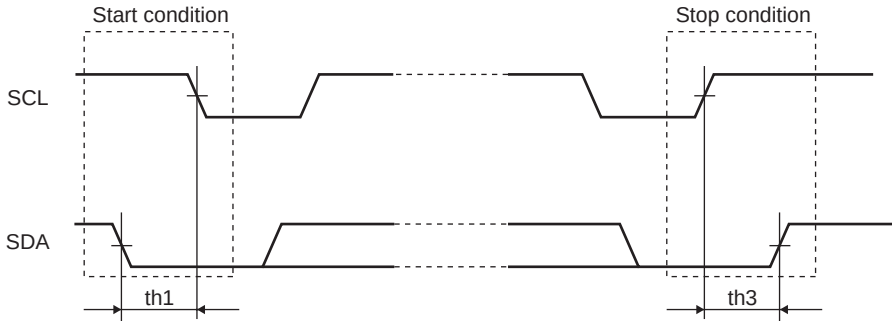
Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.



When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.

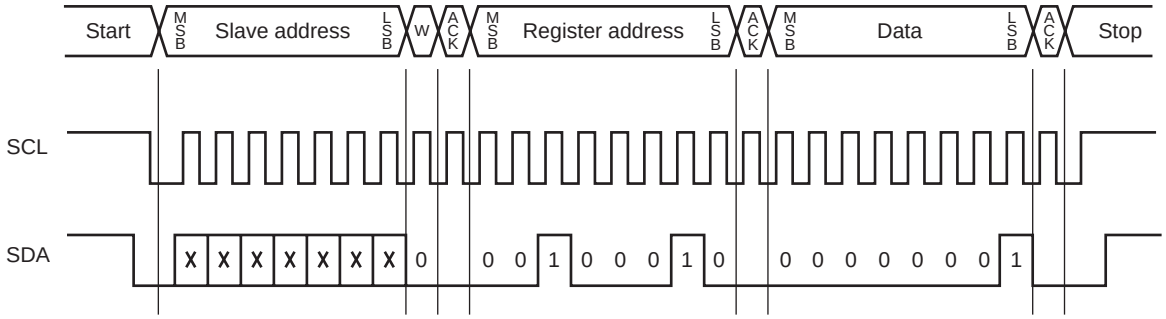


Data transfer and acknowledgement response

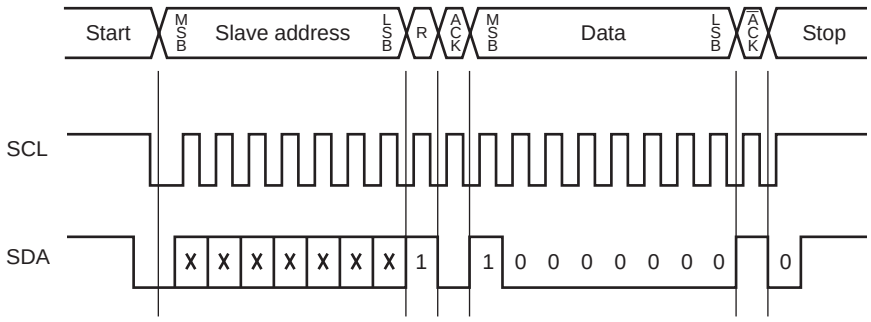
After the start condition is generated, data is transferred one byte (8 bits) at a time. Any number of data bytes can be transferred consecutively.

An ACK signal is sent to the sending side from the receiving side every time 8 bits of data are transferred. The transmission of an ACK signal is performed by setting the receiving side SDA to low after SDA at the sending side is released immediately after the clock pulse of SCL bit 8 in the data transferred has fallen low.
After the receiving side has sent the ACK signal, if the next byte transfer operation is to receive only the byte, the receiving side releases SDA on the falling edge of the 9th clock of SCL.
There are no CE signals in the I^2C bus ; instead, a 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) which specifies the direction of subsequent data transfer.
The READ function of the LV8491CT provides only the functionality to test the BUSY state.
7-bit address data is transferred sequentially starting at the MSB and the second and subsequent bytes are written if the state of the 8th bit is low and read if the state is high.
In the LV8491CT, the slave address is stipulated to be “1110010.”.

WRITE mode timing



READ mode timing



Data transfer write format

The slave address and Write command must be allocated to the first byte and the register address in the serial map must be designated in the second byte.

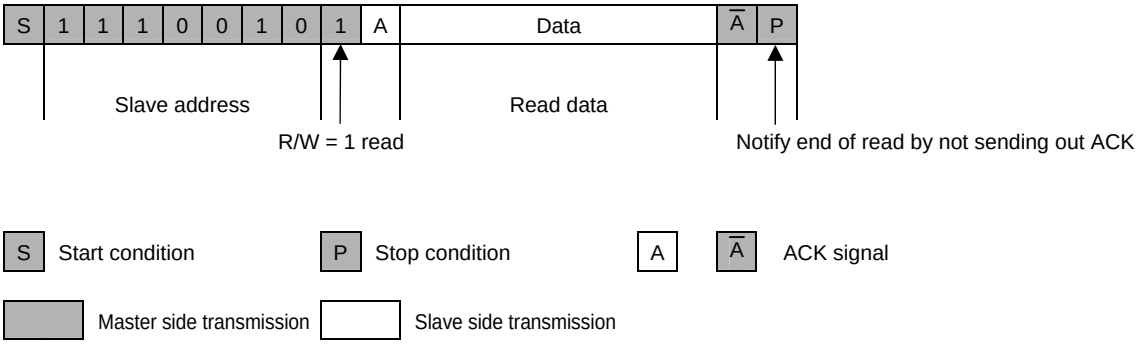
For the third byte, data transfer is carried out to the address designated by the register address which is written in the second byte. Subsequently, if data continues, the register address value is automatically incremented for the fourth and subsequent bytes.

Thus, continuous data transfer starting at the designated address is made possible.

After the register address reaches 1Fh, the transfer address for the next byte is set to 00h.

Data write example

Data read example



Serial Map

	Register Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0	M/I	DRVPULSE [6 : 0]						
0									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1	GATE	×	ENIN	CKSEL [1 : 0]		RET [1 : 0]		INIT
1									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0	RST [7 : 0]							
2									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	1	GTAS [7 : 0]							
3									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	0	GTBR [7 : 0]							
4									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	1	GTBS [7 : 0]							
5									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	1	0	STP [7 : 0]							
6									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	1	1	×	×	×	×	INITMOV [7 : 4]			
7									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	0	0	×	×	NRPULSE1 [5 : 0]					
8									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	0	1	×	×	NRP-A [5 : 0]					
9									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	1	0	×	×	NRP-B [5 : 0]					
10									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	1	1	×	×	NRP-C [5 : 0]					
11									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	0	0	×	×	NRP-D [5 : 0]					
12									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	0	1	×	×	NRPULSE2 [5 : 0]					
13																
	0	0	0	0	1	1	1	0	×	×	NRP-E [5 : 0]					
14									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	1	1	×	×	NRP-F [5 : 0]					
15									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	0	×	×	NRP-G [5 : 0]					
16									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	1	×	×	NRP-H [5 : 0]					
17									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	1	0	NR1GTBR [7 : 0]							
18									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	1	1	NR1GTBS [7 : 0]							
19									0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	0	NR2GTBR [7 : 0]							
20									0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	1	NR2GTBS [7 : 0]							
21									0	0	0	0	0	0	0	0
	0	0	0	1	0	1	1	0	NR3GTBR [7 : 0]							
22									0	0	0	0	0	0	0	0
	0	0	0	1	0	1	1	1	NR3GTBS [7 : 0]							
23									0	0	0	0	0	0	0	0

Upper : Register name Lower : Default value

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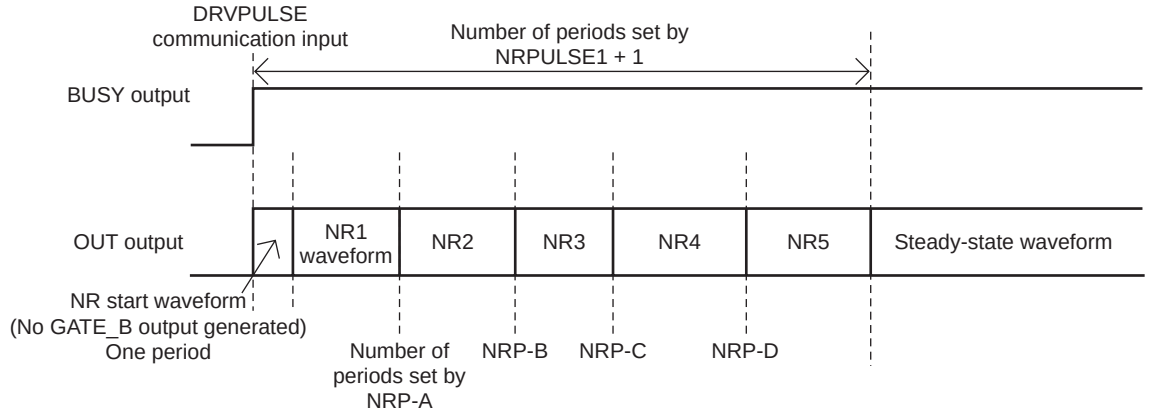
	Register Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	1	1	0	0	0	NR4GTBR [7 : 0]							
24									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	0	1	NR4GTBS [7 : 0]							
25									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	1	0	NR5GTBR [7 : 0]							
26									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	1	1	NR5GTBS [7 : 0]							
27									0	0	0	0	0	0	0	0
	READ mode only register								BUSY	×	×	×	×	×	×	×
28									0	0	0	0	0	0	0	0

Upper : Register name Lower : Default value

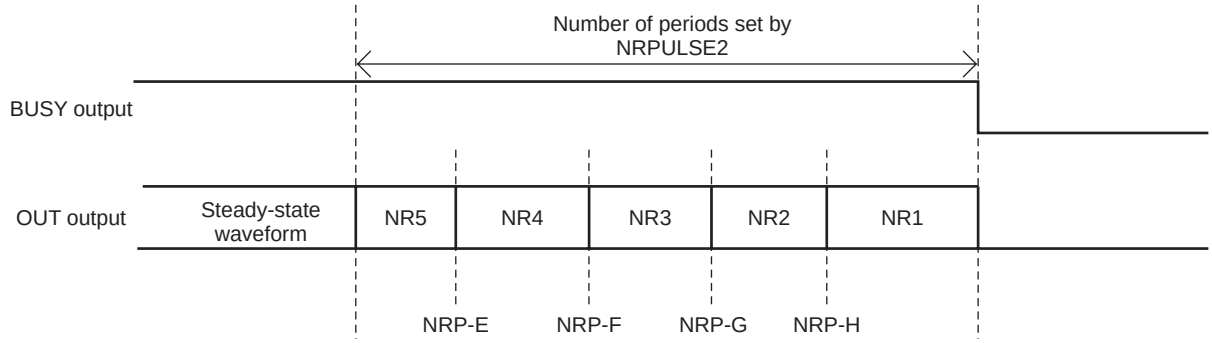
NR drive pulse output

Rise operation



For example, when NRPULSE1 is set to 15, NRP-A to 3, NRP-B to 6, NRP-C to 9, and NRP-D to 12, one period of the NR start waveform (no GATE_B output) is output, followed by three periods of the NR1 waveform, three periods of the NR2 waveform, three periods of the NR3 waveform, three periods of the NR4 waveform, three periods of the NR5 waveform, and then STP x DRVPULSE periods of the steady-state waveform.
When NRPULSE1 is set to 0, no NR pulse is generated and the same output as the normal DRVPULSE input is generated. In addition, when NRP-A and NRP-B are set the same value, the NR2 waveform is not output, and the NR3 waveform is output following the NR1 waveform.

Fall operation

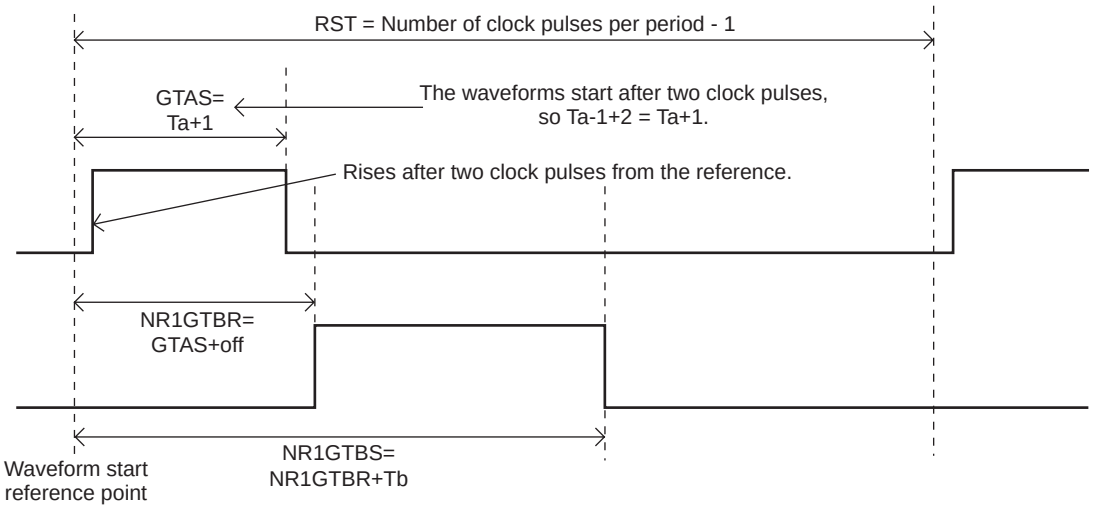


The fall waveforms are output in order from the NR5 waveform to the NR1 waveform. The switching timing is set in the same manner as that for rise operation.

NR drive waveform settings

The settings are the same as those for the normal drive waveform. Drive waveforms are generated using the same parameters as the normal waveform for RST and GTAS, and the NR waveform setting values for GTBR and GTBS.

Example: NR1 waveform

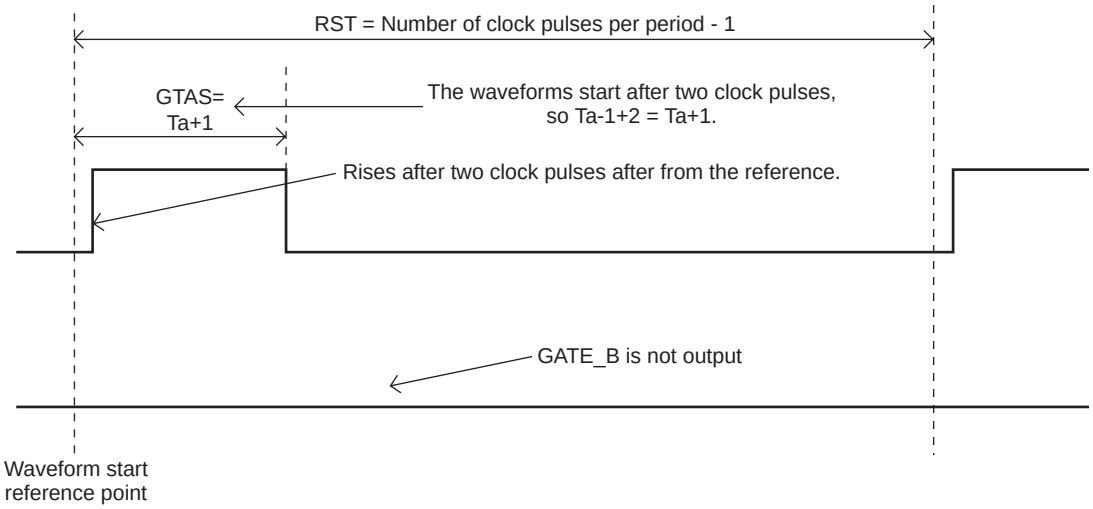


NR start waveform

NR waveform output control is as follows. When NRPULSE1 is set, a waveform without GATE_B output is output in the first rise period. After that the waveforms set by NR are output in order from NR1.

When there are no NR settings for rise operation (when NRPULSE = 0), the NR start waveform is not output.

The same parameters as those of the normal waveform are referenced for RST and GTAS, and GTBR and GTBS are zero input waveforms.



Serial Mode Settings

0	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

D0 to D6: DRVPULSE [6 : 0]

Operation count setting register. Specify a number from 0 to 127.
The number of cyclic operations determined by <DRVPLUSE setting> × <STP setting> are performed.
Additional data can be input and data is added up to the equivalent of total of 512 pulses.
However, when the EN pin is set low or ENIN is set to 0, the DRVPULSE counter is in the reset state, so DRVPULSE input is not accepted.
Output operation is performed when DRVPULSE input is recognized, and OUT output starts according to the waveform setting registers when the ACK signal is output after a 00h address instruction.

D7	M/I
0	∞
1	macro

Operation direction switching
*Default Infinity distance direction
Macro direction

Operation direction switching register

The operation count setting register is reset when the register is switched. To stop the operation of the unit, switch the M/I register and set DRVPULSE to 0 for input. This register is also used to set the direction of operation when the initialization sequence is to be performed.

1	0	0	0	0	0	0	0	1	D7	0	D5	D4	D3	D2	D1	D0

D0: Register for selecting whether the initialization sequence is to be performed when the ENIN input changes from 0 to 1.

D0	INIT
0	Initialization to be performed
1	Initialization not to be performed

Initialization to be performed/not to be performed setting
*Default

D2	D1	RET
0	0	2 times
0	1	1 time
1	0	3 times
1	1	4 times

Number of initialization sequence swing back
*Default

D4	D3	CKSEL
0	0	1/4
0	1	1/2
1	0	1
1	1	1

Input clock division ratio switching
*Default 1/4
1/2
1 (no frequency division)
1 (no frequency division)

D5 : ENIN ENIN register is used to start up IC and to give a trigger for initialization.
Output operation of the IC is performed only when ENIN is set to 1.

D7	GATE
0	MODE1
1	MODE2

Gate mode operation
*Default Forward/reverse/braking
Forward/reverse/standby

2	0	0	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0

RST7 to RST0 : Specifies the number of clocks per period (0 to 255). Default = 0

3	0	0	0	0	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

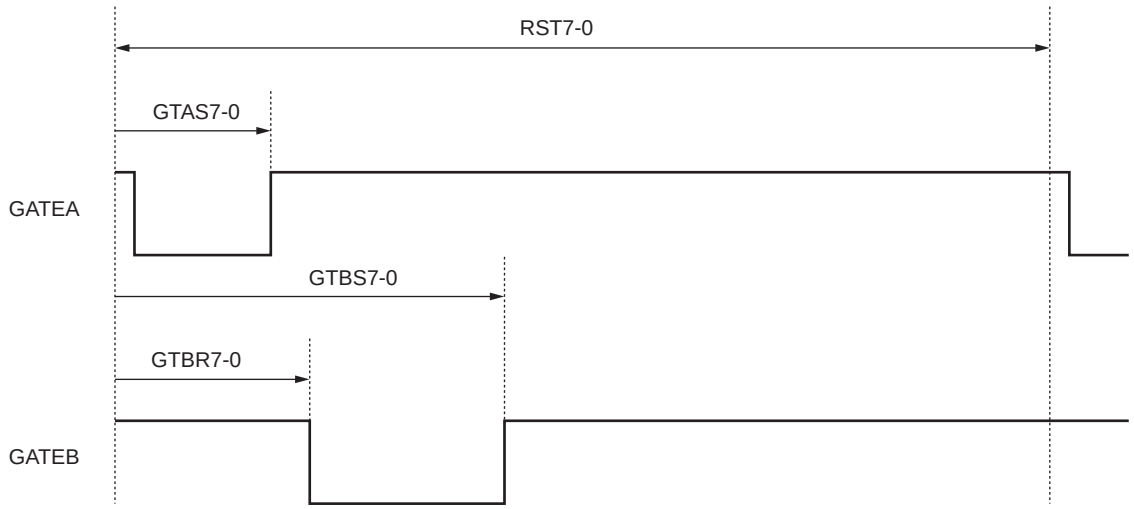
GTAS7 to GTAS0 : Sets the GATE_A pulse set value (0 to 255). Default = 0

4	0	0	0	0	0	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0

GTBR7 to GTBR0 : Sets the GATE_B pulse reset value (0 to 255). Default = 0

5	0	0	0	0	0	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0

GTBS7 to GTBS0 : Sets the GATE_B pulse set value (0 to 255). Default = 0



6	0	0	0	0	0	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0

STP7 to STP0 : Specifies the number of output pulse steps with regard to DRIVE input (1 to 256). Default = 1
The setting value range is handled as the data value plus 1.
When data is input in 8-bit units (0 to 255), it is handled as an STP period of 1 to 256.

7	0	0	0	0	0	1	1	1	0	0	0	0	D3	D2	D1	D0

INITMOV7 to INITMOV4 : Sets the number of swing back of the initialization sequence to be performed (16 to 256). Default = 16

D3	D2	D1	D0	INIT7 to 4	16 to 256
0	0	0	0	0	16
0	0	0	1	1	32
0	0	1	0	2	48
0	0	1	1	3	64
0	1	0	0	4	80
0	1	0	1	5	96
0	1	1	0	6	112
0	1	1	1	7	128
1	0	0	0	8	144
1	0	0	1	9	160
1	0	1	0	10	176
1	0	1	1	11	192
1	1	0	0	12	208
1	1	0	1	13	224
1	1	1	0	14	240
1	1	1	1	15	256

8	0	0	0	0	1	0	0	0	0	0	D5	D4	D3	D2	D1	D0

NRPUL15 to NRPUL10: 0 to 63. Default = 0

Specifies the total number of output periods of the NR1 to NR5 drive waveforms during rise operation when multiple drive waveforms are output continuously during actuator operation.

When set to 0, NR drive waveforms are not output during rise operation, and normal output operation is performed.

9	0	0	0	0	1	0	0	1	0	0	D5	D4	D3	D2	D1	D0

NRP-A5 to NRP-A0: 0 to 63. Default = 0

This register specifies the first switching timing of the rise NR drive waveform.

It determines the number of NR1 waveform output periods during rise operation.

10	0	0	0	0	1	0	1	0	0	0	D5	D4	D3	D2	D1	D0

NRP-B5 to NRP-B0: 0 to 63. Default = 0

This register specifies the second switching timing of the rise NR drive waveform.

The NR2 waveform is output for a number of periods equal to the difference between NRP-A and NRP-B.

11	0	0	0	0	1	0	1	1	0	0	D5	D4	D3	D2	D1	D0

NRP-C5 to NRP-C0: 0 to 63. Default = 0

This register specifies the third switching timing of the rise NR drive waveform.

The NR3 waveform is output for a number of periods equal to the difference between NRP-B and NRP-C.

12	0	0	0	0	1	1	0	0	0	0	D5	D4	D3	D2	D1	D0

NRP-D5 to NRP-D0: 0 to 63. Default = 0

This register specifies the fourth switching timing of the rise NR drive waveform.

The NR4 waveform is output for a number of periods equal to the difference between NRP-C and NRP-D, and the NR5 waveform is output for a number of periods equal to the difference between NRP-D and NRPUL1.

When setting the rise NR drive waveforms, the setting values should in principle satisfy the following relationship.

NRP-A ≤ NRP-B ≤ NRP-C ≤ NRP-D

(When this relationship is not satisfied, unintended drive waveforms may be output. However, this will not result in IC breakdowns or other damage.)

13	0	0	0	0	1	1	0	1	0	0	D5	D4	D3	D2	D1	D0

NRPUL25 to NRPUL20: 0 to 63. Default = 0

Specifies the total number of output periods of the NR5 to NR1 drive waveforms during fall operation, when multiple drive waveforms are output continuously during actuator operation.

When set to 0, NR drive waveforms are not output during fall operation, and operation stops.

14	0	0	0	0	1	1	1	0	0	0	D5	D4	D3	D2	D1	D0

NRP-E5 to NRP-E0: 0 to 63. Default = 0

This register specifies the first switching timing of the fall NR drive waveform.

It determines the number of NR5 waveform output periods during fall operation.

15	0	0	0	0	1	1	1	1	0	0	D5	D4	D3	D2	D1	D0

NRP-F5 to NRP-F0: 0 to 63. Default = 0

This register specifies the second switching timing of the fall NR drive waveform.

The NR4 waveform is output for a number of periods equal to the difference between NRP-E and NRP-F.

16	0	0	0	1	0	0	0	0	0	0	D5	D4	D3	D2	D1	D0

NRP-G5 to NRP-G0: 0 to 63. Default = 0

This register specifies the third switching timing of the fall NR drive waveform.

The NR3 waveform is output for a number of periods equal to the difference between NRP-F and NRP-G.

17	0	0	0	1	0	0	0	1	0	0	D5	D4	D3	D2	D1	D0

NRP-H5 to NRP-H0: 0 to 63. Default = 0

This register specifies the fourth switching timing of the fall NR drive waveform.

The NR2 waveform is output for a number of periods equal to the difference between NRP-G and NRP-H, and the NR1 waveform is output for a number of periods equal to the difference between NRP-H and NRPUL2.

When setting the fall NR drive waveforms, the setting values should in principle satisfy the following relationship.

NRP-E ≤ NRP-F ≤ NRP-G ≤ NRP-H

(When this relationship is not satisfied, unintended drive waveforms may be output. However, this will not result in IC breakdowns or other damage.)

18	0	0	0	1	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0

NR1GTBR7 to NR1GTBR0: 0 to 255. Default = 0
GATE_B pulse reset value for NR1 waveform

19	0	0	0	1	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

NR1GTBS7 to NR1GTBS0: 0 to 255. Default = 0
GATE_B pulse set value for NR1 waveform

20	0	0	0	1	0	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0

NR2GTBR7 to NR2GTBR0: 0 to 255. Default = 0
GATE_B pulse reset value for NR2 waveform

21	0	0	0	1	0	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0

NR2GTBS7 to NR2GTBS0: 0 to 255. Default = 0
GATE_B pulse set value for NR2 waveform

22	0	0	0	1	0	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0

NR3GTBR7 to NR3GTBR0: 0 to 255. Default = 0
GATE_B pulse reset value for NR3 waveform

23	0	0	0	1	0	1	1	1	D7	D6	D5	D4	D3	D2	D1	D0

NR3GTBS7 to NR3GTBS0: 0 to 255. Default = 0
GATE_B pulse set value for NR3 waveform

24	0	0	0	1	1	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

NR4GTBR7 to NR4GTBR0: 0 to 255. Default = 0
GATE_B pulse reset value for NR4 waveform

25	0	0	0	1	1	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0

NR4GTBS7 to NR4GTBS0: 0 to 255. Default = 0
GATE_B pulse set value for NR4 waveform

26	0	0	0	1	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0

NR5GTBR7 to NR5GTBR0: 0 to 255. Default = 0
GATE_B pulse reset value for NR5 waveform

27	0	0	0	1	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

NR5GTBS7 to NR5GTBS0: 0 to 255. Default = 0
GATE_B pulse set value for NR5 waveform

28	No register address								D7	0	0	0	0	0	0	0

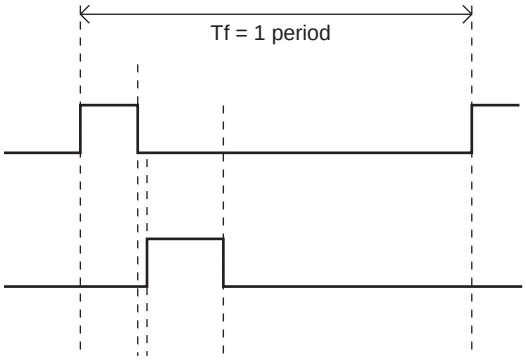
READ only register line.

D7 : BUSY register Set to 1 when the IC is performing the output operation.
Set to 0 when the IC stops the output operation.

Functional Description

1 period :

One period of OUT waveform operation is equivalent to one output operation.



Initialization sequence (on or off and direction can be set by I^2C) :

This is an internal sequence in which the actuator is moved to the initial position when the IC is started up.
Switching the value of ENIN register from 0 to 1 starts the IC.
The presence or absence of the initialization operation can be set using the initialization mode select register (INIT). If the initialization operation is specified, the direction of the initialization sequence can be set using the M/I register.

- M/I register = 0 : Initialization processing in infinity direction
  The IC performs the number of operations determined by STP setting period × INIT setting times in the infinite direction, then waits for the period equivalent to STP setting period × 4 times, and performs the number of swing back operations equal to STP setting period × RET setting times in the macro direction.
- M/I register = 1 : Auto macro operation in macro direction
  The IC performs the number of operations determined by STP setting period × INIT setting times in the macro direction, then waits for the period equivalent to STP setting periods × 4, and performs the number of swing back operations equal to STP period setting period × RET setting times in the infinity direction.

CLK input :

The input pin for the external CLK input that provides the reference time for generating drive waveforms.
The frequency division ratio for I^2C communication can be selected from 1/4, 1/2, and 1/1.
Drive waveforms are generated by counting this frequency-divided clk pulses as the basic count unit.
The LV8491CT supports frequency range of 10MHz to 60MHz depending on the frequency division ratio and counter settings.

Register setting sequence example

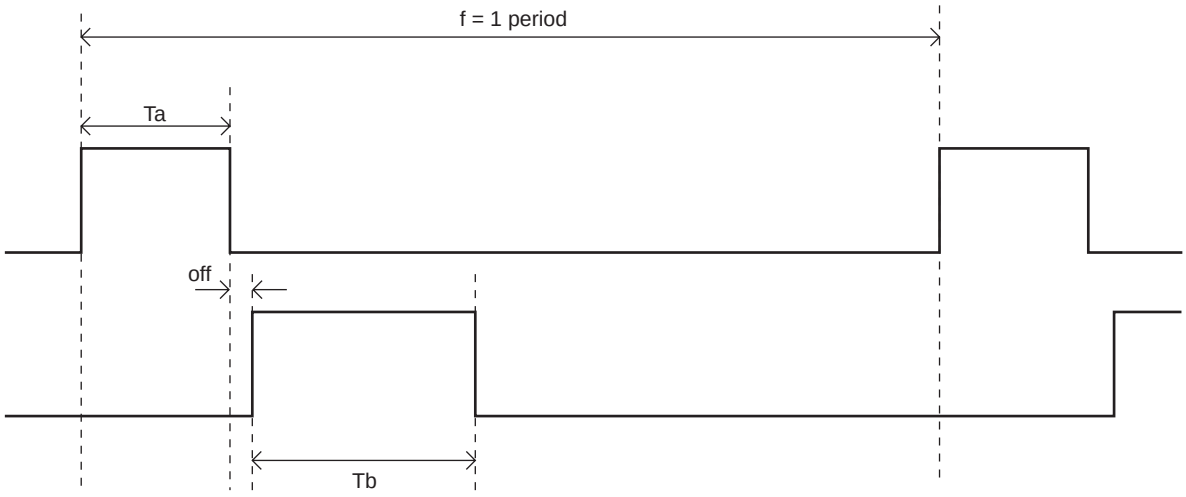
(1) Apply V_{CC}.
(2) Set up the register address 0x01 to 0x07 (setting up waveform and drive conditions)
(3) Set the ENIN register to 1 (initialization startup when the initialization sequence is enabled, or IC startup).
(4) AF operation starts (actuator operation instruction) according to the M/I and DRVPULSE settings.

I^2C communication during output operation

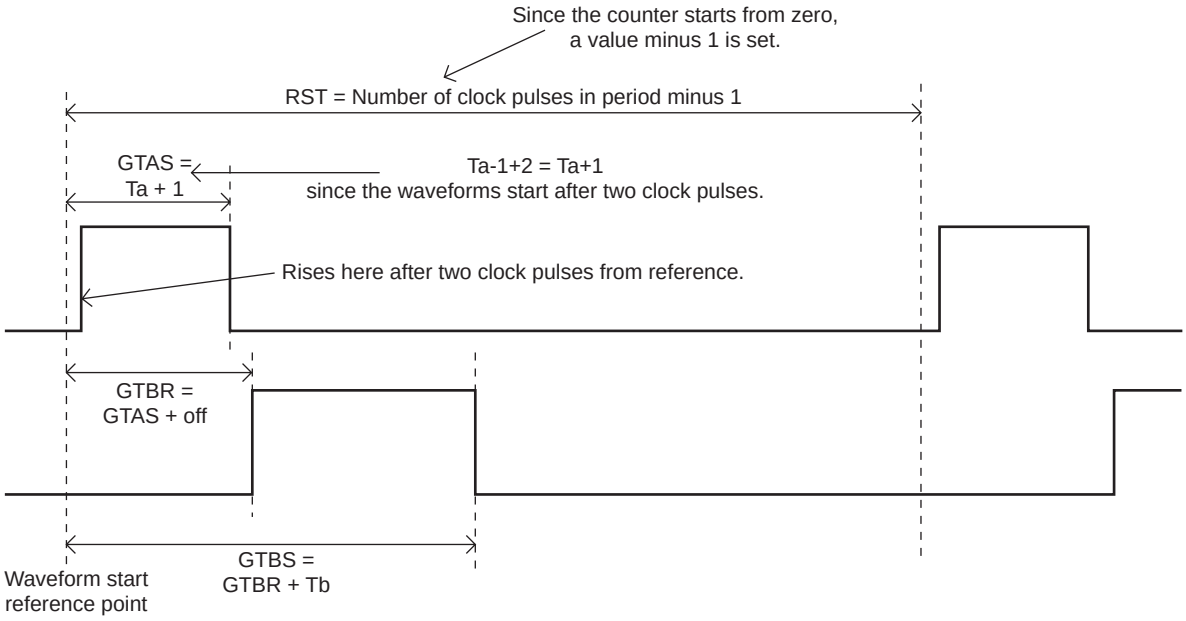
I^2C communication is possible to all registers during IC operation (during OUT output or when BUSY is high).
However, note that when drive waveform settings are changed during actuator or other operation, unintended waveforms may be output.

Actuator drive waveform settings :

Configuration of piezoelectric actuator drive waveform



Drive parameter settings



The drive waveforms are set using four parameters: RST, GTAS, GTBR and GTBS.

RST : Parameter determines the period, and sets the reference clock pulse count minus 1.

GTAS : Parameter determines the time taken for the gate signal A to the falling edge from the reference point. Since the signal raises after two clock pulses from the reference, the Ta reference clock cycle count plus 1 is set.

GTBR : Parameter determines the time taken for the gate signal B to the rising edge from the reference point. It sets the value obtained by adding the reference clock pulse count during the time from GTAS to “off.”

GTBS : Parameter determines the time taken for the gate signal B to the falling ewdge from the reference point. It sets the value obtained by adding the reference clock pulse count during the time from GTBR to “Tb.”

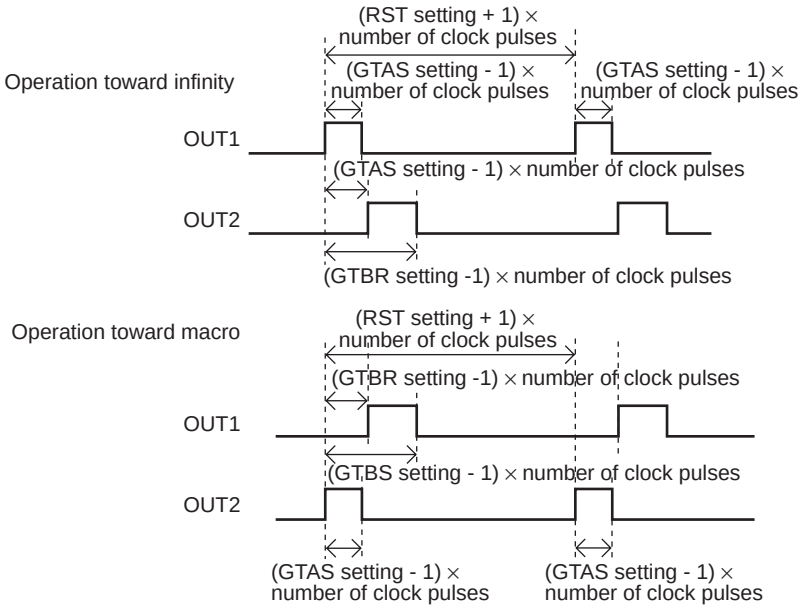
[Example of settings] When setting reference clock to 10MHz, period to 13μs, Ta to 2.0μs, off to 0.3μs, and Tb to 3.0μs

Since the reference clock time is 0.1μs :

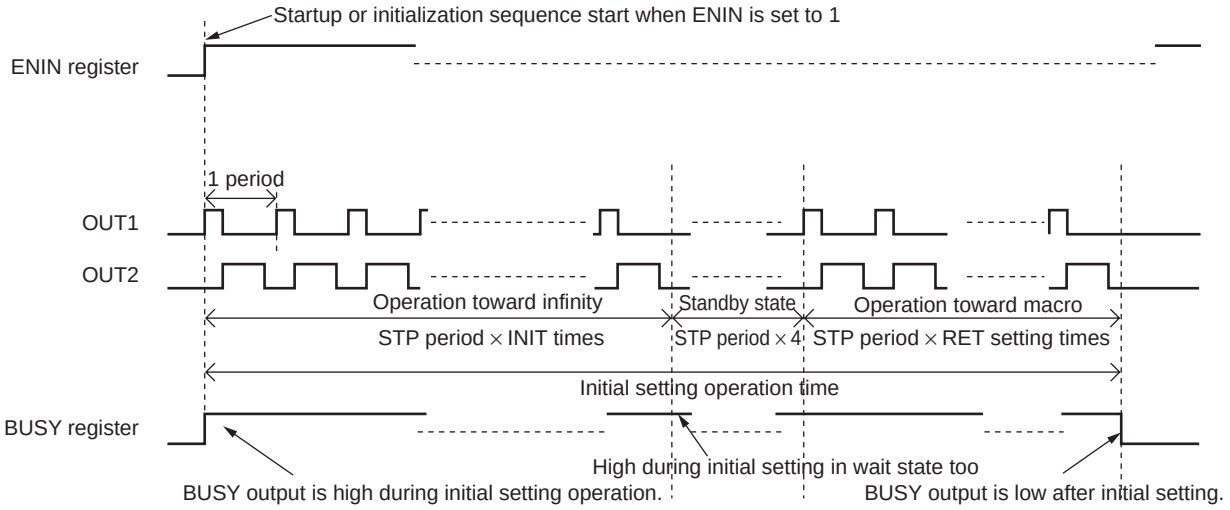
The period is 130 clks. → Specify 129 (RST value of 130 -1).
Ta is 20 clks. → Specify 21 (GTAS value of 20 + 1).
off is 3 clks. → Specify 24 (GTBR value of 21 + 3).
Tb is 30 clks. → Specify 54 (GTBS value of 24 + 30).

Timing charts

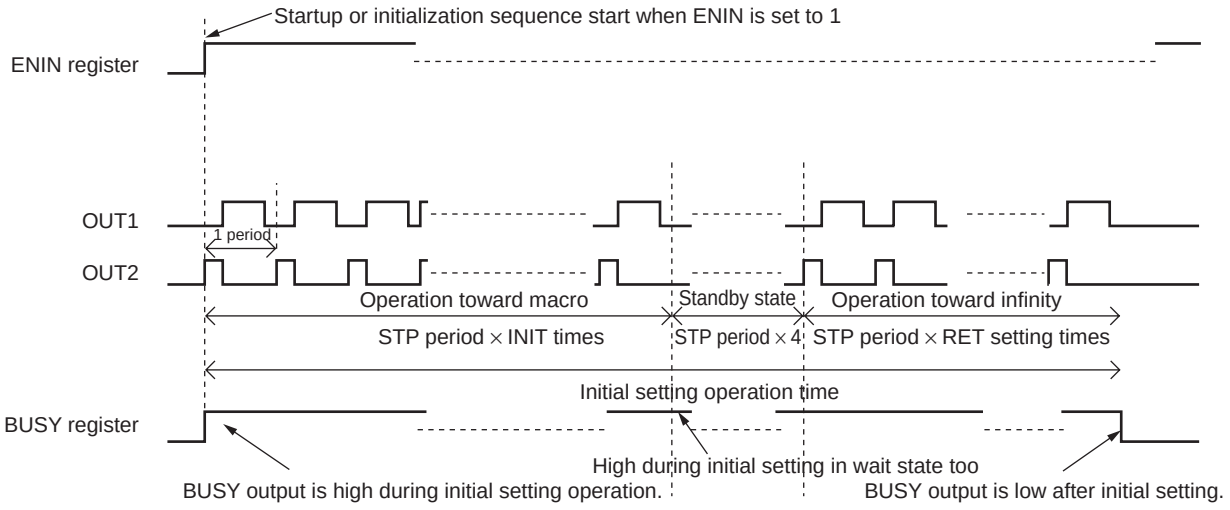
Enlarged view of the sequence of output signals



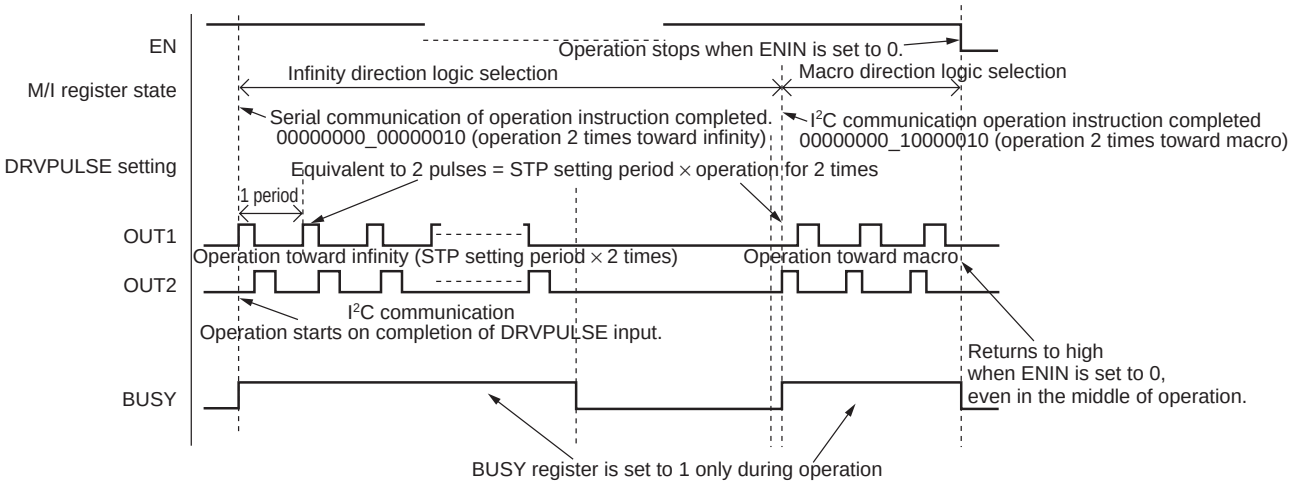
Sequence of initial setting operation (“on” or “off” can be set by the serial settings.)
When M/I register = 00 → Movement toward infinity position



When M/I register = 01 → Movement toward macro position



Sequence of operations triggered by DRVPULSE input



Gate setting output logic