



1GB – 2x64Mx64 DDR SDRAM UNBUFFERED

FEATURES

- PC2700 @ CL2.5
- Double-data-rate architecture
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Auto and self refresh, (8K/64ms refresh)
- Serial presence detect
- Power supply: V_{CC}/V_{CCQ} : 2.5V $\pm$ 0.2V
- Dual Rank
- Standard 200 pin SO-DIMM package
 - Package height options:
D4: 31.75 mm (1.25")

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The WV3EG264M64EFSU is a 2x64Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM component. The module consists of sixteen 64Mx8 bit with 4 banks DDR SDRAMs in FBGA packages mounted on a 200 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change without notice.

OPERATING FREQUENCIES

	DDR333 @CL=2.5
Clock Speed	166MHz
CL-trCD-trP	2.5-3-3

**PIN CONFIGURATION**

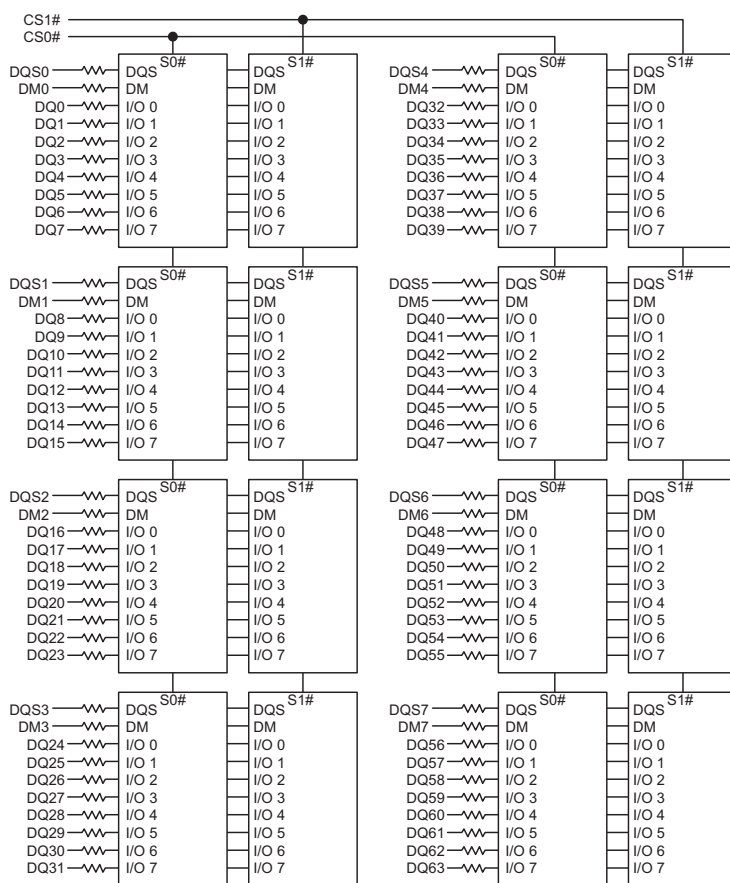
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V _{REF}	51	V _{SS}	101	A9	151	DQ42
2	V _{REF}	52	V _{SS}	102	A8	152	DQ46
3	V _{SS}	53	DQ19	103	V _{SS}	153	DQ43
4	V _{SS}	54	DQ23	104	V _{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V _{CC}
6	DQ4	56	DQ28	106	A6	156	V _{CC}
7	DQ1	57	V _{CC}	107	A5	157	V _{CC}
8	DQ5	58	V _{CC}	108	A4	158	CK1#
9	V _{CC}	59	DQ25	109	A3	159	V _{SS}
10	V _{CC}	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	V _{SS}
12	DM0	62	DM3	112	A0	162	V _{SS}
13	DQ2	63	V _{SS}	113	V _{CC}	163	DQ48
14	DQ6	64	V _{SS}	114	V _{CC}	164	DQ52
15	V _{SS}	65	DQ26	115	A10	165	DQ49
16	V _{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V _{CC}
18	DQ7	68	DQ31	118	RAS#	168	V _{CC}
19	DQ8	69	V _{CC}	119	WE#	169	DQS6
20	DQ12	70	V _{CC}	120	CAS#	170	DM6
21	V _{CC}	71	NC	121	CS0#	171	DQ50
22	V _{CC}	72	NC	122	CS1#	172	DQ54
23	DQ9	73	NC	123	NC	173	V _{SS}
24	DQ13	74	NC	124	NC	174	V _{SS}
25	DQS1	75	V _{SS}	125	V _{SS}	175	DQ51
26	DM1	76	V _{SS}	126	V _{SS}	176	DQ55
27	V _{SS}	77	NC	127	DQ32	177	DQ56
28	V _{SS}	78	NC	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	V _{CC}
30	DQ14	80	NC	130	DQ37	180	V _{CC}
31	DQ11	81	V _{CC}	131	V _{CC}	181	DQ57
32	DQ15	82	V _{CC}	132	V _{CC}	182	DQ61
33	V _{CC}	83	NC	133	DQS4	183	DQS7
34	V _{CC}	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V _{SS}
36	V _{CC}	86	NC	136	DQ38	186	V _{SS}
37	CK0#	87	V _{SS}	137	V _{SS}	187	DQ58
38	V _{SS}	88	V _{SS}	138	V _{SS}	188	DQ62
39	V _{SS}	89	NC	139	DQ35	189	DQ59
40	V _{SS}	90	V _{SS}	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	V _{CC}
42	DQ20	92	V _{CC}	142	DQ44	192	V _{CC}
43	DQ17	93	V _{CC}	143	V _{CC}	193	SDA
44	DQ21	94	V _{CC}	144	V _{CC}	194	SA0
45	V _{CC}	95	CKE1	145	DQ41	195	SCL
46	V _{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V _{CCSPD}
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	V _{SS}	199	NC
50	DQ22	100	A11	150	V _{SS}	200	NC

PIN NAMES

A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0, CK0#	Clock Input
CK1, CK1#	Clock Input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data-In Mask
V _{CC}	Power Supply (2.5V)
V _{CCQ}	Power Supply for DQS (2.5V)
V _{SS}	Ground
V _{REF}	Power Supply for Reference
V _{CCSPD}	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
NC	No Connect

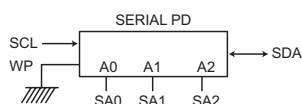
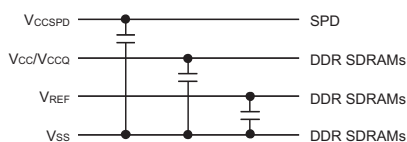


FUNCTIONAL BLOCK DIAGRAM



BA0-BA1 → DDR SDRAMs
A0-A12 → DDR SDRAMs
RAS# → DDR SDRAMs
CAS# → DDR SDRAMs
WE# → DDR SDRAMs
CKE0 → DDR SDRAMs
CKE1 → DDR SDRAMs

Clock Wiring	
Clock Input	SDRAMs
CK0/CK0#	8 SDRAMs
CK1/CK1#	8 SDRAMs



NOTE: All datalines are terminated through a 22 ohm series resistor

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 3.3	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1.0 to 3.6	V
Voltage on V _{CCQ} supply relative to V _{SS}	V _{CCQ}	-1.0 to 3.6	V
Storage Temperature	T _{STG}	-55 to +150	°C
Operating Temperature	T _A	0 to +70	°C
Power Dissipation	P _D	16	W
Short Circuit Current	I _{OS}	50	mA

Note:

- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC CHARACTERISTICS0°C ≤ T_A ≤ 70°C, V_{CC} = 2.5V ± 0.2V

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage DDR266/DDR333 (nominal V _{CC} of 2.5V)	V _{CC}	2.3	2.7		
I/O Supply voltage DDR266/DDR333 (nominal V _{CC} of 2.5V)	V _{CCQ}	2.3	2.7	V	
I/O Reference voltage	V _{REF}	0.49*V _{CCQ}	0.51*V _{CCQ}	V	1
I/O Termination voltage	V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage	V _{IH} (DC)	V _{REF} +0.15	V _{CCQ} +0.30	V	
Input logic low voltage	V _{IL} (DC)	-0.3	V _{REF} -0.15	V	
Input voltage level, CK and CK#	V _{IN} (DC)	-0.3	V _{CCQ} +0.30	V	
Input differential voltage, CK and CK#	V _{ID} (DC)	0.3	V _{CCQ} +0.60	V	3
Input crossing point voltage, CK and CK#	V _{IX} (DC)	0.3	V _{CCQ} +0.60	V	
Input leakage current	Addr, CAS#, RAS#, WE#	I _I	-32	32	uA
	CS#, CKE		-16	16	uA
	CK, CK#		-16	16	uA
	DM		-4	4	uA
Output leakage current	I _{OZ}	-10	10	uA	
Output high current (normal strength); V _{OUT} = V + 0.84V	I _{OH}	-16.8	—	mA	
Output high current (normal strength); V _{OUT} = V _{TT} - 0.84V	I _{OL}	16.8	—	mA	
Output high current (half strength); V _{OUT} = V _{TT} + 0.45V	I _{OH}	-9	—	mA	
Output high current (half strength); V _{OUT} = V _{TT} - 0.45V	I _{OL}	9	—	mA	

NOTES:

- V_{REF} is expected to be equal to 0.5*V_{CCQ} of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on V_{REF} may not exceed ±2% of the DC value
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

CAPACITANCEV_{CC} = 2.5V, V_{CCQ} = 2.5V, T_A = 25°C, f = 1MHz

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12, BA0-BA1, RAS#, CAS#, WE#)	C _{IN1}	28	44	pF
Input Capacitance (CKE0, CKE1)	C _{IN2}	16	24	pF
Input Capacitance (CS0#, CS1#)	C _{IN3}	16	24	pF
Input Capacitance (CK0, CK0#, CK1, CK1#)	C _{IN4}	16	24	pF
Input Capacitance (DM0-DM7)	C _{IN5}	11	13	pF
Data and DQS input/output capacitance (DQ0-DQ63)	C _{OUT}	11	13	pF

**AC OPERATING TEST CONDITIONS**

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.31$		V	1
Input Low (Logic 0) Voltage	$V_{IL(AC)}$		$V_{REF} - 0.31$	V	1
Input Differential Voltage, CK and CK# inputs	$V_{ID(AC)}$	0.7	$V_{CCQ} + 0.6$	V	
Input Crossing Point Voltage, CK and CK# inputs	$V_{IX(AC)}$	$0.5 \cdot V_{CCQ} - 0.2$	$0.5 \cdot V_{CCQ} + 0.2$	V	

NOTES:

- V_{IH} overshoot: $V_{IH} = V_{CCQ} + 1.5V$ for a pulse width $< 3ns$ and the pulse can not be greater than 1/3 of the cycle rate.
 V_{IL} undershoot: $V_{IL} = -1.5V$ for a pulse width $< 3ns$ and the pulse can not be greater than 1/3 of the cycle rate.

**I_{DD} SPECIFICATIONS AND TEST CONDITIONS**0°C ≤ T_A ≤ 70°C, V_{CCQ} = 2.5V ± 0.2V, V_{CC} = 2.5V ± 0.2V

Parameter	Symbol	Conditions	DDR333 @ CL = 2.5 Max	Unit
Operating current	I _{DD0} *	One device bank active; Active-Precharge; t _{RC} = t _{RC(MIN)} ; t _{CK} = t _{CK(MIN)} ; DQ, DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles	1080	mA
Operating current	I _{DD1} *	One device bank; Active-Read-Precharge; BL = 4; t _{RC} = t _{RC(MIN)} ; t _{CK} = t _{CK(MIN)} ; I _{OUT} = 0mA; Address and control inputs change once per clock cycle	1320	mA
Percharge power-down standby current	I _{DD2P} **	All device banks are idle; Power-down mode; t _{CK} = t _{CK(MIN)} ; CKE = LOW	80	mA
Idle standby current	I _{DD2F} **	CS# = HIGH; All device banks are idle; t _{CK} = t _{CK(MIN)} ; CKE = HIGH; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS and DM	720	mA
Active power-down standby current	I _{DD3P} **	One device bank active; Power-down mode; t _{CK} = t _{CK(MIN)} ; CKE = LOW	560	mA
Active standby current	I _{DD3N} **	CS# = HIGH; CKE = HIGH; One device bank active; t _{RC} = t _{RAS(MAX)} ; t _{CK} = t _{CK(MIN)} ; DQ, DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle	800	mA
Operating current	I _{DD4R} *	Burst = 2; Reads; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; t _{CK} = t _{CK(MIN)} ; I _{OUT} = 0mA	1360	mA
Operating current	I _{DD4W} *	Burst = 2; Writes; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; t _{CK} = t _{CK(MIN)} ; DQ, DM and DQS inputs change twice per clock cycle	1440	mA
Auto refresh current	I _{DD5} **	t _{RC} = t _{RFC(MIN)}	4640	mA
Self refresh current	I _{DD6} **	CKE < 0.2V	80	mA
Operating current	I _{DD7A} *	Four device bank interleaving Reads Burst = 4 with auto precharge; t _{RC} = t _{RFC(MIN)} ; t _{CK} = t _{CK(MIN)} ; Address and control inputs change only during Active READ, or WRITE commands	3280	mA

NOTE:

I_{DD} specification is based on Micron components. Other DRAM Manufacturers specification may be different.* Value calculated as one module rank in this operation condition and other module rank in I_{DD2P} (CKE low) mode.

** Value calculated as all module ranks in this operation condition.



AC TIMING PARAMETERS

Parameter	Symbol	335		Unit
		Min	Max	
Row cycle time	t _{RC}	60		ns
Refresh row cycle time	t _{RFC}	72		ns
Row active time	t _{RAS}	42	70K	ns
RAS# to CAS# delay	t _{RCD}	15		ns
Row precharge time	t _{RP}	15		ns
Row active to Row active delay	t _{RRD}	12		ns
Write recovery time	t _{WR}	15		ns
Last data into Read command	t _{WTR}	1		t _{CK}
Clock cycle time	CL = 2.5 t _{CK}	6	13	ns
Clock high level width	t _{CH}	0.45	0.55	t _{CK}
Clock low level width	t _{CL}	0.55	0.55	t _{CK}
DQS-out access time from CK/CK#	t _{DQSQ}	-0.6	+0.6	ns
Output data access time from CK/CK#	t _{AC}	-0.7	+0.7	ns
Data strobe edge to output data edge	t _{DQSQ}	—	0.45	ns
Read Preamble	t _{RPRE}	0.9	1.1	t _{CK}
Read Postamble	t _{RPST}	0.4	0.6	t _{CK}
CK to valid DQS-in	t _{DQSS}	0.75	1.25	t _{CK}
DQS-in setup time	t _{WPRES}	0		ns
DQS-in hold time	t _{WPRE}	0.25		t _{CK}
DQS falling edge to CK rising-setup time	t _{DSS}	0.2		t _{CK}
DQS falling edge from CK rising-hold time	t _{DSH}	0.2		t _{CK}
DQS-in high level width	t _{DQSH}	0.35		t _{CK}
DQS-in low level width	t _{DQSL}	0.35		t _{CK}
Address and Control Input setup time (fast)	t _{IS}	0.75		ns
Address and Control Input hold time (fast)	t _{IH}	0.75		ns
Address and Control Input setup time (slow)	t _{IS}	0.7		ns
Address and Control Input hold time (slow)	t _{IH}	0.7		ns
Data-out high impedance time from CK/CK#	t _{HZ}		+0.7	ns
Data-out low impedance time from CK/CK#	t _{LZ}	-0.7		ns

Note:

AC Timing Parameters are based on Micron components. Other DRAM Manufacturers parameters may be different.



AC TIMING PARAMETERS (Continued)

Parameter	Symbol	335		Unit
		Min	Max	
Mode register set cycle time	tMRD	10		ns
DQ & DM setup time to DQS	tDS	0.4		ns
DQ & DM hold time to DQS	tDH	0.4		ns
Control & Address input pulse width	tIPW	2.2		ns
DQ & DM input pulse width	tDIPW	1.75		ns
Exit self refresh o non-Read command	tXSNR	75		ns
Exit self refresh to read command	tXSRD	200		tCK
Refresh interval time	tREFI		7.8	us
Output DQS valid window	tQH	tHP - tQHS	—	ns
Clock half period	tHP	tCL(min) or tCH(min)	—	ns
Data hold skew factor	tQHS		0.55	ns
DQS write postamble time	tWPST	0.4	0.6	tCK
Active to Read with Auto precharge command	tRAP	15		
Auto precharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		tCK



Part Number	Speed	CAS Latency	t _{RCD}	t _{RP}	Height*
WV3EG264M64EFSU335D4xG	166MHz/333Mb/s	2.5	3	3	31.75mm (1.25")

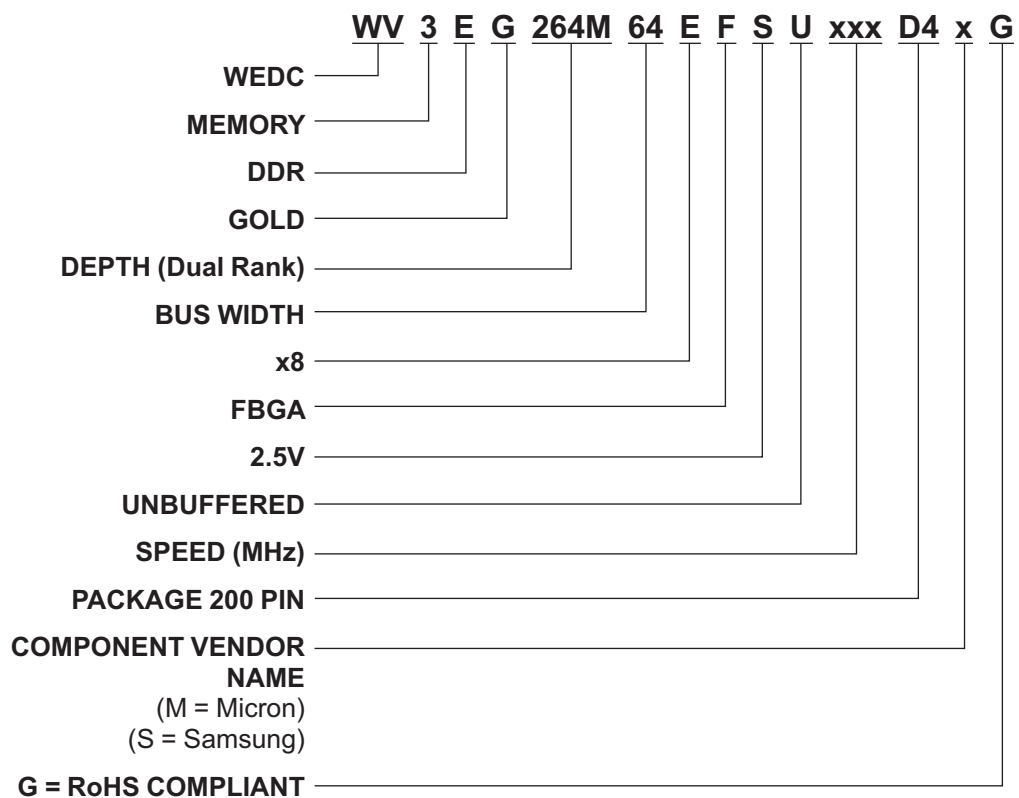
NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

Technical drawing of a 16-pin connector housing. The drawing includes a top view showing a 2x8 grid of pins and a side view showing the profile of the housing. Dimensions are provided in both inches and millimeters. Key dimensions include overall width of 67.60 (2.661), pin pitch of 1.00 (0.04), and pin diameter of 0.25 (0.01). The drawing also shows a detail of the pin profile with a maximum width of 3.80 (0.150) and a minimum height of 4.00 (0.158).



PART NUMBERING GUIDE





WHITE ELECTRONIC DESIGNS

WV3EG264M64EFSU-D4

PRELIMINARY

Document Title

1GB – 2x64Mx64 DDR SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	8-05	Preliminary